1990

INTEGRATED CIRCUITS

DATA BOOK

Siliconix
incorporated

Siliconix incorporated reserves the right to make changes in the circuitry or specifications at any time without notice and assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Warning Regarding Life Support Applications

Siliconix products are not sold for applications in any medical equipment intended for use as a component of any life support system unless a specific written agreement pertaining to such intended use is executed between the manufacturer and Siliconix. Such agreement will require the equipment manufacturer either to contract for additional reliability testing of the Siliconix parts and/or to commit to undertake such testing as a part of its manufacturing process. In addition, such manufacturer must agree to indemnify and hold Siliconix harmless from any claims arising out of the use of the Siliconix parts in life support equipment.

Stresses listed under "Absolute Maximum Ratings" may be applied (one at a time) to devices without resulting in permanent damage. This is a stress rating only and not subject to production testing. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding absolute maximum ratings for any time may result in permanent degradation, damage, or even destruction of the device.

Printed in U.S.A.

Siliconix incorporated

SILICONIX
INTEGRATED CIRCUITS

For over 25 years, Siliconix, has been a leading supplier of a broad selection of analog integrated circuits (ICs), small-signal FETs, and power MOSFETs. With worldwide corporate and manufacturing headquarters in Santa Clara, California, Siliconix also has manufacturing facilities in Wales and Taiwan.

The IC products detailed in this data book include analog switches and multiplexers, wideband/video switches, multiplexers, crosspoints, buffers, amplifiers and voltage converters. These products are designed for applications in the industrial, computer peripherals, communications, and military markets. Siliconix serves these customers with products of unequaled performance, quality and reliability through the use of our leading design, processing, packaging and testing technologies.

The product specifications listed in this data book are arranged in a simplified format. The electrical tables and performance curves contain detailed information, simplifying the tasks of design and component engineers. Each of the data sheets is controlled by the Siliconix Quality Assurance organization, which guarantees that all limits stated are fully tested in production.

Some mature products continue to be available and are listed in the Siliconix Price List. For information on these products, contact your nearest Siliconix sales office.

We solicit your comments and suggestions, and look forward to continually serving your future analog integrated circuit requirements.

About This Edition of the Siliconix Integrated Circuit Data Book

NEW PRODUCT DATA SHEETS APPEARING FOR THE FIRST TIME:

DISCONTINUED/NEW UPGRADE CROSS REFERENCE:

Part Number	Availability/Replacement/Upgrade	Part Number	Availability/Replacement/Upgrade
D125	Note 1	DG5045	DG405
D129	Note 1	DG5140	DG401
DG123	Note 1	DG5141	DG401
DG125	Note 1	DG5142	DG403
DG126	Note 1	DG5143	DG403
DG134	Note 1	DG5144	DG405
DG143	Note 1	DG5145	DG405
DG144	Note 1	DGP201A	DG441
DG145	Note 1	DGP303	DG403
DG146	Note 1	G118	Note 1
DG400	DG401	G119	Note 1
DG402	DG403	IS05	Note 2
DG404	DG405	Si2504	Note 3
DG526	Note 1	Si7541	Note 1
DG527	Note 1	Si7542	Note 1
DG568	Note 1	Si7543	Note 1
DG569	Note 1	Si7545	Note 1
DG5040	DG401	Si7820	Note 1
DG5041	DG401	Si8603	Note 1
DG5042	DG403	Si8604	Note 1
DG5044	DG405		

NOTES:

1. Obsolete product.
2. Obsolete product. Contact Universal Semiconductor.
3. Obsolete product. Contact International Microcircuits.

Siliconix incorporated

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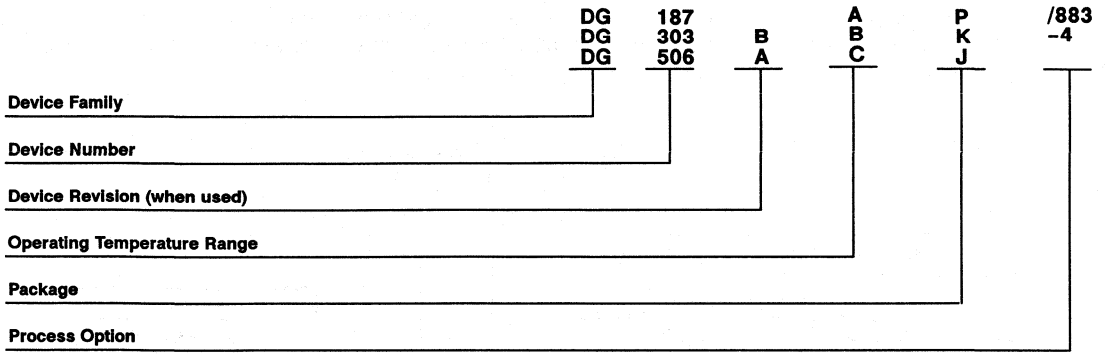
ALPHA-NUMERIC INDEX

DEVICE ORDERING INFORMATION

Integrated Circuits



DEVICE FAMILY
(1 or 2 Letters)

DG - Analog Switches and Analog Multiplexers
SI - Siliconix Proprietary Integrated Circuit or Second Source Part

DEVICE NUMBER
(3 Digit Numbers)

OPERATING TEMPERATURE RANGE
(1 Letter)

A -55 to 125°C
B -25 to 85°C
C 0 to 70°C
D -40 to 85°C

B and D temperature range parts receive industrial processing unless a process option dash number is added to the part number.

C temperature range parts are given commercial processing.

All possible combinations of device types, temperature ranges, package types and MIL-883 process options are not necessarily available. Consult individual data book pages or sales office for complete information.

PACKAGE
(1 Letter)

A - Metal Can
J - Dual-In-Line Package-Plastic
K - Dual-In-Line Package-CERDIP
M - Ceramic J-Leaded Chip Carrier (CLCC)
N - Plastic J-Leaded Chip Carrier PLCC
P - Dual-In-Line Package-Side Braze
R - Dual-In-Line Package-Side Braze
Y - Small Outline Package (SOIC)
Z - Leadless Chip Carrier (LCC)

PROCESS OPTION

/883 - Processing to the current revision of MIL-STD-883, Level B. Compliant-Non JAN
-4 - 160 Hour Burn-In
/BS - BS9000 Compliant

JAN38510 ORDERING INFORMATION ANALOG SWITCHES AND MULTIPLEXERS

Several Siliconix Analog Switches and multiplexers are available fully certified on the QPL (Qualified Parts List) published monthly by Defense Electronics Supply Center (DESC). The QPL numbers follow this format: JM38510/XXXXX. Refer to the current Siliconix Price list for available part types and order numbers.

JAN Part Numbering System

J M38510 /111 07 B E C

"JAN" Certification Mark

Military Designator

Detail Specification (Slash Sheet)

/111--DG181 Series
/116--DG300A Series
/123--DG200A Series
/190--DG506 Series

	Device Type	
/111	01-DG181 02-DG182 03-DG184 04-DG185	05-DG187 06-DG188 07-DG190 08-DG191
/116	01-DG300A 02-DG301A 03-DG302A 04-DG303A	05-DG304A 06-DG305A 07-DG306A 08-DG307A
/123	01-DG200A	02-DG201A
/190	01-DG506A 03-DG507A	07-DG508A 08-DG509A

Lead Finish

A--Solder Dip
C--Gold Plate

Case Outline

C--14-Lead Dual in Line
E--16-Lead Dual in Line
I--10-Lead Metal Can
D--14-Lead Flatpack
X--28-Pin Dual in Line

Device Class

S--Class S
B--Class B

Available JAN Parts

Generic Part Number	JAN Part Number
DG181AP/883	JM38510/11101BCC
DG181AP/883	JM38510/11101BCA
DG181AA/883	JM38510/11101BIC
DG181AL/883	JM38510/11101BDC
DG182AP/883	JM38510/11102BCC
DG182AP/883	JM38510/11102BCA
DG182AA/883	JM38510/11102BIC
DG182AL/883	JM38510/11102BDC
DG184AP/883	JM38510/11103BEC
DG184AP/883	JM38510/11103BEA
DG184AL/883	JM38510/11103BDC
DG185AP/883	JM38510/11104BEC
DG185AP/883	JM38510/11104BEA
DG185AL/883	JM38510/11104BDC

Available JAN Parts (continued)

Generic Part Number	JAN Part Number
DG187AP/883	JM38510/11105BCC
DG187AP/883	JM38510/11105BCA
DG187AA/883	JM38510/11105BIC
DG187AL/883	JM38510/11105BDC
DG188AP/883	JM38510/11106BCC
DG188AP/883	JM38510/11106BCA
DG188AA/883	JM38510/11106BIC
DG188AL/883	JM38510/11106BDC
DG190AP/883	JM38510/11107BEC
DG190AP/883	JM38510/11107BEA
DG190AL/883	JM38510/11107BDC
DG191AP/883	JM38510/11108BEC
DG191AP/883	JM38510/11108BEA
DG191AL/883	JM38510/11108BDC
DG200AAP/883	JM38510/12301BCC
DG200AAP/883	JM38510/12301BCA
DG200AAA/883	JM38510/12301BIC
DG201AAP/883	JM38510/12302BEC
DG201AAP/883	JM38510/12302BEA
DG300AAP/883	JM38510/11601BCC
DG300AAP/883	JM38510/11601BCA
DG300AAA/883	JM38510/11601BIC
DG301AAP/883	JM38510/11602BCC
DG301AAP/883	JM38510/11602BCA
DG301AAA/883	JM38510/11602BIC
DG302AAP/883	JM38510/11603BCC
DG302AAP/883	JM38510/11603BCA
DG303AAP/883	JM38510/11604BCC
DG303AAP/883	JM38510/11604BCA
DG304AAP/883	JM38510/11605BCC
DG304AAP/883	JM38510/11605BCA
DG304AAA/883	JM38510/11605BIC
DG305AAP/883	JM38510/11606BCC
DG305AAP/883	JM38510/11606BCA
DG305AAA/883	JM38510/11606BIC
DG306AAP/883	JM38510/11607BCC
DG306AAP/883	JM38510/11607BCA
DG307AAP/883	JM38510/11608BCC
DG307AAP/883	JM38510/11608BCA
DG506AAR/883	JM38510/19001BXC
DG507AAR/883	JM38510/19003BXC
DG508AAP/883	JM38510/19007BEA
DG508AAP/883	JM38510/19007BEC
DG509AAP/883	JM38510/19008BEA
DG509AAP/883	JM38510/19008BEC

STANDARD MILITARY DRAWING (SMD) /883 Compliant/Non-JAN Class B

Siliconix offers products which meet requirements of MIL-STD-883, paragraph 1.2.1, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices."

SMD Compliant/Non-JAN

SMD/DESC Part #	Generic Part #
7705201EA	DG508AAK DESC
7705201EC	DG508AAK DESC
7705201FA	DG508AAL/883
7705201FC	DG508AAL DESC
7705301EA	DG201AAK DESC
7705301EC	DG201AAP DESC
7801401CA	DG129AP DESC
7801401CC	DG129AP DESC
8100601EA	DG5140AK DESC
8100602EA	DG5141AK DESC
8100603EA	DG5142AK DESC
8100604EA	DG5143AK DESC
8100605EA	DG5144AK DESC
8100605IC	DG5144AA DESC
8100606EA	DG5145AK DESC
8100609EA	DG5140AK DESC
8100609IC	DG5140AA DESC
8100610EA	DG5141AK DESC
8100610IC	DG5141AA DESC
8100611EA	DG5142AK DESC
8100612EA	DG5143AK DESC
8100613EA	DG5144AK DESC
8100613IC	DG5144AA DESC
8100614EA	DG5145AK DESC
5962-9056901EA	DG401AK/883
5962-90569012A	DG401AZ/883
5962-8976301EA	DG403AK/883
5962-89763012A	DG403AZ/883
5962-8996101EA	DG405AK/883
5962-89961012A	DG401AZ/883

Class B /883 Compliant/Non-JAN

Industry Part #	Siliconix Part #
AD7506JD/883	DG506AAR/883
AD7507JD	DG507AAR/883
AH129D/883	DG129AP/883
AH0133D/883	DG133AP/883
AH0139D/883	DG139AP/883
AH0140D/883	DG140AP/883
AH0141D/883	DG141AP/883
AH0143D/883	DG143AP/883
AH0151D/883	DG141AP/883
AH0152D/883	DG133AP/883
AH0153D/883	DG140AP/883
AH0154D/883	DG129AP/883

Industry Part #	Siliconix Part #
AH0164D/883	DG139AP/883
DGM184AK/HR	DG405AK/883
DGM184AK/883B	DG405AK/883
DGM185AK/HR	DG405AK/883
DG185AK/883	DG405AK/883
DGM190AK/HR	DG403AK/883
DGM189AK/883B	DG403AK/883
ADG191AK/HR	DG403AK/883
DG129AL	DG129AL/883
DG129AL-2	DG129AL/883
DG129AL/HR	DG129AL/883
DG129AL/883	DG129AL/883

Industry Part #	Siliconix Part #
DG129AL/883B	DG129AL/883
DG129AP-2	DG129AP/883
DG129AP/883	DG129AP/883
DG133AP-2	DG133AP/883
DG133AP/883	DG133AP/883
DG139AP-2	DG139AP/883
DG139AP/883	DG139AP/883
DG140AL	DG140AL/883
DG140AL-2	DG140AL/883
DG140AL/HR	DG140AL/883
DG140AL/883	DG140AL/883
DG140AP-2	DG140AP/883

Class B /883 Compliant/Non-JAN (Cont'd)

Industry Part #	Siliconix Part #
DG140AP/HR	DG140AP/883
DG140AP/883	DG140AP/883
DG141AL	DG141AL/883
DG141AL-2	DG141AL/883
DG141AL/HR	DG141AL/883
DG141AL/883	DG141AL/883
DG141AP-2	DG141AP/883
DG141AP/883	DG141AP/883
DG142AP-2	DG142AP/883
DG142AP/883	DG142AP/883
DG151AP-2	DG141AP/883
DG151AP/883	DG141AP/883
DG152AP-2	DG133AP/883
DG152AP/883	DG133AP/883
DG153AL-2	DG140AL/883
DG153AL/883	DG140AL/883
DG153AP-2	DG140AP/883
DG153AP/883	DG140AP/883
DG154AP-2	DG129AP/883
DG154AP/883	DG129AP/883
DG164AP-2	DG139AP/883
DG164AP/883	DG139AP/883
DG180AA-2	DG180AA/883
DG180AA/883	DG180AA/883
DG180AP-2	DG180AP/883
DG180AP/883	DG180AP/883
DG181AA-2	DG181AA/883
DG181AA/883	DG181AA/883
DG181AP-2	DG181AP/883
DG181AP/883	DG181AP/883
DG182AA-2	DG182AA/883
DG182AA/883	DG182AA/883
DG182AL-2	DG182AL/883
DG182AL/883	DG182AL/883
DG182AP-2	DG182AP/883
DG182AP/883	DG182AP/883
DG183AP-2	DG183AP/883
DG183AP/883	DG183AP/883
DG184AP-2	DG184AP/883
DG184AP/883	DG184AP/883
DG185AP-2	DG185AP/883
DG185AP/883	DG185AP/883
DG186AA-2	DG186AA/883
DG186AA/883	DG186AA/883
DG186AP-2	DG186AP/883
DG186AP/883	DG186AP/883
DG187AA-2	DG187AA/883
DG187AA/883	DG187AA/883
DG187AP-2	DG187AP/883
DG187AP/883	DG187AP/883
DG188AA-2	DG188AA/883
DG188AA/883	DG188AA/883

Industry Part #	Siliconix Part #
DG188AL-2	DG188AL/883
DG188AL/883	DG188AL/883
DG188AP-2	DG188AP/883
DG188AP/883	DG188AP/883
DG189AP/883	DG189AP/883
DG190AP-2	DG190AP/883
DG190AP/883	DG190AP/883
DG191AP-2	DG191AP/883
DG191AP/883	DG191AP/883
DG200AAA-2	DG200AAA/883
DG200AAA/883	DG200AAA/883
DG200AAK-2	DG200AAK/883
DG200AAK/883	DG200AAK/883
DG200AAP-2	DG200AAP/883
DG200AAP/883	DG200AAP/883
DG201AAK-2	DG201AAK/883
DG201AAK/883	DG201AAK/883
DG201AAZ/883	DG201AAZ/883
DG201AA/883	DG201AAK/883
DG202AK-2	DG202AK/883
DG202AK/883	DG202AK/883
DG221AK-2	DG221AK/883
DG221AK/883	DG221AK/883
DG243AK-2	DG243AK/883
DG243AK/883	DG243AK/883
DG271AK-2	DG271AK/883
DG271AK/883	DG271AK/883
DG271AZ/883	DG271AZ/883
DG281AA-2	DG181AA/883
DG281AA/883	DG181AA/883
DG281AP-2	DG181AP/883
DG281AP/883	DG181AP/883
DG284AP-2	DG184AP/883
DG284AP/83	DG184AP/883
DG287AA-2	DG187AA/883
DG287AA/883	DG187AA/883
DG287AP-2	DG187AP/883
DG287AP/883	DG187AP/883
DG290AP-2	DG190AP/883
DG290AP/883	DG190AP/883
DG300AAA-2	DG300AAA/883
DG300AAA/883	DG300AAA/883
DG300AAK-2	DG300AAK/883
DG300AAK/883	DG300AAK/883
DG301AAA-2	DG301AAA/883
DG301AAA/883	DG301AAA/883
DG301AAK-2	DG301AAK/883
DG301AAK/883	DG301AAK/883
DG302AAK-2	DG302AAK/883
DG302AAK/883	DG302AAK/883
DG303AAK-2	DG303AAK/883
DG303AAK/883	DG303AAK/883

Industry Part #	Siliconix Part #
DG303AAZ/883	DG303AAZ/883
DG304AAK-2	DG304AAK/883
DG304AAK/883	DG304AAK/883
DG306AAK-2	DG306AK/883
DG306AK/883	DG306AK/883
DG307AAK-2	DG307AAK/883
DG307AAK/883	DG307AAK/883
DG307AAZ/883	DG307AAZ/883
DG308AAK-2	DG308AAK/883
DG308AAK/883	DG308AAK/883
DG309AK-2	DG309AK/883
DG309AK/883	DG309AK/883
DG381AAK-2	DG381AAK/883
DG381AAK/883	DG381AAK/883
DG384AAK-2	DG405AK/883
DG384AAK/883	DG405AK/883
DG387AAA-2	DG387AAA/883
DG387AAA/883	DG387AAA/883
DG387AAK-2	DG387AAK/883
DG387AAK/883	DG387AAK/883
DG390AAK-2	DG403AK/883
DG390AAK/883	DG403AK/883
DG401AK/883	DG401AK/883
DG401AZ	DG401AZ/883
DG401AZ/883	DG401AZ/883
DG403AK/883	DG403AK/883
DG403AZ	DG403AZ/883
DG403AZ/883	DG403AZ/883
DG405AK/883	DG405AK/883
DG405AZ	DG405AZ/883
DG405AZ/883	DG405AZ/883
DG411AK/883	DG411AK/883
DG411AZ/883	DG411AZ/883
DG412AK/883	DG412AK/883
DG412AZ/883	DG412AZ/883
DG413AK/883	DG413AK/883
DG413AZ/883	DG413AZ/883
DG417AK/883	DG417AK/883
DG418AK/883	DG418AK/883
DG419AK/883	DG419AK/883
DG485AK/883	DG485AK/883
DG501AP-2	DG501AP/883
DG501AP/883	DG501AP/883
DG503AP-2	DG503AP/883
DG5041AK-2	DG401AK/883
DG5041AK/883	DG401AK/883
DG5042AK-2	DG403AK/883
DG5042AK/883	DG403AK/883
DG5043AK-2	DG403AK/883
DG5043AK/883	DG403AK/883
DG5045AK-2	DG405AK/883
DG5045AK/883	DG405AK/883

Class B /883 Compliant/Non-JAN (Cont'd)

Industry Part #	Siliconix Part #
DG506AAK-2	DG506AAK/883
DG506AAK/883	DG506AAK/883
DG506AAR-2	DG506AAR/883
DG506AAR/883	DG506AAR/883
DG506AAZ/883	DG506AAZ/883
DG507AAK-2	DG507AAK/883
DG507AAK/883	DG507AAK/883
DG507AAR-2	DG507AAR/883
DG507AAR/883	DG507AAR/883
DG507AAZ/883	DG507AAZ/883
DG508AAL-2	DG508AAK/883
DG508AAK/883	DG508AAK/883
DG508AAZ/883	DG508AAZ/883
DG509AAK-2	DG509AAK/883
DG509AAK/883	DG509AAK/883
DG509AAZ/883	DG509AAZ/883
DG5141AK/883	DG401AK/883
DG5143AK/883	DG403AK/883
DG5145AK/883	DG405AK/883
DG534AP/883	DG534AP/883
DG535AP/883	DG535AP/883
DG536AM/883	DG536AM/883
DG538AP/883	DG538AP/883
DG540AP/883	DG540AP/883
DG541AK/883	DG541AK/883

Industry Part #	Siliconix Part #
DG542AK/883	DG542AK/883
DG601AP/883	DG601AP/883
DG884AM/883	DG884AM/883
D139AA-2	D139AA/883
D469AP-2	D469AP/883
D469AP/883	D469AP/883
HI1-200-8	DG200AAK/883
HI1-201-8	DG201AAK/883
HI1-300-8	DG300AAK/883
HI1-302-8	DG302AAK/883
HI1-303-8	DG303AAK/883
HI1-304-8	DG304AAK/883
HI1-305-8	DG305AAK/883
HI1-306-8	DG306AAK/883
HI1-307-8	DG307AAK/883
HI1-384-8	DG405AK/883
HI1-387-8	DG387AAK/883
HI1-390-8	DG403AK/883
HI1-5041-8	DG401AK/883
HI1-5043-8	DG403AK/883
HI1-5045-8	DG405AK/883
HI1-506-8	DG506AAR/883
HI1-506L-8	DG526AK/883
HI1-507-8	DG507AAR/883
HI1-507L-8	DG527AK/883

Industry Part #	Siliconix Part #
HI1-508-8	DG508AAK/883
HI1-508L-8	DG528AK/883
HI1-509-8	DG509AAK/883
HI1-509L-8	DG529AK/883
HI2-200-8	DG200AAA/883
HI2-300-8	DG300AAA/883
HI2-301-8	DG301AAA/883
HI2-304-8	DG304AAA/883
HI2-387-8	DG387AAA/883
IH5041MJE/HR	DG401AK/883
IH5041MJE/883	DG401AK/883
IH5043MJE/HR	DG403AK/883
IH5043MJE/883	DG403AK/883
IH5045MJE/HR	DG405AK/883
IH5045MJE/883	DG405AK/883
IH5141MJE/883	DG401AK/883
IH5143MJE/883	DG403AK/883
IH5145MJE/883	DG405AK/883
L161AP-2	L161AP/883
L161AP/883	L161AP/883
SW-01BQ883	DG201AAK/883
SW-02BQ883	DG202AAK/883
SW-05BK883	DG200AAA/883
SW-05BY883	DG200AAK/883

BURN-IN CONNECTIONS

Part/Package		Pin Number																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG133	P	10 k GND	+10 V	10 k GND	-	+10 V	10 k GND	10 k GND	+10 V	GND	GND	+10 V	-20 V	GND	+10 V				
DG139 DG140	P	10 k GND	+10 V	10 k GND	-	+10 V	10 k GND	10 k GND	+10 V	GND	GND	+10 V	-20 V	GND	+10 V				
DG141	P/L	10 k GND	-10 V	10 k GND	-	+10 V	10 k GND	10 k GND	+10 V	GND	GND	+10 V	-20 V	GND	+10 V				
DG142	P	10 k GND	+10 V	10 k GND	-	+10 V	10 k GND	10 k GND	+10 V	GND	GND	+10 V	-20 V	GND	+10 V				
DG172	P	(14)	GND	GND	-	-20 V	GND	+5 V	+5 V	+5 V	+5 V	GND	+5 V	(14)	7.5 k -20 V				
DG180 DG181	A	+15 V	10 k GND	GND	+15 V	+5 V	GND	-15 V	GND	10 k GND	+15 V								
DG180 DG181	P	+15 V	10 k GND	-	-	GND	+15 V	+5 V	GND	-15 V	GND	-	-	10 k GND	+15 V				
DG182	P/L	+15 V	10 k GND	-	-	GND	+15 V	+5 V	GND	-15 V	GND	-	-	10 k GND	+15 V				
DG182 DG186	A	+15 V	10 k GND	GND	+15 V	+5 V	GND	-15 V	GND	10 k GND	+15 V								
DG183 DG184 DG185	L	-15 V	10 k GND	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V	10 k GND	10 k GND	-15 V				
DG183 DG184 DG185	P	10 k GND	-	10 k GND	-15 V	-15 V	10 k GND	-	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V		
DG186 DG187 DG188	P	-15 V	10 k GND	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V	10 k GND	10 k GND	-15 V				
DG187 DG188	A	+15 V	10 k GND	GND	+15 V	+5 V	GND	-15 V	GND	10 k GND	+15 V								
DG189 DG190 DG191	L	-15 V	10 k GND	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V	10 k GND	10 k GND	-15 V				
DG189 DG190 DG191	P	10 k GND	-	10 k GND	-15 V	-15 V	10 k GND	-	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V		

NOTES:
1. Parenthesis indicate direct connection to that pin, i.e. (2) = connect to pin 2; all voltages ±5%.
2. Package types: P = all dual-in-line packages, L = all flat packages, A = all 10-lead TO-5's, R = 28 pin dual-in-line packages.

Part/Package		Pin Number																	
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG200A	P	+15 V	-	GND	-	(10)	(10)	-15 V	-	(10)	10 k GND	-	+15 V	-	+15 V				
DG201A	P	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	-	+15 V	(15)	10 k GND	+15 V		
DG202	K	+15 V	10 k GND	10 k GND	-15 V	GND	10 k GND	10 k GND	+15 V	+15 V	10 k GND	10 k GND	N/C	+15 V	10 k GND	10 k GND	+15 V		
DG211	P	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	+5 V	+15 V	(15)	10 k GND	+15 V		
DG212	K	-15 V	10 k GND	10 k GND	-15 V	GND	10 k GND	10 k GND	-15 V	-15 V	10 k GND	10 k GND	+5 V	+15 V	10 k GND	10 k GND	-15 V		
DG221	K	+15 V	10 k GND	10 k GND	-15 V	GND	10 k GND	10 k GND	+15 V	+15 V	10 k GND	10 k GND	-15 V	+15 V	10 k GND	10 k GND	+15 V		
DG243	K	(16)	-	(16)	(16)	(16)	(16)	-	(16)	(16)	GND	+15 V	+5 V	GND	-15 V	GND	10 k GND		
DG300A DG301A DG304A DG305A	A	(9)	(9)	GND	-	GND	-15 V	GND	(9)	10 k GND	+15 V								
DG300A DG306A DG307A	P	-	(13)	(13)	(13)	(13)	GND	GND	-15 V	GND	(13)	(13)	(13)	10 k GND	+15 V				
DG301A DG302A DG303A DG304A DG305A DG306A DG307A	P/L	-	(13)	(13)	(13)	(13)	GND	GND	-15 V	GND	(13)	(13)	(13)	10 k GND	+15 V				
DG308A	P	+15 V	(15)	(15)	-15 V	GND	(15)	(15)	+15 V	+15 V	(15)	(15)	-	+15 V	(15)	10 k GND	+15 V		
DG309	P	-15 V	(15)	(15)	-15 V	GND	(15)	(15)	-15 V	-15 V	(15)	(15)	-	(15)	(15)	10 k GND	-15 V		
DG381A	A	+15 V	10 k GND	GND	+15 V	+5 V	GND	-15 V	GND	10 k GND	+15								
DG381A	P	+15 V	10 k GND	-	-	GND	+15 V	+5 V	GND	-15 V	GND	-	-	10 k GND	+15 V				
DG384A	L	-15 V	10 k GND	10 k GND	+15 V	GND	+15 V	+5 V	GND	-15 V	GND	+15 V	10 k GND	10 k GND	-15 V				

NOTES:
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2. Package types: P = all dual-in-line packages, L = all flat packages, A = all 10-lead TO-5's, R = 28 pin dual-in-line packages.

Part/Package		Pin Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
DG384A DG390A	P	10 k GND	–	10 k GND	−15 V	−15 V	10 k GND	–	10 k GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V		
DG387A	P	−15 V	10 k GND	10 k GND	+15 V	GND	+15 V	+5 V	GND	−15 V	GND	+15 V	10 k GND	10 k GND	−15 V				
DG408 DG508A	P	GND	GND	−15 V	(12)	(12)	(12)	(12)	(12)	(12)	(12)	(12)	10 k GND	+15 V	GND	GND	GND		
DG409 DG509A	P	GND	GND	−15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10 k GND	+15 V	GND	GND		
DG528	P	GND	GND	GND	−15 V	(13)	(13)	(13)	(13)	(13)	(13)	(13)	(13)	10 k GND	+15 V	GND	GND	GND	GND
DG529	P	GND	GND	GND	−15 V	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	(14)	10 k GND	+15 V	GND	GND	GND
DG5040 DG5041 DG5042 DG5043 DG5044 DG5045	P	10 k GND	–	10 k GND	10 k GND	10 k GND	19 k GND	N/C	10 k GND	10 k GND	GND	+15 V	+5 V	GND	−15 V	GND	10 k GND		
Si7661		N/C	N/C	GND	N/C	1 k −15 V	N/C	N/C	1 k 15 V										

	Pin Number 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Part/Pkg	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**
DG406 DG506A	15 V	(28)		(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	GND		GND	GND	GND	GND	GND	(28)	(28)	(28)	(28)
(R)	(28)	(28)	(28)	(28)	−15 V	10 k GND																
DG507A	15 V	10 k GND	--	(2)	(2)	(2)	(2)	(2)	(2)	(2)	(2)	GND	--	GND	GND	GND	GND	GND	(2)	(2)	(2)	(2)
(R)	(2)	(2)	(2)	(2)	−15 V	(2)																
DG526 DG527	15 V	(28)	GND	(28)	(28)	(28)	(28)	(28)	(28)	(28)	(28)	GND	GND	GND	GND	GND	GND	GND	(28)	(28)	(28)	(28)
(K)	(28)	(28)	(28)	(28)	−15 V	10 k GND																

NOTES:
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	Pin Number																					
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Part/Pkg*	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	**32**	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**
DG534 (PLCC)	GND	10 k GND	1 k 15 V	1 k 15 V	GND	1 k 15 V	GND	GND	GND	GND	GND	GND	GND		1 k 5 V	1 k 15 V	GND	1 k 15 V	1 k -5 V	10 k GND		
DG535	GND	(18)	(18)	(18)	(18)	(18)	(18)	(18)	(18)	(18)	(18)	GND	GND	GND	GND	GND	GND	10 k 15 V	(18)	10 k GND	(18)	(18)
(P)	(18)	(18)	(18)	(18)	(18)	(18)																
DG536	10 k 15 V	GND	(1)	GND	(1)	GND	(1)	(1)	GND	GND	GND	GND	GND	GND	(1)	(1)	10 k GND	GND	(1)	GND	(1)	GND
(PLCC)	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND	(1)	GND
DG538 (PLCC)	GND	10 k GND	1 k 15 V	(3)	GND	(3)	GND	(3)	GND	(3)	GND	GND	GND	GND	GND	GND	GND	GND	1 k 5 V	(3)	GND	(3)
	GND	(3)	GND	(3)	1 k -5 V	(2)																
Si8601	5 V	CLK 8kHz	5.6 k 5 V	5.6 k 5 V	5.6 k 5 V	5.6 k 5 V	22 k GND	GND	GND	GND	GND	GND	5 V	5 V	5 V	5 V	GND	5 V	GND	(7)	5 V	(7)
	GND	GND	GND	GND	GND	GND																
Si8602	15 V	CLK 15 V	5.6 k 15 V	5.6 k 15 V	5.6 k 15 V	5.6 k 15 V	(27)	GND	GND	GND	GND	GND	15 V	15 V	15 V	15 V	GND	15 V	GND	(27)	10 V	(27)
	5.6 k GND	5.6 k GND	5.6 k GND	5.6 k GND	22 k GND	GND																

NOTES:
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PROCESS OPTION FLOW CHARTS

Manufacturing Process Option Flows for Integrated Circuits

Test & Condition		U.S. Build Only If Specified	U.S. Build U.S. Test	Parts Shall Be Marked P.N./883	
Description	Method Per MIL-STD-883	Space Rated Extended Hi-Rel	Class B S/S JAN Devices	/883 Compliant Non-JAN Method 5004/5005	Industrial Standard
Traceability Wafer Lot		X	X	X	N/A
SEM		X	N/A	N/A	N/A
Internal VIS	2010	Cond. A	Cond. B	Cond. B	Ind.
DIE Shear	2019	X	N/A	N/A	N/A
Bond Strength cert/ data	2011	X	N/A	N/A	N/A
Stab Bake	1008-C	X	X	X	N/A
Temp Cycle	1010-C	X	X	X	Plastic Only
Centrifuge	2001-E	X	X	X	N/A
Pind	2020-A	X	N/A	N/A	N/A
Fine Leak	1014 A or B	X	X	X	N/A
Gross Leak	1014-C	X	X	X	Hermetic Only
1st Electrical	per spec	X	X	X	N/A
Burn-In	1015 A or C	72 hrs -A	160 hrs per S/S	160 hrs A or C	N/A
Interim Electrical Post Burn-In		Per device spec	Static 25c PDA per S/S	Static 25c PDA = 5%	N/A
Burn-In	1015 A or C	240 Dyn. (Min)	per S/S	N/A	N/A
Interim Electrical Post Burn-In	Static*	Static 25c PDA = 5%	N/A	N/A	N/A
Interim Electrical Post Burn-In	Functional*	Func. 25c PDA = 3% (datalog)	per S/S	N/A	N/A
Final Electrical	Min. Temp	X	X	X	X
Final Electrical	Max. Temp	X	X	X	N/A
Fine Leak	1014 A or B	X	N/A	N/A	N/A
Gross Leak	1014 C	X	N/A	N/A	N/A
X-Ray	2012	X	N/A	N/A	N/A
QCI A	5005	per Spec	X	X	25c
QCI B	5005	X	X	X	N/A
QCI C	5005	N/A	X	X	N/A
QCI D	5005	X	X	X	N/A
External Visual	2009	X	X	X	AQL = 0.65
Deltas		Option	X	Option	N/A
Solder Dip		Option	X	Option	X
	* = PDA applies to both burn-ins	Notice: On U.S. builds, unless otherwise specified by 38510 or dwg. parts may be assembled off shore.		Note: Parts not qualified for /883 must not be marked as such. A special flow for this product will be generated as custom.	

Process Option Flows for IC Chip/Wafer

Standard Die/Chip, and Chip Samples with Element Evaluation		
Die ship element evaluation non compliant/non JAN subgroup 1 & 3 performed in-line screen	Die ship No canned sample	Die Wafer form
Wafer probe Static 25c (min) per device spec Internal visual method 2010 cond. B	Wafer probe Static 25c (min) per device spec Internal visual method 2010 cond. B	Wafer probe Static 25c (min) per device spec Internal visual method 2010 cond. B
Canned samples: Method 2008 MILI std 883 class B device Subgroup 1 (ss-10/0) Internal visual method 2010 cond. B Subgroup 2 (ss-10/1) Final electrical static @25c min/max oper. temp. (per deivce spec) Subgroup 3 (5 Die min) (s/s = 10/0 or 20/1 wires) NDT Method 2023 wire bond eval. Method 2011 (cert & data) *sem available	Die prep process	

ANALOG SWITCH SELECTOR CHART

$r_{DS(ON)}$ – Drain-to-Source On-Resistance	Switching Speed t_{ON} or t_{OFF}, Whichever is Greater							
	20/35 to 60/75 ns	125/150 ns	200 ns	250 ns	300 ns	500/600 ns	750 ns	1 µS
175 Ω						DG201A-*C,Q,SS* DG202-*C,Q,SS*		DG211-*C,Q,SS* DG212-*C,Q,SS*
100 Ω		DG441-*C,Q,SS* DG442-*C,Q,SS* DG444-*C,Q,SS* DG445-*C,Q,SS*	DG308A-*C,Q,SS* DG309-*C,Q,SS* DG485-*C,8,CD*			DG221-*C,Q,SS,L*		
80 Ω	DG540-*D,Q,SS* DG541-*D,Q,SS* DG542-*D,Q,SS*			DG182-*J,D,SS* DG185-*J,D,DS* DG188-*J,S,SD* DG191-*J,D,SD*				DG200A-*C,D,SS*
50 Ω	DG271-*C,Q,SS*			DG304A-*C,D,SS* DG305A-*C,S,SD* DG306A-*C,D,DS* DG307A-*C,D,SD*	DG300A-*C,D,SS* DG301A-*C,S,SD* DG302A-*C,D,DS* DG303A-*C,D,SD* DG381A-*C,D,SS* DG384A-*C,D,DS* DG387A-*C,S,SD* DG390A-*C,D,SD*			DG243-*C,D,SD,M*
30 Ω to 25 Ω	DG601-*L,Q,SS*	DG181-*J,D,SS* DG184-*J,D,DS* DG187-*J,S,SD* DG190-*J,D,SD* DG401-*C,D,SS* DG403-*C,D,SD* DG405-*C,D,DS* DG411-*C,Q,SS* DG412-*C,Q,SS* DG413-*C,Q,SS* DG417-*C,S,SS* DG418-*C,S,SS* DG419-*C,SD,S* DG421-*C,D,SS,L* DG423-*C,D,SD,L* DG425-*C,D,DS,L*							
10 Ω					DG180-*J,D,SS* DG183-*J,D,DS* DG186-*J,S,SD* DG189-*J,D,SD*			

Information

C Q SS L
- *L* — Miscellaneous
- *SS* — Configuration
- *Q* — Number per Package
- *C* — Process

Process
- *C* = Plus-40 CMOS or 44 V SI-Gate
- *D* = DMOS or D/CMOS
- *J* = JFET
- *P* = PMOS
- *L* = Low Voltage CMOS (PolyMOS)

Number per Package
- *S* = Single (1 per package)
- *D* = Dual (2 per package)
- *Q* = Quad (4 per package)
- *8* = Eight per package

Configuration
- *SS* = Single–Pole Single-Throw
- *SD* = Single-Pole Double-Throw
- *DS* = Double-Pole Single-Throw
- *DD* = Double-Pole Double-Throw
- *CD* = Common Drain

Miscellaneous
- *r* = $r_{DS(ON)}$ is a function of drive voltage
- *M* = Make-Before-Break
- *L* = Latchable Inputs

ANALOG SWITCHES

Functional Configuration	Basic Part Number	Switch Type	$r_{DS(ON)}$ MAX[2] (Ω)	$I_{S(OFF)}$ MAX[2] (nA)	Supply Voltage V+	Supply Voltage V-	Supply Voltage V_L[3]	Voltage Range[2]	Switching Time (nS MAX) t_{ON}	Switching Time (nS MAX) t_{OFF}	MAX Supply Range	Analog Voltage Range (V)	Levels V_{INL}	Levels V_{INH}	Comments	Notes	Package and Temperature Offerings: Plastic DIP	Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can
1 Ch. SPST	DG417	44V SiGate	35	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Mini DIP, Low Power	3	DJ	DY	AK				
	DG418	44V SiGate	35	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Mini DIP, Low Power	3	DJ	DY	AK				
2 Ch. SPST	DG401	44V SiGate	35	0.25	15	−15	5	30	150	100	44	V+ to V−	0.8	2.4	Low Power, High Perf.	3	DJ		AK				
	DG421	44V SiGate	35	0.25	15	−15	5	30	250	200	44	V+ to V−	0.8	2.4	Low Power, Wide Dyn. Range	3	DJ		AK				
	DG181	N-JFET	30	1.00	10	−20	5	20	150	130	36	(V+) to (V−) +7.5	0.8	2.0	Use DG401 for New Designs	3			AK				AA,BA
	DG181	N-JFET	30	1.00	15	−15	5	15	150	130			0.8	2.0	Use DG401 for New Designs	3				AP,BP		AL	AA,BA
	DG182	N-JFET	75	1.00	10	−20	5	20	250	130	36	(V+) to (V−) +5	0.8	2.0	Use DG401 for New Designs	1,3				AP,BP		AL	AA,BA
	DG182	N-JFET	75	1.00	15	−15	5	20	250	130			0.8	2.0	Use DG401 for New Designs	1,3				AP,BP		AL	AA,BA
	DG300A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	JAN Qualified		CJ		AK,BK	AP,BP			AA,BA
	DG304A	CMOS + 40	50	1.00	15	−15		30	250	150	44	V+ to V−	3.5	11.0	JAN Qualified		CJ		AK				
	DG381A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	Use DG401 for New Designs		CJ		AK,BK,				
	DG200A	CMOS + 40	70	2.00	15	−15		30	1000	500	44	V+ to V−	0.8	2.4	JAN Qualified		CJ		AK,BK,				AA,BA
	DG180	N-JFET	10	10.00	10	−18		20	300	250	36	(V+) to (V−) +7.5	0.8	2.5	Use DG401 for New Designs	1,3						AL	AA,BA
	DG180	N-JFET	10	10.00	15	−15	5	15	300	250			0.8	2.0	Use DG401 for New Designs	1,3				AP,BP		AL	AA,BA
4 Ch. SPST	DG411	44V SiGate	35	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Low Power, High Perf.	3	DJ	DY	AK				
	DG412	44V SiGate	35	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Low Power, High Perf.	3	DJ	DY	AK				
	DG413	44V SiGate	35	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Low Power, High Perf.	3	DJ	DY	AK				
	DG441	44V SiGate	85	0.50	15	−15		30	250	120	44	V+ to V−	0.8	2.4	DG201A Upgrade		DJ	DY	AK				
	DG442	44V SiGate	85	0.50	15	−15		30	250	170	44	V+ to V−	0.8	2.4	DG202 Upgrade		DJ	DY	AK				
	DG444	44V SiGate	85	0.50	15	−15	5	30	250	120	44	V+ to V−	0.8	2.4	DG211 Upgrade	3	DJ	DY					
	DG445	44V SiGate	85	0.50	15	−15	5	30	250	170	44	V+ to V−	0.8	2.4	DG212 Upgrade	3	DJ	DY					
	DG201A	CMOS + 40	175	1.00	15	−15		30	600	450	44	V+ to V−	0.8	2.4	JAN Qualified		CJ	DY	AK,BK,CK				
	DG202	CMOS + 40	175	1.00	15	−15		30	600	450	44	V+ to V−	0.8	2.4	JAN Qualified		CJ		AK				
	DG221	CMOS + 40	100	1.00	15	−15		30	550	340	44	V+ to V−	0.8	2.4	Latchable Inputs		CJ	DY	AK,BK,CK				
	DG271	44V SiGate	50	1.00	15	−15		30	60	60	44	V+ to V−	0.8	2.0	High Speed, Low Charge Inj.		CJ	DY	AK				
	DG308A	CMOS + 40	100	1.00	15	−15		30	200	150	44	V+ to V−	3.5	11.0	Single Supply		CJ	DY	AK,BK,CK				
	DG309	CMOS + 40	100	1.00	15	−15		30	200	150	44	V+ to V−	3.5	11.0	Single Supply		CJ	DY	AK				
	DG601	22 V SiGate	35	4.00	12	0		12	45	30	22	12 to 0	0.8	2.0	Very High Speed	4	DJ	DY	AK	AP			
	DG211	CMOS + 40	175	5.00	15	−15	5	30	1000	500	44	V+ to V−	0.8	2.4	Low Cost	3	CJ	DY					
	DG212	CMOS + 40	175	5.00	15	−15	5	30	1000	500	44	V+ to V−	0.8	2.4	Low Cost	3	CJ	DY					
	DG540	D/CMOS	60	10.00	12	−3		10	90	50	18	(V+) −5 to V−	0.8	2.4	Wideband Video		DJ	DN		AP			
	DG541	D/CMOS	60	10.00	12	−3		10	90	50	18	(V+) −5 to V−	0.8	2.4	Wideband Video		DJ	DY		AP			
1 Ch. SPDT	DG419	44V SiGate	25	0.25	15	−15	5	30	175	145	44	V+ to V−	0.8	2.4	Mini DIP, Low Power	3	DJ	DY	AK				
	DG187	N-JFET	30	1.00	10	−20	5	20	150	130	36	(V+) to (V−) +7.5	0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA
	DG187	N-JFET	30	1.00	15	−15	5	15	150	130			0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA
	DG188	N-JFET	75	1.00	15	−15	5	20	250	130			0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA
	DG188	N-JFET	75	1.00	10	−20	5	20	250	130	36	(V+) to (V−) +5	0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA
	DG301A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	JAN Qualified		CJ		AK,BK				AA,BA
	DG305A	CMOS + 40	50	1.00	15	−15		30	250	150	44	V+ to V−	3.5	11.0	JAN Qualified								AA
	DG387A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	Use DG403/419 for New Des.		CJ		AK				AA
	DG186	N-JFET	10	10.00	15	−15	5	15	300	250			0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA
	DG186	N-JFET	10	10.00	10	−20	5	20	300	250	35	(V+) to (V−) +7	0.8	2.0	Use DG403/419 for New Des.	1,3				AP,BP		AL	AA,BA

Notes:
1. XXXX Not recommended for new designs.
2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch $r_{DS(ON)}$ is also a function of supply and analog voltage. See 1990 data book for more details.
3. Logic supply voltage required for TTL compatible inputs.
4. Preliminary product. Specifications subject to change. Contact the factory for availability.
5. Input reference voltage of 2.5 V is required. See 1990 data book for more details.

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ANALOG SWITCHES (Cont'd)

Functional Configuration	Basic Part Number	Switch Type	$r_{DS(ON)}$ MAX[2] (Ω)	$I_{S(OFF)}$ MAX[2] (nA)	Supply Voltage V+	Supply Voltage V−	Supply Voltage V_L[3]	Voltage Range[2]	Switching Time (nS MAX) t_{ON}	Switching Time (nS MAX) t_{OFF}	MAX Supply Range	Analog Voltage Range (V)	Levels V_{INL}	Levels V_{INH}	Comments	Notes	Package and Temperature Offerings: Plastic DIP	Plastic SO	CerDIP	Side Braze	LCC	Flat Pack	Metal Can
2 Ch. SPDT	DG403	44V SIGate	35	0.25	15	−15	5	30	150	100	44	V+ to V−	0.8	2.4	Low Power, High Perf.	3	DJ	DY	AK				
	DG423	44V SIGate	35	0.25	15	−15	5	30	250	200	44	V+ to V−	0.8	2.4	Low Power, Wide Dyn. Range	3	DJ	DN	AK				
	DG190	N-JFET	30	1.00	15	−15	5	15	150	130			0.8	2.0	Use DG403 for New Designs	1,3				AP,BP		AL	
	DG190	N-JFET	30	1.00	10	−20	5	20	150	130	36	(V+) to (V−) +7.5	0.8	2.0	Use DG403 for New Designs	1,3				AP,BP		AL	
	DG191	N-JFET	75	1.00	10	−20	5	20	250	130	36	(V+) to (V−) +5	0.8	2.0	Use DG403 for New Designs	3				AP,BP		AL	
	DG191	N-JFET	75	1.00	15	−15	5	20	250	130			0.8	2.0	Use DG403 for New Designs	3				AP,BP		AL	
	DG243	CMOS + 40	50	1.00	15	−15	5	30	1000	500	44	V+ to V−	0.8	2.0	Use DG403 for New Designs	3	CJ		AK,CK				
	DG303A	CMOS + 40	50	1.00	15	−15	5	30	300	250	44	V+ to V−	0.8	4.0	JAN Qualified		CJ		AK,BK				
	DG307A	CMOS + 40	50	1.00	15	−15		30	250	150	44	V+ to V−	3.5	11.0	JAN Qualified		CJ		AK,BK				
	DG390A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	Use DG403 for New Designs		CJ		AK,BK,CK				
	DG5043	CMOS + 40	50	1.00	15	−15		30	1000	500	44	V+ to V−	0.8	2.4	Use DG403 for New Designs	1,3	CJ						
	DG189	N-JFET	10	10.00	10	−20	5	20	300	250	36	(V+) to (V−) +7.5	0.8	2.0	Use DG403 for New Designs	3				AP,BP		AL	
	DG189	N-JFET	10	10.00	15	−15	5	15	300	250			0.8	2.0	Use DG403 for New Designs	3				AP,BP		AL	
	DG542	D/CMOS	60	10.00	12	−3	5	10	90	50	18	(V+) −5 to V−	0.8	2.4	Wideband Video		DY	DY		AP			
1 Ch. DPST	DG185	N-JFET	75	1.00	15	−15	5	20	250	130			0.8	2.0	Use DG405 for New Designs	1,3				AP,BP		AL	
	DG185	N-JFET	75	1.00	10	−20	5	20	250	130	36	(V+) to (V−) +5	0.8	2.0	Use DG405 for New Designs	1,3				AP,BP		AL	
	DG302A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to V−	0.8	4.0	JAN Qualified		CJ		AK,BK,CK				
	DG306A	CMOS + 40	50	1.00	15	−15		30	250	150	44	V+ to V−	3.5	11.0	JAN Qualified		CJ		AK,BK,CK				
	DG384A	CMOS + 40	50	1.00	15	−15		30	300	250	44	V+ to	0.8	4.0	Use DG405 for New Designs	1	CJ		AK,BK,CK				
	DG183	N-JFET	10	10.00	15	−15	5	15	300	250			0.8	2.0	Use DG405 for New Designs	1,3				AP,BP		AL	
	DG183	N-JFET	10	10.00	10	−20		20	300	250	36	(V+) to (V−) +8	0.8	2.0	Use DG405 for New Designs	1,3				AP,BP		AL	
2 Ch. DPST	DG405	44 V SIGate	35	0.25	15	−15		30	150	100	44	V+ to V−	0.8	2.4	Low Power, High Perf.		DJ	DY	AK				
	DG425	44 V SIGate	25	0.25	15	−15	5	30	250	200	44	V+ to V−	0.8	2.4	On Board Latches	3	DJ		AK				
	DG184	N-JFET	30	1.00	10	−20	5	20	150	130	36	(V+) to (V−) +7.5	0.8	2.0	Use DG405 for New Designs	3				AP,BP		AL	
	DG184	N-JFET	30	1.00	15	−15	5	15	150	130			0.8	2.0	Use DG405 for New Designs	3				AP,BP		AL	
	DG425	44 V SIGate	35	0.25	15	−15	5	30	250	200	44	V+ to V−	0.8	2.4	Low Power with Latch	3				AK			
															Wide Dynamic Range		DJ						

Notes:
1. XXXX Not recommended for new designs.
2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch $r_{DS(ON)}$ is also a function of supply and analog voltage. See 1990 data book for more details.
3. Logic supply voltage required for TTL compatible inputs.
4. Preliminary product. Specifications subject to change. Contact the factory for availability.
5. Input reference voltage of 2.5 V is required. See 1990 data book for more details.
6. See data book for switch states of differential and multiple switches.

LINEARS

Functional Configuration	Basic Part Number	Technology	Open Loop Gain (dB)	MIN Supply Voltage (V)	MAX Supply Voltage (V)	Input Offset Voltage (mV) MAX	TC Input Offset (µV/°C)	Comments	Package and Temperature Ranges[1] Plastic DIP	Side Braze	CerDIP	Metal Can
450 MHz Video Buffer	SI581	Comp. Bipolar		± 3.	± 7	8	3	Unity Gain	DJ,DY			
180 MHz Video Buffer/Amp	SI582	Comp. Bipolar		± 3.	± 7	5.5	40	± 1 ≤ Gain ≤ ± 8	DJ,DY			
Quad Buffer	SI584	Comp. Bipolar		± 3.	± 7			Unity Gain	DJ,DY			

Notes: 1. Available in Comercial, Industrial, and Military versions.

VOLTAGE CONVERTERS

Functional Configuration	Basic Part Number	Technology	MAX Input Current (mA)	MIN Supply Voltage (V)	MAX Supply Voltage (V)	MIN Output Voltage (V)	MAX Output Voltage (V)	Comments	Package and Temperature Ranges		
									Plastic DIP	Metal Can	SO
Voltage Doubler/Inverter	SI7660	CMOS	0.5	1.5	10	-10	20.0		CJ		
Voltage Doubler/Inverter	SI7661	CMOS	2.0	60.0	20	-20.0	40.0	Increased Voltage Range	CJ		

ANALOG MULTIPLEXERS

Function	Basic Part Number	Input Latches	$r_{DS(ON)}$ MAX[2] (Ω)	$I_{D(OFF)}$ (nA)	Analog Range[2] (V)	Transition Time (µs)	Logic Levels (V)		Supply Voltages (V)			Comments	Packages and Temperature Ranges						
							V_{INL}	V_{INH}	V+	V-	V_L		Plastic DIP	CerDIP	Side Braze	Hermetic Quad/LCC	Quad PLCC	Flat Pack	SO
8-Channel Serial Input Switch Array	DG485	Yes	85	1	±15	0.2	0.8	2.4	15	-15	5	Serial Address	DJ	AK			DN		
8-Channel MUX + Enable	DG408	No	100	1	±15	0.2	0.8	2.4	15	-15		High Performance	DJ	AK					DY
8-Ch. Single/Four Ch. Diff. MUX	DG538	Yes	90	10	-5 to +10	0.2	0.8	2.4	15	-5		Wideband/Video	DJ		AP	AZ	DN		
8-Channel MUX + Enable	DG508A	No	400	10	±15	1.0	0.8	2.4	15	-15			CJ	AK,BK,CK					DY
8-Channel MUX + Enable	DG528	Yes	400	10	±15	1.0	0.8	2.4	15	-15		Latches on Board	CJ	AK,BK,CK			DN		
16 Channel MUX + Enable	DG536	Yes	90	10	0 to 10	0.3	4.5	10.5	15	15		Wideband/Video				AM	DN		
16 Channel MUX + Enable	DG535	Yes	90	10	0 to 10	0.3	4.5	10.5	15	15		Wideband/Video	DJ		AP				
16 Channel MUX + Enable	DG506A	No	400	10	±15	1.0	0.8	2.4	15	15			CJ	AK,BK,CK	BR		DN		
4 Channel Dual MUX	DG409	No	100	1	±15	0.2	0.8	2.4	15	15		High Performance	DJ	AK					DY
8 Ch. Single/Four Ch. Diff. MUX	DG538	Yes	90	10	-5 to +10	0.3	0.8	2.4	15	15		Wideband/Video	DJ		AP		DN		
4 Ch. Single/Two Ch. Diff. MUX	DG534	Yes	90	10	-5 to +10	0.3	0.8	2.4	15	15		Wideband/Video	DJ		AP		DN		
4 Channel Dual MUX	DG529	Yes	400	10	±15	1.0	0.8	2.4	15	15		Latches on Board	CJ	AK,BK					
4 Channel Dual MUX	DG509A	No	400	10	±15	1.0	0.8	2.4	15	15		Precision	CJ	AK,BK,CK					DY
8 Channel Dual Mux + Enable	DG507A	No	400	5	±15	1.0	0.8	2.4	15	15			CJ	AK,BK,CK	BR				
Specials																			
8 x 4 Crosspoint Array	DG884	Yes	90	20	-5 to +8	0.3	0.8	2.0	15	-5	5	Wideband/Video				AM	DN		
RGB Switch	DG894	Yes	100	10	±2	0.2	1.5	3.0	12	-5		I²C or dc Control	DJ						

Notes: 1. XXXX Not recommended for new designs.
2. For most products, the analog voltage range is a function of supply voltages. For PMOS or CMOS switch $r_{DS(ON)}$ is also a function of supply and analog voltage. See 1989 data book for more details.

Cross Reference

Siliconix Part Number

Suggestions are based on the similarity of mechanical and electrical characteristics, as reported in the manufacturer's published data. Interchangeability is not guaranteed. Before selecting a device as a substitute, compare the specifications.

Siliconix Approximate Replacement

Suggestions are based on the similarity of electrical characteristics, as reported in the manufacturer's published data. Interchangeablity is not guaranteed, as these parts may have different pin configurations. Before selecting a device as a substitute, compare the specifications. For devices not shown in this guide, or for additional information, the user should contact the nearest Siliconix sales office.

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
ADG200AA		DG200AAA
ADG200AA/883		DG200AAA/883
ADG200AP		DG200AAP
ADG200AP/883		DG200AAP/883
ADG200BA		DG200ABA
ADG200BP		DG200ABP
ADG200CJ		DG200ACJ
ADG201ABQ	DG441AK	
ADG201AKN	DG441DJ	
ADG201AP	DG441AK	
ADG201AP/883	DG441AK/883	
ADG201ATQ	DG441AK	
ADG201ATQ/883	DG441AK/883	
ADG201BP	DG441AK	
ADG201CJ	DG441DJ	
ADG201HS		DG271
ADG202ABQ	DG442AK	
ADG202AKN	DG442DJ	
ADG202ATQ	DG442	
ADG211	DG444	
ADG212A	DG445	
ADG221	DG221	
ADG222	DG222	
ADG506A	DG406	
ADG507A	DG407	
ADG508A	DG408	
ADG509A	DG409	
ADG526A	DG526	
ADG528A	DG528	
ADG529A	DG529	
AD200DIAA		DG200AAA
AD200DIAP		DG200AAK
AD200DIBA		DG200ABA
AD200DICJ		DG200ACJ
AD200DIPB		DG200ABK
AD201DIAP		DG411AK
AD201DIBP		DG411AK
AD201DICJ		DG411DJ
AD302DIAP	DG302AAK	
AD302DIBP	DG302AAK	
AD302DICJ	DG302CJ	
AD303DIAP	DG303AAK	
AD303DIBP	DG303AAK	
AD303DICJ	DG303ACJ	
AD7501JD		DG501BK
AD7501JN		DG501CJ
AD7501KD		DG501BK
AD7501KN		DG501CJ
AD7503JD		DG503BK
AD7501SD		DG501AK
AD7503JN		DG503CJ
AD7503KD		DG503BK
AD7503KN		DG503CJ
AD7503SD		DG503AK
AD7506JD	DG506AAR/883	
AD7506JD/883	DG506AAR/883	
AD7506JN	DG506ACJ	
AD7506KD	DG506AAR/883	
AD7506KN	DG506ACJ	
AD7506SD	DG506AAR/883	
AD7506TD	DG506AAR/883	
AD7507JD	DG507AAR/883	
AD7507JD/883	DG507AAR/883	
AD7507JN	DG507ACJ	
AD7507KD	DG507AAR/883	
AD7507KN	DG507ACJ	
AD7507SD	DG507AAR/883	
AD7507TD	DG507AAR/883	
AD7508KD		DG508ABK
AD7508KN		DG508ACJ
AD7508SD		DG508AAK
AD7509KD		DG509ABK
AD7509KN		DG509ACJ
AD7509SD		DG509AAK
AH0126CD	DG129BP	
AH0126D	DG129AP/883	
AH0126D/883	DG129AP/883	
AH0129CD	DG129BP	
AH0129D	DG129AP/883	
AH0129D/883	DG129AP/883	
AH0133CD	DG141BP	
AH0133D	DG141AP/883	
AH0133D/883	DG141AP/883	
AH0134CD	DG141BP	
AH0134D	DG141AP/883	
AH0134D/883	DG141AP/883	
AH0139CD	DG139AP/883	
AH0139D	DG139AP/883	
AH0139D/883	DG139AP/883	
AH0140CD	DG140AP/883	
AH0140D	DG140AP/883	
AH0140D/883	DG140AP/883	
AH0141CD	DG141AP/883	
AH0141D	DG141AP/883	
AH0141D/883	DG141AP/883	
AH0142CD	DG142AP/883	

Cross Reference

Siliconix incorporated

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
AH0142D	DG142AP/883	
AH0143D/883	DG141AP/883	
AH0146CD	DG141AP/883	
AH0151CD	DG141AP/883	
AH0151D	DG141AP/883	
AH0151D/883	DG141AP/883	
AH0152CD	DG141BP	
AH0152D	DG141AP/883	
AH0152D/883	DG141AP/883	
AH0153CD	DG140AP/883	
AH0153D	DG140AP/883	
AH0153D/883	DG140AP/883	
AH0154CD	DG129BP	
AH0154D	DG129AP/883	
AH0154D/883	DG129AP/883	
AH0164CD	DG139AP/883	
AH0164D	DG139AP/883	
AH0164D/883	DG139AP/883	
AM3705CD	DG501BP	
AM3705D	DG501AP	
CDG201AK		DG541AP
CDG201BJ		DG541AP
CDG201BK		DG541AP
CDG211CJ		DG541AP
CDG308AK		DG541AP
CDG308BJ		DG541DJ
CDG308BK		DG541AP
CDG308CJ		DG541DJ
CDG4308BJ		DG540AP
D469AP	D469AAK	
D469AP-2	D469AAK/883	
D469AP/883	D469AAK/883	
D469BP	D469AAK	
D469CJ	D469ADJ	
DG129AK	DG129AP/883	
DG129AK/HR	DG129AP/883	
DG129AK/883B	DG129AP/883	
DG129AP	DG129AP/883	
DG129AP-2	DG129AP/883	
DG129BK	DG129BP	
DG133AK	DG133AP/883	
DG133AK/HR	DG133AP/883	
DG133AK/883B	DG133AP/883	
DG133AP	DG141AP/883	
DG133AP-2	DG141AP/883	
DG134AK	DG141AP/883	
DG134AK/HR	DG141AP/883	
DG134AK/883B	DG141AP/883	
DG134AP	DG141AP/883	
DG134AP-2	DG141AP/883	
DG139AK	DG141AP/883	
DG139AK/HR	DG139AP/883	
DG139AK/883B	DG139AP/883	
DG139AP	DG139AP/883	
DG139AP-2	DG139AP/883	
DG139BK		DG139AP/883
DG139BP	DG139AP/883	
DG140AP	DG140AP/883	
DG140AP-2	DG140AP/883	
DG535CY	DG535DY	
DG140AP/HR	DG140AP/883	
DG140BP	DG140AP/883	
DG200AAP/883	DG200AAK/883	
DG200ABP	DG200ABK	
DG200AK	DG200AAK	
DG200AP	DG200AAK	
DG200AP/883	DG200AAK/883	
DG200BA	DG200ABA	
DG200BK	DG200ABK	
DG200BP	DG200ABK	
DG200CA	DG200ACA	
DG200CJ	DG200ACJ	
DG201AAK-2	DG201AAK/883	
DG201ACSE	DG201ADY	
DG201ACY	DG201ADY	
DG201AK	DG201AAK	
DG201AK/883	DG201AAK/883	
DG201BK	DG201ABK	
DG201CJ	DG201ACJ	
DG202AK-2	DG202AK/883	
DG202BK	DG202AK	
DG202BSE	DG202DY	
DG202CJ	DG202DJ	
DG202CK	DG202AK	
DG211CSE	DG211DY	
DG211CY	DG444DY	
DG211DY	DG444DY	
DG212CJ	DG445DJ	
DG212CSE	DG445DY	
DG212CY	DG445DY	
DG212DY	DG445DY	
DG221AK	DG221AK/883	
DG221AK-2	DG221AK/883	
DG221CK	DG221BK	
DG221CY	DG221DY	
DG243AK	DG243AK/883	
DG243AK-2	DG243AK/883	
DG271AK	DG271AK/883	
DG271AK-2	DG271AK/883	
DG271BK	DG271AK/883	
DG271CK	DG271AK/883	
DG281AA/883	DG181AA/883	
DG281AP/883	DG181AP/883	
DG284AP/883	DG184AP/883	
DG287AP/883	DG187AP/883	
DG290AP/883	DG190AP/883	
DG300AA	DG300AAA/883	
DG300AAA	DG300AAA/883	
DG300AAA-2	DG300AAA/883	
DG300AAK-2	DG300AAK/883	
DG300ACA	DG300ABA	
DG300ACJ	DG300ABK	
DG300ACK	DG300ABK	
DG300AK	DG300AAK	
DG300BA	DG300ABA	
DG300BK	DG300ABK	
DG300CJ	DG300ABK	
DG300CK	DG300ABK	
DG301AA	DG301AAA	
DG301AAA-2	DG301AAA/883	
DG301AAK-2	DG301AAK/883	
DG301ACA	DG301ABA	
DG301ACK	DG301ABK	
DG301AK	DG301AAK	
DG301BA	DG301ABA	
DG301BK	DG301ABK	
DG301CJ	DG301ACJ	
DG301CK	DG301ABK	
DG302AAK-2	DG302AAK/883	
DG302ABK	DG302AAK	
DG302ACK	DG302AAK	
DG302AK	DG302AAK	

Cross Reference

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
DG302BK	DG302AAK	
DG302CJ	DG302ACJ	
DG302CK	DG302AAK	
DG303AAK-2	DG303AAK/883	
DG303ACK	DG303AAK	
DG303AK	DG303AAK	
DG303BK	DG303AAK	
DG303CJ	DG303ACJ	
DG303CK	DG303AAK	
DG304AAA-2	DG304AAA/883	
DG304AAK	DG304AAK/883	
DG304AAK-2	DG304AAK/883	
DG304ABA	DG304CJ	
DG304ACK	DG304AAK	
DG304AK	DG304AAK/883	
DG304BK	DG304AAK/883	
DG304CJ	DG304ACJ	
DG304CK	DG304AAK	
DG305AA	DG305AAA	
DG305AAA-2	DG305AAA/883	
DG305AAK-2	DG305AAK/883	
DG305ABA	DG305AAA	
DG305ACA	DG305AAA	
DG306AAK	DG306AAK/883	
DG306ABK	DG306AAK/883	
DG306ACJ	DG306AAK/883	
DG306ACK	DG306AAK/883	
DG306AK	DG306AAK/883	
DG306BK	DG306AAK/883	
DG306CJ	DG306ACJ	
DG306CK	DG306AAK/883	
DG307AAK-2	DG307AAK/883	
DG307ACK	DG307ABK	
DG307AK	DG307AAK	
DG307BK	DG307ABK	
DG307CJ	DG307AAK	
DG307CK	DG307ABK	
DG308AAK-2	DG308AAK/883	
DG308ACK	DG308ABK	
DG309AK	DG309AK/883	
DG309AK-2	DG309AK/883	
DG309CK	DG309AK/883	
DG381AAK	DG381AAK/883	
DG381AAK-2	DG381AAK/883	
DG381ACK	DG381ABK	
DG381AK	DG381AAK/883	
DG381BA	DG381ABA	
DG381BK	DG381AAK/883	
DG381CA	DG381ABA	
DG381CJ	DG381ACJ	
DG381CK	DG381AAK/883	
DG384AAK/883	DG405AK/883	
DG387AA	DG387AAA/883	
DG387AAA	DG387AAA/883	
DG387AAA-2	DG387AAA/883	
DG387AAK	DG387AAK/883	
DG387AAK-2	DG387AAK/883	
DG387ABA	DG387AAA/883	
DG387ABK	DG387AAK/883	
DG387ACA	DG387AAA/883	
DG387ACK	DG387AAK/883	
DG387AK	DG387AAK/883	
DG387BA	DG387AAA/883	
DG387BK	DG387AAK/883	
DG387CA	DG387AAA/883	
DG387CJ	DG387ACJ	
DG387CK	DG387AAK/883	
DG390AAK/883	DG403AK/883	
DG401CJ	DG401DJ	
DG403CJ	DG403DJ	
DG403CK	DG403AK	
DG405CJ	DG405DJ	
DG405CK	DG405AK	
DG501AK	DG501AP	
DG501AP-2	DG501AP/883	
DG501BK	DG501AP	
DG501BP	DG501AP	
DG501DK	DG501AP	
DG503AK	DG503AP/883	
DG503AP	DG503AP/883	
DG503AP-2	DG503AP/883	
DG503BP	DG503AP/883	
DG5041AK	DG401AK	
DG5041AK-2	DG401AK/883	
DG5041AK/883	DG401AK/883	
DG5041CJ	DG401DJ	
DG5041CK	DG401AK	
DG5043AK	DG403AK	
DG5043AK-2	DG403AK/883	
DG5043AK/883	DG403AK/883	
DG5043CJ	DG403DJ	
DG5043CK	DG403AK	
DG5045AK	DG405AK	
DG5045AK-2	DG405AK/883	
DG5045AK/883	DG405AK/883	
DG5045CJ	DG405DJ	
DG5045CK	DG405AK	
DG506AAK-2	DG506AAK/883	
DG506AAR-2	DG506AAR/883	
DG506ACR	DG506ABR	
DG507AAK-2	DG507AAR/883	
DG507AAR	DG507AAR/883	
DG507AAR-2	DG507AAR/883	
DG507ACK	DG507ABK	
DG507ACR	DG507ABR	
DG508AAK-2	DG508AAK/883	
DG509AAK-2	DG509AAK/883	
DG5141AK	DG401AK	
DG5141AK/883	DG401AK/883	
DG5141CJ	DG401DJ	
DG5141CK	DG401DJ	
DG5143AK/883	DG403AK/883	
DG5143AKE	DG403AK	
DG5143CJ	DG403DJ	
DG5143CK	DG403AK	
DG5145AK	DG405AK	
DG5145AK/883	DG405AK/883	
DG5145CJ	DG405DJ	
DG5145CK	DG405AK	
DG526AK	DG526AK/883	
DG526BK	DG526AK/883	
DG526CJ	DG526AK/883	
DG526CK	DG526AK/883	
DG527BK	DG527AK/883	
DG527CK	DG527AK/883	
DGM181AA		DG381AAA
DGM181AA/HR		DG381AAA/883
DGM181AA/883B		DG381AAA/883
DGM181AK		DG381AAK
DGM181AK/HR		DG381AAK

Cross Reference

Siliconix incorporated

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
DGM181AK/883B		DG381AAK/883
DGM181BA		DG381ABA
DGM181BK		DG381ABK
DGM181CJ		DG381ACJ
DGM182AA		DG381AAA
DGM182AA/HR		DG381AAA/883
DGM182AA/883B		DG381AAA/883
DGM182AK		DG381AAK
DGM182AK/HR		DG381AAK
DGM182AL		DG381AAL
DGM182AL/HR		DG381AAL/883
DGM182AL/883B		DG381AAL/883
DGM182BA		DG381ABA
DGM182BK		DG381ABK
DGM182CJ		DG381ACJ
DGM184AK	DG405AK	
DGM184AK/HR	DG405AK/883	
DGM184AK/883B	DG405AK/883	
DGM184AL		DG184AL
DGM184AL/HR		DG184AL/883
DGM184AL/883B		DG184AL/883
DGM184BK	DG405AK	
DGM184CJ	DG405DJ	
DGM185AK	DG405AK	
DGM185AK/HR	DG405AK/883	
DGM185AK/883B	DG405AK/883	
DGM185AL		DG185AL
DGM185AL/HR		DG185AL/883
DGM185AL/883B		DG185AL/883
DGM185BK	DG405AK	
DGM185CJ	DG405DJ	
DGM187AA		DG387AAA
DGM187AA/HR		DG387AAA/883
DGM187AA/883B		DG387AAA/883
DGM187AK		DG387AAK
DGM187AK/HR		DG387AAK
DGM187AK/883B		DG387AAK/883
DGM187BA		DG387ABA
DGM187BK		DG387ABK
DGM187CJ		DG387ACJ
DGM188AA		DG387AAA
DGM188AA/HR		DG387AAA/883
DGM188AA/883B		DG387AAA/883
DGM188AK		DG387AAK
DGM188AK/HR		DG387AAK
DGM188AL		DG387AAL
DGM188AL/HR		DG387AAL/883
DGM188AL/883B		DG387AAL/883
DGM188BA		DG387ABA
DGM188BK		DG387ABK
DGM188CJ		DG387ACJ
DGM189AK/883B	DG403AK/883	
DGM190AK	DG403AK	
DGM190AK/HR	DG403AK/883	
DGM190AK/883B	DG403AK/883	
DGM190AL		DG190AL
DGM190AL/HR		DG190AL/883
DGM190AL/883B		DG190AL/883
DGM190BK	DG403AK	
DGM190CJ	DG403DJ	
DGM191AK	DG403AK	
DGM191AK/HR	DG403AK/883	
DGM191AK/883B	DG403AK	
DGM191AL		DG191AL
DGM191AL/HR		DG191AL/883

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
DGM191AL/883B		DG191AL/883
DGM191BK	DG403AK	
DGM191CJ	DG403DJ	
DGP201AAK	DG441AK	
DGP201AAK/883	DG44AK/883	
DGP201ADJ	DG441DJ	
DGP201ADY	DG441DY	
DGP303AAK	DG403AK	
DGP303AAK/883	DG403AK/883	
DGP303ADJ	DG403DJ	
DGP303ADY	DG403DY	
DGP508AAK	DG408AK	
DGP508AAK/883	DG408AAK/883	
DGP508ADJ	DG408DJ	
DGP509AAK	DG409AK	
DGP509AAK/883	DG409AK/883	
DGP509ADJ	DG409DJ	
DGP509ADY	DG409DY	
HI1-200-2	DG200AAK	
HI1-200-4	DG200ABK	
HI1-200-5	DG200ABK	
HI1-200-8	DG200AAK/883	
HI1-201-2	DG201AAK	
HI1-201-8	DG201AAK/883	
HI1-300-2	DG300AAK	
HI1-300-5	DG300ABK	
HI1-300-8	DG300AAK/883	
HI1-301-2	DG301AAK	
HI1-301-5	DG301ABK	
HI1-301-8	DG301AAK/883	
HI1-302-2	DG302AAK	
HI1-302-5	DG302ABK	
HI1-302-8	DG302AAK/883	
HI1-303-2	DG303AAK	
HI1-303-5	DG303ABK	
HI1-303-8	DG303AAK/883	
HI1-304-2	DG304AAK/883	
HI1-304-5	DG304ABK	
HI1-304-8	DG304AAK/883	
HI1-305-2	DG305AAK/883	
HI1-305-5	DG305AAK/883	
HI1-305-8	DG305AAK/883	
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HI1-306-5	DG306AAK/883	
HI1-306-8	DG306AAK/883	
HI1-307-2	DG307AAK/883	
HI1-307-5	DG307ABK	
HI1-307-8	DG307AAK/883	
HI1-381-2	DG381AAK/883	
HI1-381-5	DG381ABK	
HI1-381-8	DG381AAK/883	
HI1-384-8	DG405AK/883	
HI1-387-2	DG387AAK/883	
HI1-387-5	DG387AAK/883	
HI1-387-8	DG387AAK/883	
HI1-390-8	DG403AK/883	
HI1-5041-2	DG401AK	
HI1-5041-5	DG401AK	
HI1-5041-8	DG401AK/883	
HI1-5043-2	DG403AK	
HI1-5043-5	DG403AK	
HI1-5043-8	DG403AK/883	
HI1-5045-2	DG405AK	
HI1-5045-5	DG405AK	
HI1-5045-8	DG405AK/883	

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
HI1-506-2	DG506AAR/883	
HI1-506-8	DG506AAR/883	
HI1-506L-2	DG526AK/883	
HI1-506L-5	DG526AK/883	
HI1-506L-8	DG526AK/883	
HI1-507-2	DG507AAR/883	
HI1-507-8	DG507AAR/883	
HI1-507L-2	DG527AK/883	
HI1-507L-5	DG527AK/883	
HI1-507L-8	DG527AK/883	
HI1-508-2	DG508AAK	
HI1-508-5	DG508ACK	
HI1-508-8	DG508AAK/883	
HI1-508A-2	DG458AK	
HI1-508L-2	DG528AK	
HI1-508L-5	DG528CK	
HI1-508L-8	DG528AK/883	
HI1-509-2	DG509AAK	
HI1-509-5	DG509ACK	
HI1-509-8	DG509AAK/883	
HI1-509A-2	DG459AK	
HI1-509L-2	DG529AK/883	
HI1-509L-5	DG529AK/883	
HI1-509L-8	DG529AK/883	
HI2-200-2	DG200AAA	
HI2-200-4	DG200ABA	
HI2-200-5	DG200ACA	
HI2-200-8	DG200AAA/883	
HI2-300-2	DG300AAA/883	
HI2-300-5	DG300ABA	
HI2-300-8	DG300AAA/883	
HI2-301-2	DG301AAA	
HI2-301-5	DG301ABA	
HI2-301-8	DG301AAA/883	
HI2-304-2	DG304AAA	
HI2-304-5	38510/11605BIC	
HI2-304-8	DG304AAA/883	
HI2-305-2	38510/11606BIC	
HI2-305-5	DG305ACA	
HI2-305-8	38510/11606BIC	
HI2-381-2	DG381AAA	
HI2-381-5	DG381ACA	
HI2-387-2	DG387AAA/883	
HI2-387-8	DG387AAA/883	
HI3-200-5	DG200ACJ	
HI3-201-5	DG201ACJ	
HI3-300-5	DG300ACJ	
HI3-301-5	DG301ACJ	
HI3-302-5	DG302ACJ	
HI3-303-5	DG303ACJ	
HI3-304-5	DG304ACJ	
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HI3-306-5	DG306ACJ	
HI3-307-5	DG307ACJ	
HI3-381-5	DG381ACJ	
HI3-387-5	DG387ACJ	
HI3-390-5	DG403DJ	
HI3-5041-5	DG401DJ	
HI3-5043-5	DG403DJ	
HI3-5045-5	DG405DJ	
HI3-506-5	DG506ACJ	
HI3-506L-5	DG526AK/883	
HI3-507L-5	DG527AK/883	
HI3-508-5	DG508ACJ	
HI3-508A-4	DG458DJ	
HI3-508A-5	DG458DJ	
HI3-508L-5	DG528CJ	
HI3-509-5	DG509ACJ	
HI3-509A-4	DG459DJ	
HI3-509A-5	DG459DJ	
HI3-509L-5	DG529AK/883	
ICL7660CBA	SI7660DY	
ICL7660CPA	SI7660CJ	
ICL7662CPA	SI7661CJ	
ICL7662CTV	SI7661AA	
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IH181CTW	DG181BA	
IH181MTW	DG181AA	
IH182CJD	DG182BP	
IH182CTW	DG182BA	
IH182MJD	DG182AP	
IH182MTW	DG182AA	
IH184CJE	DG184BP	
IH184MJE	DG184AP	
IH185CJE	DG185BP	
IH185MJE	DG185AP/883	
IH187CTW	DG187BA	
IH187MJD	DG187AP	
IH187MTW	DG187AA	
IH188CJD	DG187BP	
IH188CTW	DG188BA	
IH188MJD	DG188AP/883	
IH188MTW	DG188AA	
IH190CJE	DG190BP	
IH190MJE	DG190AP	
IH191CJE	DG191BP	
IH5041CJE	DG401CK	
IH5041CPE	DG401CJ	
IH5041MJE	DG401AK	
IH5041MJE/HR	DG401AK/883	
IH5041MJE/883	DG401AK/883	
IH5043CJE	DG5043CK	
IH5043CPE	DG5043CJ	
IH5043MJE	DG403AK	
IH5043MJE/HR	DG5043AK/883	
IH5043MJE/883	DG5043AK/883	
IH5045CJE	DG405CK	
IH5045CPE	DG5045CJ	
IH5045MJE	DG405AK	
IH5045MJE/HR	DG5045AK/883	
IH5045MJE/883	DG5045AK/883	
IH5141CJE	DG401AK	
IH5141CPE	DG401DJ	
IH5141MJE	DG401AK	
IH5141MJE/883	DG401AK/883	
IH5143CJE	DG5143CJ	
IH5143CPE	DG403DJ	
IH5143MJE	DG403AK	
IH5143MJE/883	DG403AK/883	
IH5145CJE	DG405AK	
IH5145CPE	DG405DJ	
IH5145MJE	DG405AK	
IH5145MJE/883	DG405AK/883	
IH6108CJE	DG508ACK	
IH6108CPE	DG508ACJ	
IH6108MJE	DG508AAK	
IH6116CJI	DG506AAK/883	
IH6116CPI	DG506ACJ	
IH6116MJI	DG506AAK	
IH6208CJE	DG509ACK	

Cross Reference

Siliconix incorporated

COMPETITIVE PART NUMBER	SILICONIX PART NUMBER	APPROXIMATE REPLACEMENT
IH6208CPE	DG509ACJ	
IH6208MJE	DG509AAK	
IH6216CJI	DG507AAR/883	
IH6216CPI	DG507ACJ	
IH6216MJI	DG507AAR/883	
LF11201D		DG411AK
LF11201N		DG411DJ
LF11202D		DG412AK
LF12201D		DG411AK
LF12202D		DG412AK
LF12202N		DG412DJ
LF13201D		DG411AK
LF13201N		DG411DJ
LF13202D		DG412AK
LF13202N		DG412DJ
LTC1044CJ8	SI7660CJ	
LTC1044MH	SI7660AA/883	
L144AP	L144AP/883	
L161AP	L161AP/883	
L161AP-2	L161AP/883	
MAX331MJE	DG441AK	
MAX332MJE	DG442AK	
MAX358CPE	DG458DJ	
MAX358EPE	DG458DJ	
MAX358MJE	DG458AK	
MAX359CPE	DG459DJ	
MAX359EPE	DG459DJ	
MAX359MJE	DG459AK	
MPC16S		DG506AAR/883
MPC4D		DG509ADK
MPC8D		DG507AAR/883
MPC8S		DG508ADK
MP200DIAA		DG200AAA
MP200DIAP		DG200AAK
MP200DIBA		DG200ABA
MP200DICJ		DG200ACJ
MP200DIPB		DG200ABK
MP201DIAP		DG411AK
MP201DIBP		DG411AK
MP201DICJ		DG411CJ
MP302DIAP	DG302AAK	
MP302DIBP	DG302AAK	
MP302DICJ	DG302CJ	
MP303DIAP	DG303AAK	
MP303DIBP	DG303AAK	
MP303DICJ	DG303ACJ	
MP7501JD		DG501BK
MP7501JN		DG501CJ
MP7501KD		DG501BK
MP7501KN		DG501CJ
MP7501SD		DG501AK
MP7501TD		DG501AK
MP7503JD		DG503BK
MP7503JN		DG503CJ
MP7503KD		DG503BK
MP7503KN		DG503CJ
MP7503SD		DG503AK
MP7503TD		DG503AK
MP7506JD	DG506AAR/883	
MP7506JN	DG506ACJ	
MP7506KD	DG506AAR/883	
MP7506KN	DG506ACJ	
MP7506SD	DG506AAR/883	
MP7506TD	DG506AAR/883	
MP7507JD	DG507AAR/883	
MP7507JN	DG507ACJ	
MP7507KD	DG507AAR/883	
MP7507KN	DG507ACJ	
MP7507SD	DG507AAR/883	
MP7507TD	DG507AAR/883	
MP7508KD		DG508ABK
MP7508KN		DG508ACJ
MP7508SD		DG508AAK
MP7509KD		DG509ABK
MP7509KN		DG509ACJ
MP7509SD		DG509AAK
MUX08BQ		DG408AK
MUX08FP		DG408DJ
MUX08FQ		DG408AK
MUX16BT		DG506AAR
MUX16FT		DG506ABR
MUX24BQ		DG409AK
MUX24FP		DG409DJ
MUX24FQ		DG409AK
MUX28BT		DG507AAR
MUX28FT		DG507ABR
SI3705142K	DG503AP/883	
SI3705142P	DG503AP/883	DG503AK
SI3705192P	DG503AP/883	DG503AK
SI520DJ	SI8601DJ	
SI520DK	SI8601AK/883	
SI6009DL		G118AL
SI7652DK	SI7652DK	
SI7661CA	SI7661AA	
SI8601AK	SI8601AK/883	
SI8601DK	SI8601AK/883	
SW01BQ		DG201AAK
SW01BQ883		DG201AAK/883
SW01FQ		DG201ABK
SW02BQ		DG202AAK
SW02BQ883		DG202AAK/883
SW02FQ		DG202ABK
SW05BK		DG200AAA
SW05BK883		DG200AAA/883
SW05BY		DG200AAK
SW05BY883		DG200AAK/883
SW05FK		DG200ABA
SW05FY		DG200ABK
SW05GP		DG202ACJ
SW201BQ		DG411AK
SW201BQ883		DG411AK/883
SW201FQ		DG411AK
SW201GP		DG411DJ
SW202BQ		DG412AK
SW202BQ883		DG412AK/883
SW202FQ		DG412AK
SW202GP		DG412DJ
TSC7660COA	SI7660DY	
TSC7660CPA	SI7660CJ	
UC161AJ	L161AP	
UC161BJ	L161BP	
UC161CN	L161CJ	

This Cross Reference material is accurate to the best knowledge and belief of Siliconix, incorporated. Since individual circuit design and layout can influence device performance, the purchaser must be responsible for the ultimate selection and determination of interchangeability.

TABLE OF CONTENTS

ANALOG SWITCHES AND MULTIPLEXERS

Introduction

Siliconix is the world's leading supplier of high performance, precision solid-state analog switches and multiplexers. Through the implementation of state-of-the-art technologies (Metal-Gate CMOS, High-Voltage Silicon-Gate CMOS, and PolyMOS® and JFET processes) in conjunction with advanced design techniques, the products shown in this section represent a broad selection of industrial, military, and commercial grade parts suiting a wide range of applications. Siliconix is dedicated to giving the designer the widest range of functions, performance, and packaging as standards to ensure ease of design.

The products in this section include pin-compatible upgrades for most of the popular Siliconix "DG" series of single, dual, and quad analog switches, single-ended and differential multiplexers plus many new and preliminary devices.

Siliconix is establishing new standards in the high performance switch and multiplexer arena with our proprietary high voltage silicon gate DG4XX family. The established DG2XX, DG3XX and DG5XX families are made on our mature metal gate process which gives adequate performance for many applications. If higher performance (i.e. lower ON-resistance, leakage currents, and power dissipation with faster switching) is required in your application, then the DG4XX family is recommended. Most of our DG4XX devices, including analog switches, multiplexers, latched switches, and switch array, incorporate ESD protection > ±4000 V. Single supply operation, charge injection optimization, and a wide range of packaging options, including small outline and PLCC, are additional benefits of this family. Of course, we still offer the popular JFET (DG18x) family of switches.

If extremely fast switching and very low ON-resistance are the most important parameters in your system, then the DG601 PolyMOS® quad analog switch, pin compatible with the industry standards DG201A is the device of choice.

The serially addressed switch array is a new architecture giving designers greater levels of flexibility in routing signals. The DG485 is a silicon-gate switch array/multiplexer that allows control of any of eight switches. Now, summing node applications can be accomplished using a high performance switch array architecture.

The following paragraphs discuss important selection criteria for analog switches and multiplexers.

Functional Description

One of the most common control elements in electrical circuitry is the ON-OFF switch. The switch has evolved over the years from the manually operated circuit breaker of the early experimenters to the multi-switch integrated circuits of today. However, the function of the switch has remained the same; to electrically isolate or connect two sections of a circuit. The ideal switch has the following characteristics:

1) Zero ON-resistance
2) Infinite OFF-resistance
3) Instantaneous t_{ON} and t_{OFF} times

Although an analog switch is not perfect and can have many different parasitic elements (Figure 1), it can still be a very good approximation of the ideal switch. ON-resistance ($r_{DS(ON)}$) can be as low as 10 Ω, OFF isolation can be as high as 90 dB (at 1 MHz), and switching speeds can reach 60 ns for a CMOS part, while PolyMOS™ products can obtain 45 ns switching speeds.

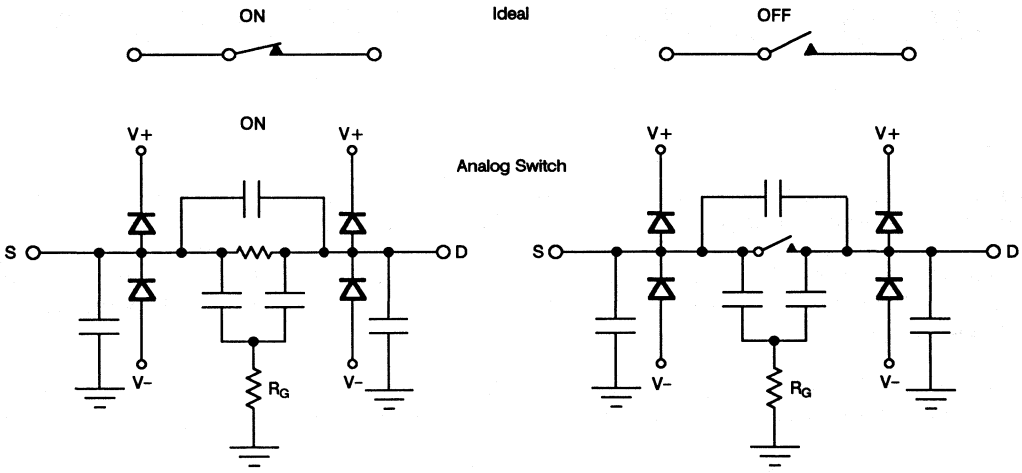


Figure 1. Comparison of the "Ideal" Switch to a Solid-state Analog Switch

CMOS

Since CMOS analog switches are parallel combinations of p- and n-channel MOSFETs, the effective ON-resistance is a combination of the PMOS and NMOS resistance curves (Figure 3). This gives a fairly constant ON-resistance over the entire analog voltage range. The CMOS switch also has the advantage of very low quiescent supply current because other than for channel leakage, no current flows in the driver except when a control input transition occurs.

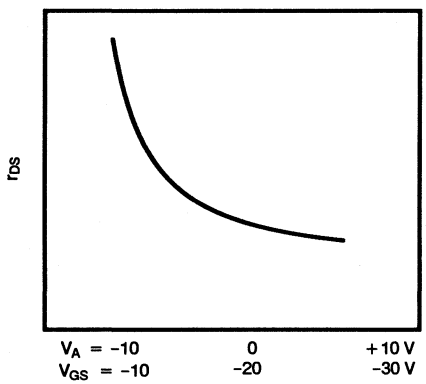


Figure 2. Variation of PMOS Switch Resistance with Signal Voltage

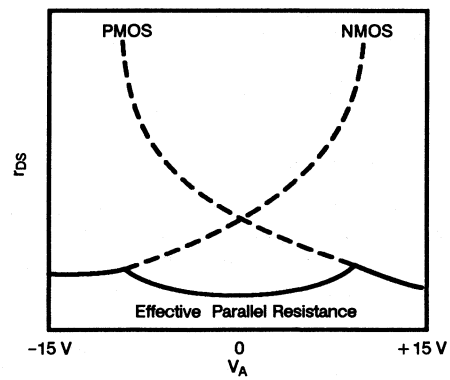


Figure 3. Graph of CMOS Switch Resistance vs. Analog Signal

Metal Gate and Silicon Gate CMOS

Both metal and silicon gate technologies are incorporated into our CMOS processes, but each is used with separate product lines. The mature metal gate process is used for our DG2XX, DG3XX, and DG5XX families. Our newer silicon-gate process (DG4XX family) is recommended for applications needing state-of-the-art performance and versatility.

Figure 4 gives a comparison of the ON-resistance curves for a JFET (DG180), a PMOS (DG172), a metal gate CMOS (DG201A) and a silicon gate CMOS (DG400) analog switches.

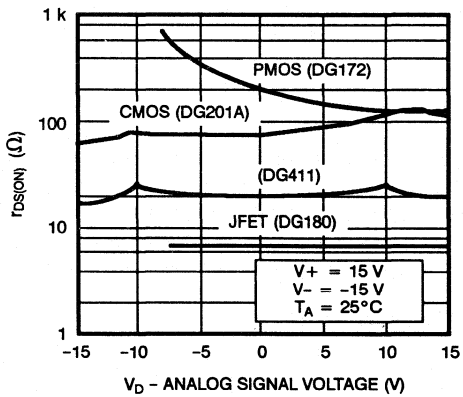


Figure 4. On-resistance for Several Analog Switch Technologies

Important Switch Parameters

Each switch family in the Siliconix product line has a set of distinct characteristics that make it suitable for certain types of applications. Several major specifications should be compared and prioritized before selecting an analog switch for a particular circuit.

$r_{DS(ON)}$

This specification is simply the dc resistance of the channel when the analog switch is in the ON state. As explained earlier, the ON-resistance of an analog switch depends upon the device type and the analog signal magnitude. Although the resistance may vary across the entire analog signal range, the worst case is normally specified on the data sheet.

Switching Speed

Switching speed is the elapsed time from the application of the control signal on the input pin to the appearance (or disappearance) of the analog signal at the output. Switching speed can be affected by the load on the analog switch. Each data sheet shows a switching time test circuit with a standard load for comparison purposes.

Switch Current

The amount of current that can be fed through the switch channel is sometimes important. For example, the DG411 can handle up to 100 mA of pulsed current or 30 mA of continuous current, while the DG180 can pass up to 200 mA of continuous current.

Break-Before-Make vs. Make-Before-Break

For most analog switch applications, break-before-make switching is desired. This is the case because in most applications it is necessary to disconnect one signal source before connecting another to avoid source crosstalk. However, make-before-break switching is critical in some control circuits such as the feedback resistor gain selector for programmable gain op amps, to avoid opening the loop.

Electrostatic Discharge Sensitivity (ESDS)

Electrostatic discharge is the transfer of charge that occurs when an object makes contact with a device at a different potential. The government, per MIL-883C method 3015.7, has classified three levels of voltage protection that a device must withstand on all pins. Class 1 devices are protected to 1999 V, Class 2 from 2000 to 3999 V, and Class 3 protection is greater than 4000 V. Beginning with the DG411 series, all our new devices have Class 2 or 3 ESDS ratings and are marked accordingly.

Charge Injection

Charge injection is the transfer of charge to a load from the gates of the FETs during switching. In a sample and hold circuit, charge injection is critical as the charge added or subtracted from the holding capacitor is seen as an offset error. The lower the charge injection the better. The DG4XX family, especially the DG441 and DG411 series, are designed for balanced (linear and crossing near zero) charge injection. The DG601 and DG441 use internal compensation on the drain and/or source to minimize the charge injection seen by applications sensitive to this parameter.

Power Supplies and Power Consumption

A bipolar supply means positive and negative voltages are used, while single supply means the negative supply is grounded. Most analog designs use bipolar supplies, but a growing number are turning to single supply operation to save board space and cost. Most of our devices work well with bipolar supplies but not all function properly in the single supply mode. The DG4XX family of analog switches and multiplexers not only function superbly in a single supply mode, but is fully characterized and specified with V+ at 12 V and V– at GND. The lower the power consumed by a device within a system the better. Some members of the DG4XX family draw under 1 μA of supply current compared to the milliamps required by previous products.

Interfacing

This can be one of the most important parameters of an analog switch application since so many possibilities exist. The two most important interface criteria are logic compatibility and microprocessor compatibility.

The two most common logic families are TTL and CMOS. The standard logic levels for both families are displayed in Table 1. Remember that not all analog switches are compatible with both types of logic. Refer to the functional diagram section of each data sheet to determine the required logic levels.

Table 1

Logic	TTL	CMOS
"0"	$\leq$ 0.8 V	$\leq$ 1.5 V
"1"	$\geq$ 2.4 V	$\geq V_{CC}$ – 1.5 V

Logic Levels for TTL and CMOS Compatibility

Microprocessor compatibility is a growing concern when designing with analog switches. Standard analog switches require a constant control signal present on the input to hold the switch in the desired position (ON or OFF). This could tie up a microprocessor control system unless external latches are added to control the switch. The DG42X series has incorporated these latches, complete with control logic, onboard to minimize parts count and ease interface to microprocessor-based control systems.

Multiplexing

Analog multiplexers represent a higher level of integration of analog switches. They have many (4, 8, 16, or more) inputs with only 1 or 2 common outputs. Multiplexers are used where it is necessary to transfer information from many signal channels at a transmitting point to a central or common receiving point, or vice versa. This is most often used when only one transmission line is available for all data transfer between points. The transmitted signals are in either analog or digital form, with multiplexers in this section being the analog variety that pass bipolar voltages or currents which are often obtained from transducers. The analog signals may represent any physical phenomenon such as temperature, pressure, velocity, speech, etc. Examples of this can be found in data acquisition, industrial process control, aircraft systems monitoring, medical electronics, telemetry, and communications.

Differential vs. Single-Ended Multiplexing

When is it better to select a differential multiplexer versus a single-ended configuration? Figures 5 and 6 demonstrate both options. Single-ended multiplexing, as shown in Figure 5, applies to systems that have signal sources that are close to full-scale range and are referenced to a common point (usually ground). Another case is where differential signal sources with small signal amplitude (millivolt range) are generated by transducers. Instrumentation amplifiers can be used to precondition the signals and provide a common reference. This reduces feedthrough errors and losses while tailoring each signal source to a desired voltage (or current) to obtain the maximum resolution available in an A/D or D/A converter or other device driven by the multiplexer.

Differential multiplexing (Figure 6) is utilized for low level switching and in noisy environments. It can tolerate switching transients or some mismatch without a significant degradation of the signal accuracy via the multiplexer. Major considerations are switch matching ($r_{DS(ON)}$, $I_{(OFF)}$, and capacitance), common-mode rejection, and the system's tolerance to switching transients introduced by the break-before-make switching sequence.

5

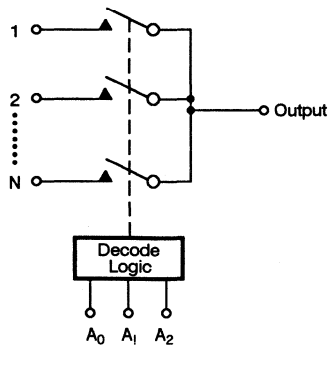


Figure 5. Single-Ended Multiplexing

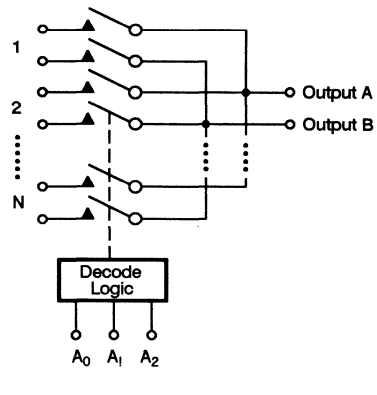


Figure 6. Differential Multiplexing

Factors Affecting System Performance

In any multiplexer application, the following factors should be considered:

1) System Attenuation -- Includes loss in the analog signal caused by the multiplexer and the transmission path. This is a frequency dependent factor.

2) Channel Isolation -- At low frequencies, this is principally a function of channel OFF leakage currents, and at high frequencies, it is a function of device and system capacitances.

3) Crosstalk -- There are several sources of crosstalk, including: overlap between switching channels due to imperfect break-before-make switching, switch leakages, OFF switch capacitances, inter-switch capacitances, stray circuit capacitances, distortion in the transmission medium, etc.

4) Noise -- There are several sources of noise, including thermal or Johnson noise generated in any resistive components, crosstalk, leakages, switching transients, as well a thermal EMFs and transmission path pickup.

5) Switching Rate -- This is important in sampling system where it determines the maximum bandwidth frequency of the multiplexer (via the sampling theorem) and defines crosstalk errors.

6) Settling Time -- Although settling time is a function of the source and load impedances, the multiplexer's contribution is directly related to the $r_{DS(ON)} \times C_{S(ON)}$ time constant and to the charge injection of the multiplexer.

Siliconix incorporated

DG180/181/182
High-Speed Drivers with Dual SPST JFET Switches

FEATURES

- Constant ON-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

The DG180-182 are precision dual single-pole, single-throw (SPST) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON-resistance over the entire analog range.

The major design difference is the ON-resistance, being 10, 30, and 75 Ω for the DG180, DG181, and DG182 respectively. Reduced switching errors are achieved through low leakage current ($I_{S(OFF)}$ < 1 nA for the DG181/182). Applications which benefit from flat ON-resistance include audio switching, video switching, and sample and holds.

Each device comprises four n-channel JFET transistors and a bipolar driver (TTL compatible) to achieve fast and accurate switch performance. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

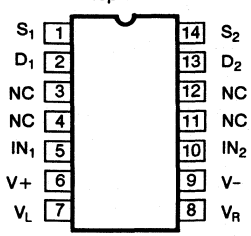
Packaging options for the DG180-182 include a 14-pin side braze and 10-pin metal can options. The flatpack version is only available for the DG181. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

PIN CONFIGURATION

5

Dual-In-Line Package

Top View

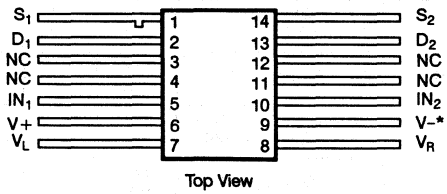


Order Numbers:

Side Braze:

DG180AP, DG180AP/883, DG180BP
DG181AP, DG181AP/883, DG181BP
DG182AP, DG182AP/883, DG182BP

Flat Package

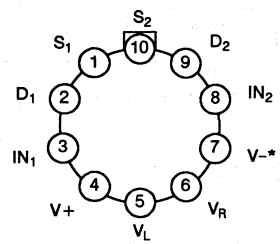


Top View

Order Number:

Refer to JAN38510 Information Chapter 1

Top View



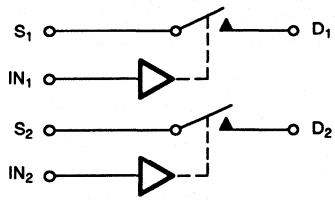
Metal Can Package

Order Numbers:

DG180AA, DG180AA/883, DG180BA
DG181AA, DG181AA/883, DG181BA
DG182AA, DG182AA/883, DG182BA

*Common to Substrate and Case

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



Two SPST Switches per Package

Truth Table*

Logic	Switch
0	ON
1	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 36 V
V+ to V_D ..... 33 V
V_D to V- ..... 33 V
V_D to V_D ..... ±22 V
V_L to V- ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V- ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG180 ..... 200 mA
Current (S or D) DG181, DG182 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C

Power Dissipation*
10-Pin Metal Can** ..... 450 mW
14-Pin DIP*** ..... 825 mW
14-Pin Flat Pack**** ..... 900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a] (DG180)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5, V_{IN} = 0.8 V		Room Full	7.5		10 20		15 25	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.05		10 1000		15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		10 1000		15 300	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 0.8 V		Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration		Room	300					mA

SPECIFICATIONS[a] (DG180)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	240		400		600	ns
Turn-OFF Time	t_{OFF}			Room	140		200		250	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	21					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	17					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	17					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>55					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG181)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5 V_{IN} = 0.8 V		Room Full	18		30 60		50 75	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.07		1 100		5 100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.5		1 100		5 100	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.6		1 100		5 100	

5

SPECIFICATIONS[a] (DG181)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 0.8 V		Room Hot	-0.02	-2 -200		-10 -200		nA
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-OFF Time	t_{OFF}			Room	95		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG182)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-10	15	-10	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5 V_{IN} = 0.8 V		Room Full	35		75 150		100 150	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.07		1 100		5 100	

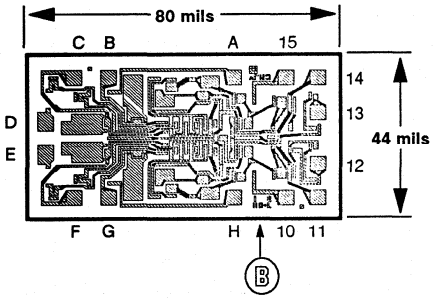
SPECIFICATIONS[a] (DG182)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 2 V	V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.4		1 100		5 100	nA
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.5		1 100		5 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 0.8 V		Room Hot	-0.02	-2 -200		-10 -200		
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	120		250		300	ns
Turn-OFF Time	t_{OFF}			Room	100		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Room = 25°C, Hot and Full = as determined by the operating temperature suffix.

5

DIE TOPOGRAPHY (DRIVER)



Interchip Pad Connections

A No Connection
B No connection
C To JFET 2, Gate
D From JFET 2, Source
E From JFET 1, Source
F To JFET 1, Gate
G No Connection
H No Connection

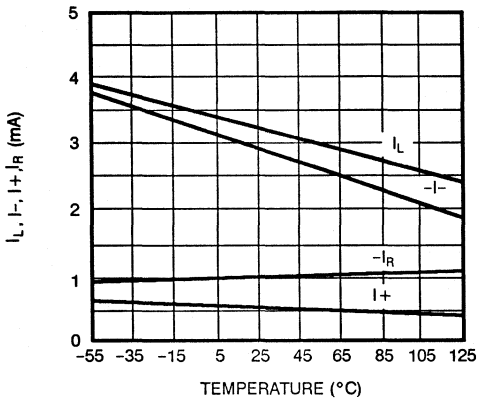
Pad No.	Function
10	IN_2
11	V+
12	V_L
13	V_R
14	V- (Substrate)
15	IN_1

CMJB
6 Capacitors
7 Resistors
8 p-channel Depletion MOSFETs
2 n-channel Depletion MOSFETs

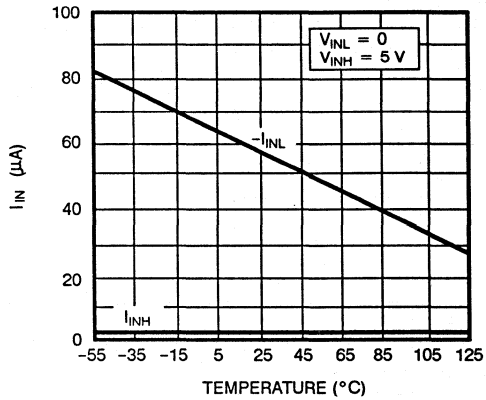
8 PNP bipolar Transistors
4 NPN bipolar Transistors
4 Diodes

TYPICAL CHARACTERISTICS

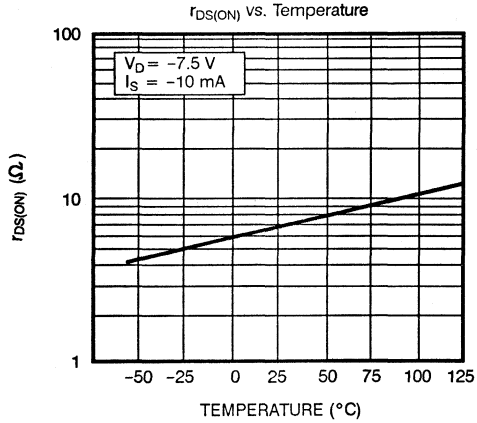
Supply Current vs. Temperature



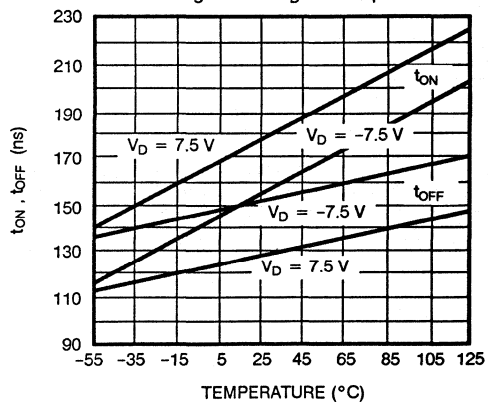
I_{IN} vs. V_{IN} and Temperature



10 Ω DG180
$r_{DS(ON)}$ vs. Temperature

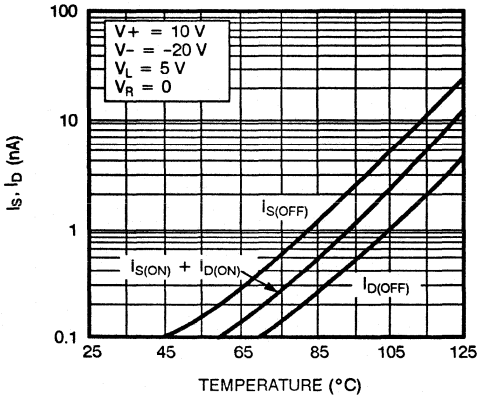


10 Ω DG180
Switching Time vs. V_D and Temperature

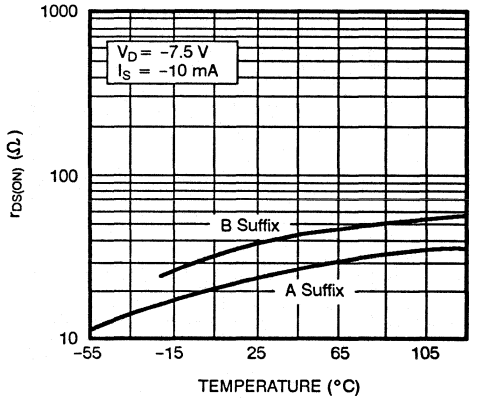


TYPICAL CHARACTERISTICS (Cont'd)

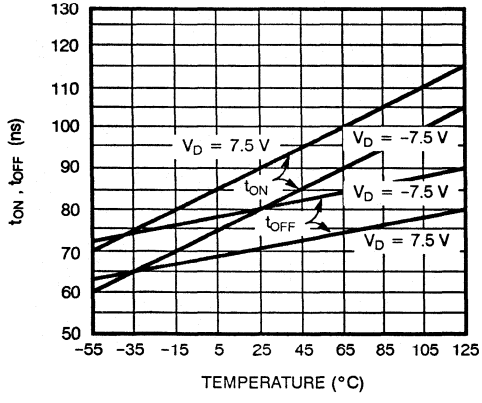
10 Ω DG180
Leakage vs. Temperature



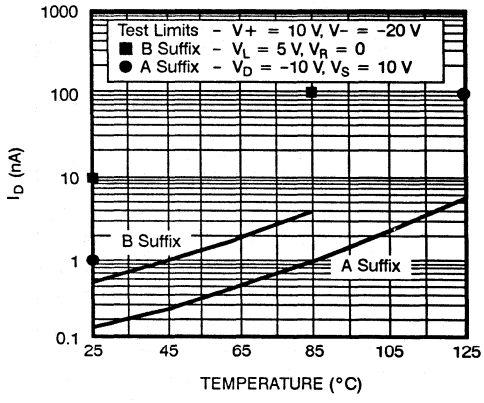
30 Ω DG181
$r_{DS(ON)}$ vs. Temperature



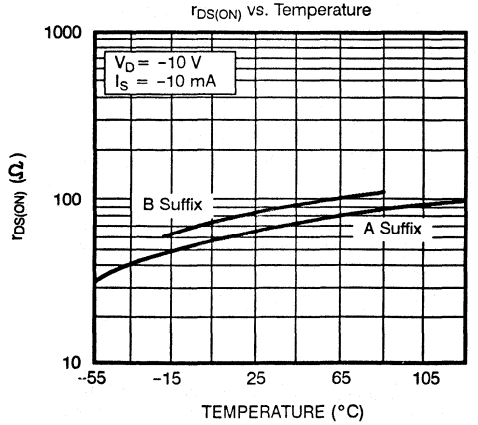
30 Ω DG181
Switching Time vs. V_D and Temperature



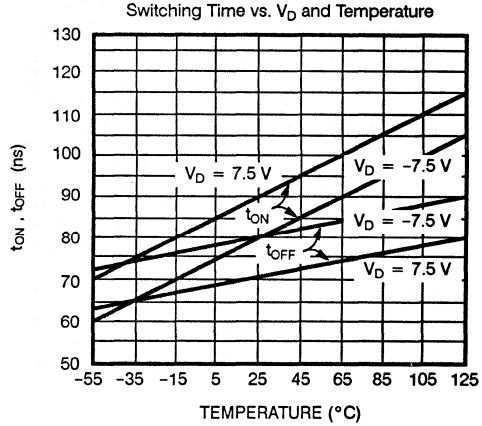
30 Ω DG181
$I_{D(OFF)}$ vs. Temperature



75 Ω DG182
$r_{DS(ON)}$ vs. Temperature



75 Ω DG182
Switching Time vs. V_D and Temperature



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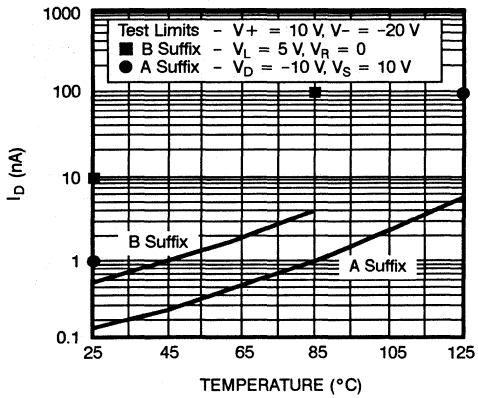
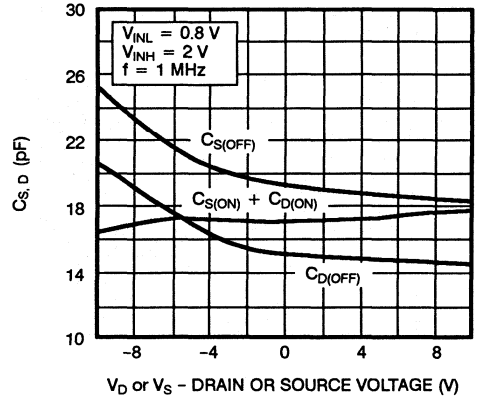
TYPICAL CHARACTERISTICS (Cont'd)

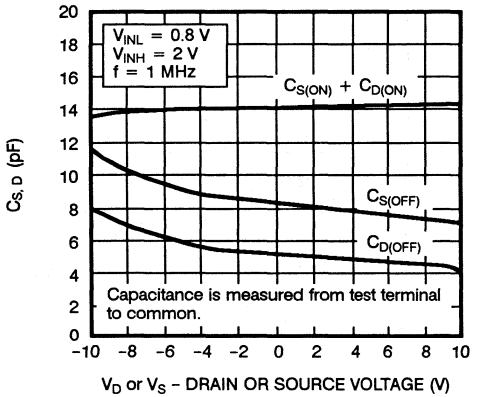
75 Ω DG182
$I_{D(OFF)}$ vs. Temperature



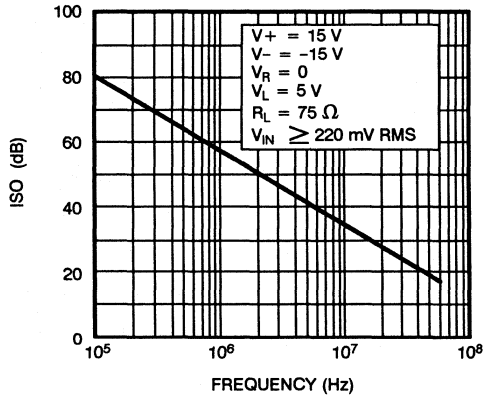
Capacitance vs. V_D or V_S (10 Ω FET)



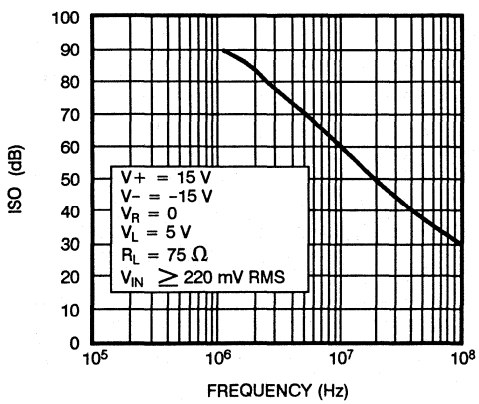
Capacitance vs. V_D or V_S (30 - 75 Ω FET)



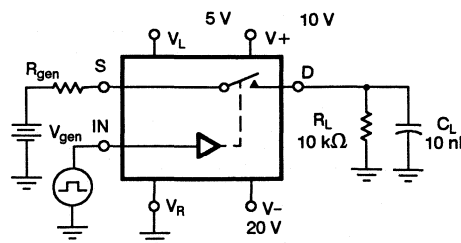
OFF Isolation vs. Frequency (10 Ω FET)



OFF Isolation vs. Frequency (30 - 75 Ω FET)



Typical delay, rise, fall settling times, and switching transients in this circuit.



If R_{gen}, R_L, or C_L is increased, there will be proportional increases in rise and/or fall times.

TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

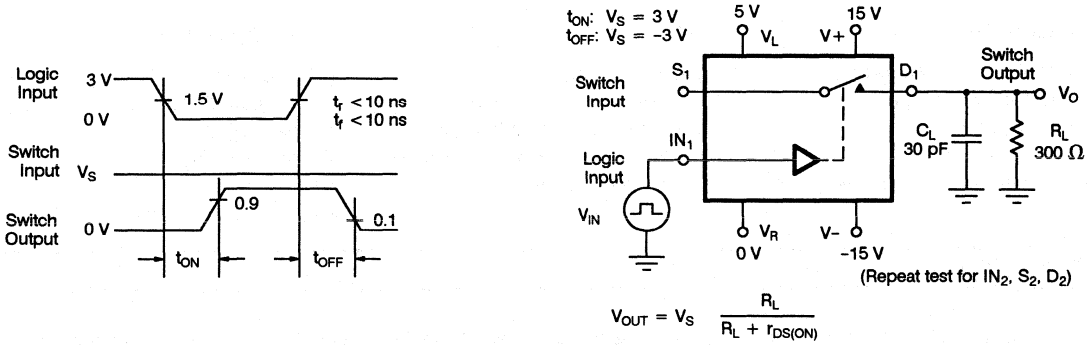


Figure 1. Switching Time

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

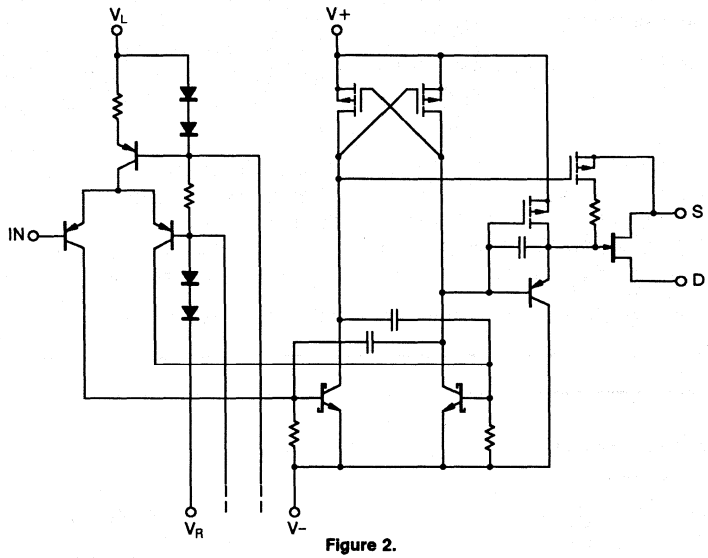


Figure 2.

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH}MIN/V_{INL}max (V)	V_S Analog Voltage Range (V)
10 Ω and 30 Ω	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 Ω	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

DG183/184/185
High-Speed Drivers with Dual DPST JFET Switches

Siliconix incorporated

FEATURES

- Constant ON-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk
- Break-Before-Make Switching

BENEFITS

- Low Distortion
- Reduced SwitchingErrors
- Improved Channel Isolation
- Eliminates Inadvertent Shorting Between Channels

APPLICATIONS

- Audio Switching
- Precision Switching
- Video Switching
- Video Routing
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

The DG183-185 are precision dual double-pole, single-throw (DPST) analog switches designed to provide accurate switching of audio and video signals. This series is ideally suited for applications requiring a constant ON-resistance over the entire analog range.

The major design difference is in ON-resistance, being 10, 30, and 75 Ω for the DG183, DG184 and DG185, respectively.

Reducing switching errors is also accomplished through low leakages ($I_{S(OFF)}$ < 1 nA for the DG184/185). Applications which benefit from flat ON-resistance include audio switching, video switching, and sample and holds.

Each device consists of four n-channel JFET transistors and a bipolar driver (TTL compatible) to achieve fast and accurate switch performance. The driver is designed to achieve Break-Before-Make switching action, eliminating inadvertent shorting and the crosstalk between channels that may result. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

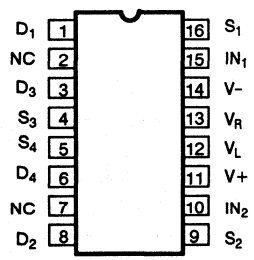
Packaging options for the DG183-185 include a 16-pin side braze and flatpack. Performance grades include both the military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

The DG184 and DG185 are JAN qualified devices.

PIN CONFIGURATION

Dual-In-Line Package

Top View

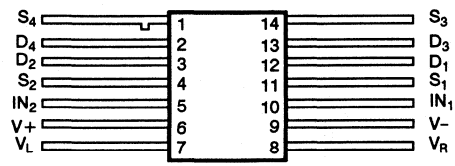


Order Numbers:

Side Braze:

DG183AP/883, DG183BP
DG184AP, DG184AP/883, DG184BP
DG185AP/883, DG185BP

Flat Package

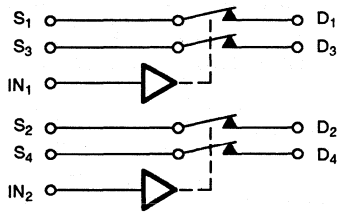


Top View

Order Numbers:

Refer to JAN38510 Information Chapter 1

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



Two DPST Switches per Package*

Truth Table*

Logic	Switch
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 36 V
V+ to V_D ..... 33 V
V_D to V- ..... 33 V
V_D to V_D ..... ±22 V
V_L to V- ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V- ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG183 ..... 200 mA
Current (S or D) DG184, DG185 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
Power Dissipation*
16-Pin DIP** ..... 900 mW
Flat Pack*** ..... 900 mW

*All leads welded or soldered to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a] (DG183)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5, V_{IN} = 2 V		Room Full	7.5		10 20		15 25	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.05		10 1000		15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		10 1000		15 300	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 2 V		Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration		Room	300					mA

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Siliconix incorporated

SPECIFICATIONS[a] (DG183)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	240		400		425	ns
Turn-OFF Time	t_{OFF}			Room	140		200		225	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	21					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	17					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	17					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>55					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG184)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5 V_{IN} = 2 V		Room Full	22		30 60		50 75	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.06		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.05		1 100		5 100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.4		1 100		5 100	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.3		1 100		5 100	

SPECIFICATIONS[a] (DG184)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 2 V		Room Hot	-0.02	-2 -200		-10 -200		nA
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-OFF Time	t_{OFF}			Room	95		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		3		3	mA
Negative Supply Current	I-			Room	-2.7	-5.5		-5.5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG185)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-10	15	-10	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = -7.5 V_{IN} = 2 V		Room Full	35		75 150		100 150	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.07		1 100		5 100	

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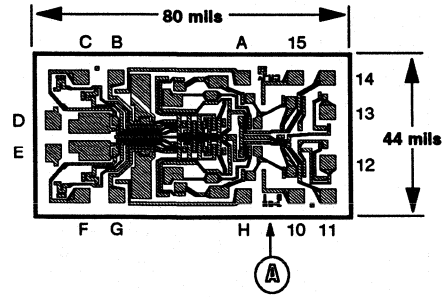
Siliconix incorporated

SPECIFICATIONS[a] (DG185)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 2 V	V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		1 100		5 100	nA
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		1 100		5 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 2 V		Room Hot	-0.03	-2 -200		-10 -200		
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	120		250		300	ns
Turn-OFF Time	t_{OFF}			Room	100		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		3		3	mA
Negative Supply Current	I-			Room	-2.7	-5.5		-5.5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Room = 25°C, Hot and Full = as determined by the operating temperature suffix.

DIE TOPOGRAPHY (DRIVER)



Interchip Pad Connections

A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Source
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

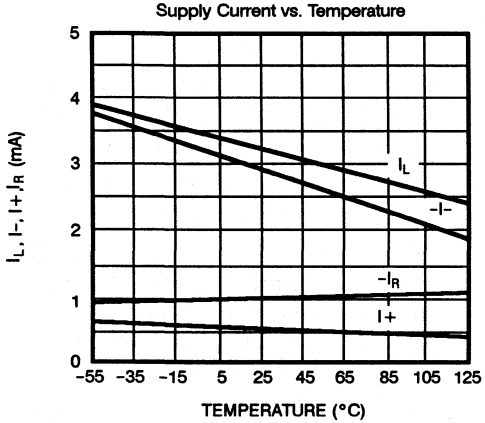
Pad No.	Function
10	IN_2
11	V+
12	V_L
13	V_R
14	V- (Substrate)
15	IN_1

CMJA
8 Capacitors
7 Resistors
12 p-channel Depletion MOSFETs
4 n-channel Depletion MOSFETs

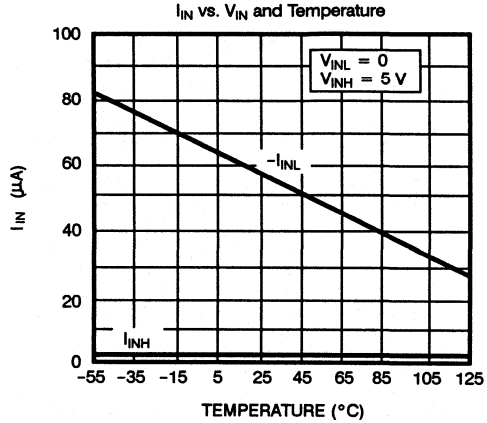
10 PNP bipolar Transistors
4 NPN bipolar Transistors
4 Diodes

TYPICAL CHARACTERISTICS

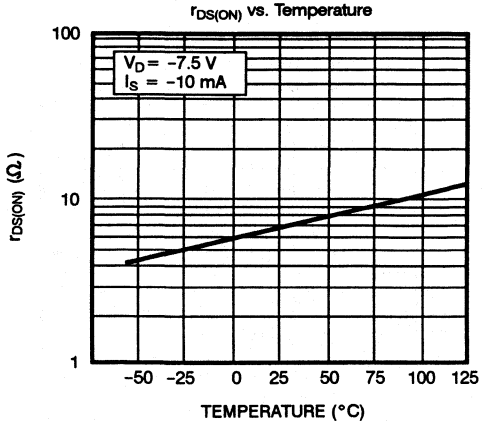
Supply Current vs. Temperature



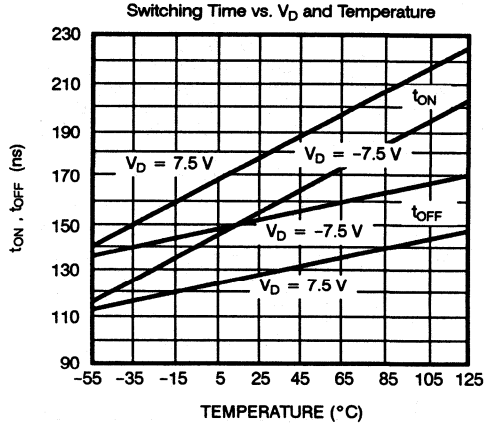
I_{IN} vs. V_{IN} and Temperature



10 Ω DG183
$r_{DS(ON)}$ vs. Temperature



10 Ω DG183
Switching Time vs. V_D and Temperature



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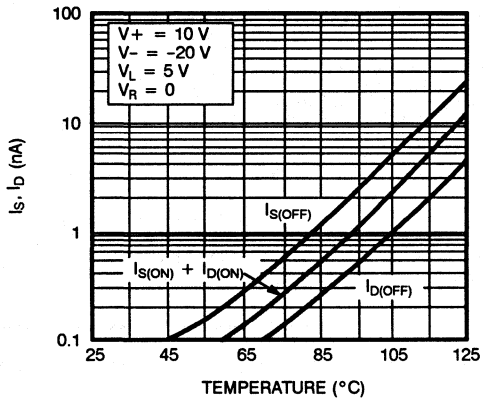
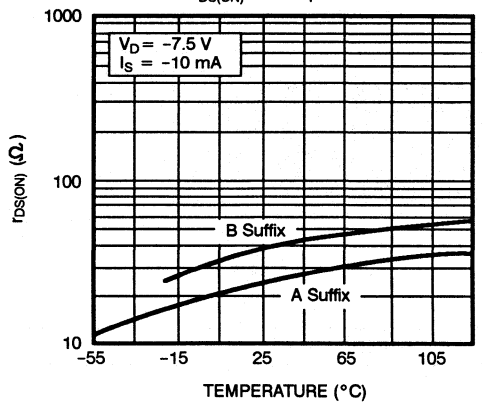
TYPICAL CHARACTERISTICS (Cont'd)

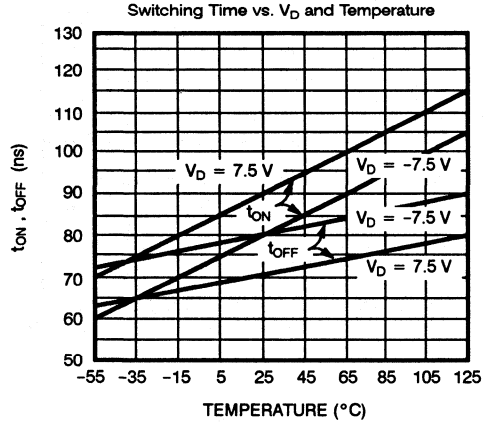
10 Ω DG183
Leakage vs. Temperature



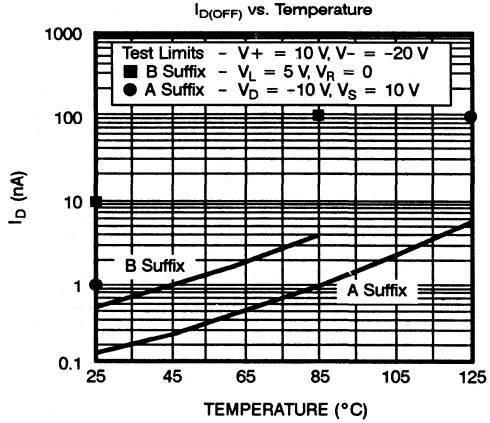
30 Ω DG184
$r_{DS(ON)}$ vs. Temperature



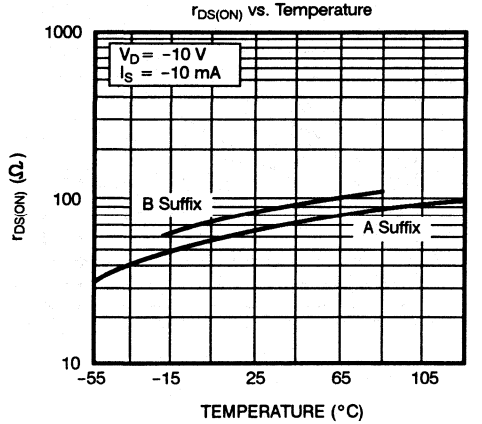
30 Ω DG184
Switching Time vs. V_D and Temperature



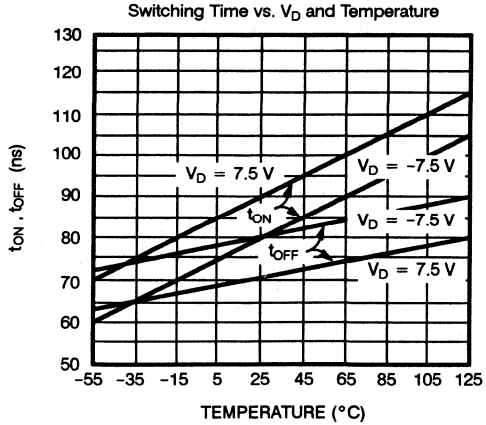
30 Ω DG184
$I_{D(OFF)}$ vs. Temperature



75 Ω DG185
$r_{DS(ON)}$ vs. Temperature

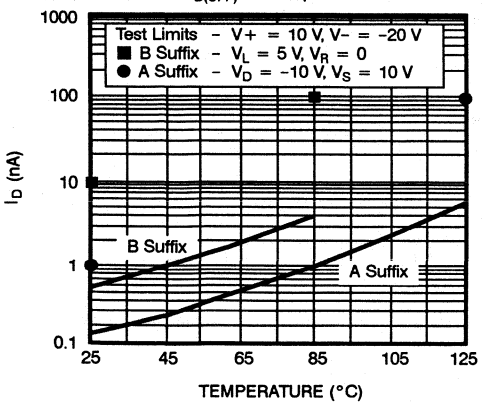


75 Ω DG185
Switching Time vs. V_D and Temperature

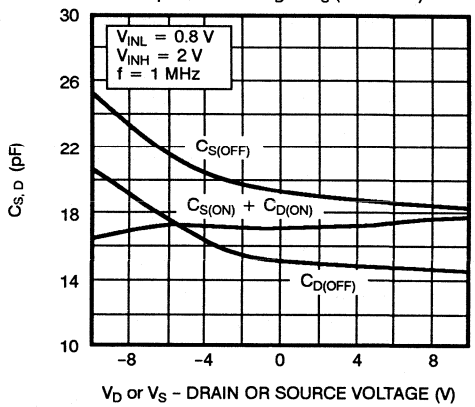


TYPICAL CHARACTERISTICS (Cont'd)

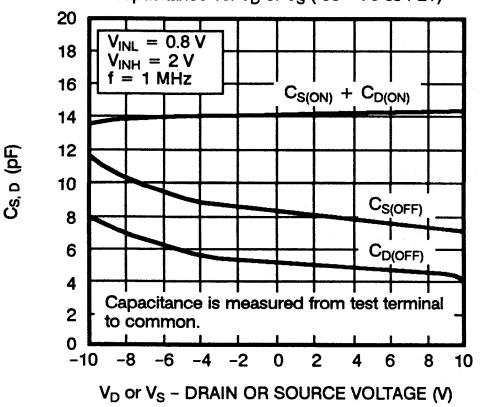
75 Ω DG185
$I_{D(OFF)}$ vs. Temperature



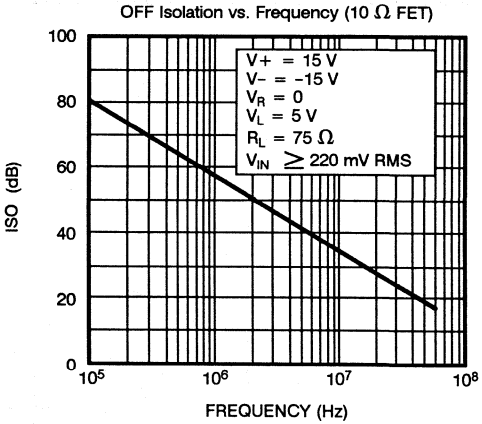
Capacitance vs. V_D or V_S (10 Ω FET)



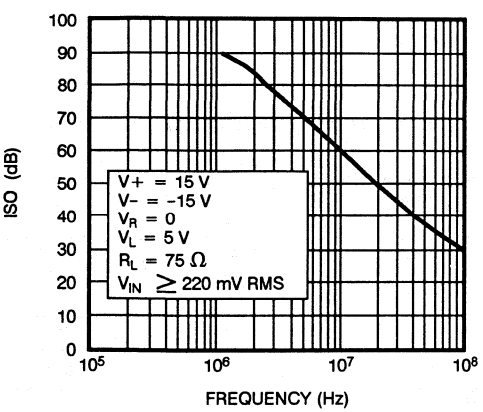
Capacitance vs. V_D or V_S (30 – 75 Ω FET)



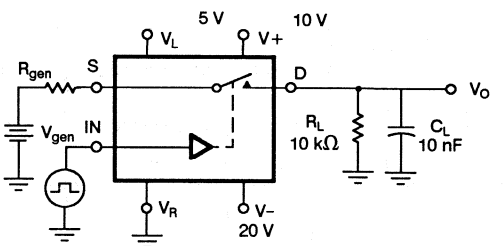
OFF Isolation vs. Frequency (10 Ω FET)



OFF Isolation vs. Frequency (30 – 75 Ω FET)



Typical delay, rise, fall settling times, and switching transients in this circuit.



If $R_{gen,}$ R_L, or C_L is increased, there will be proportional increases in rise and/or fall times.

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TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

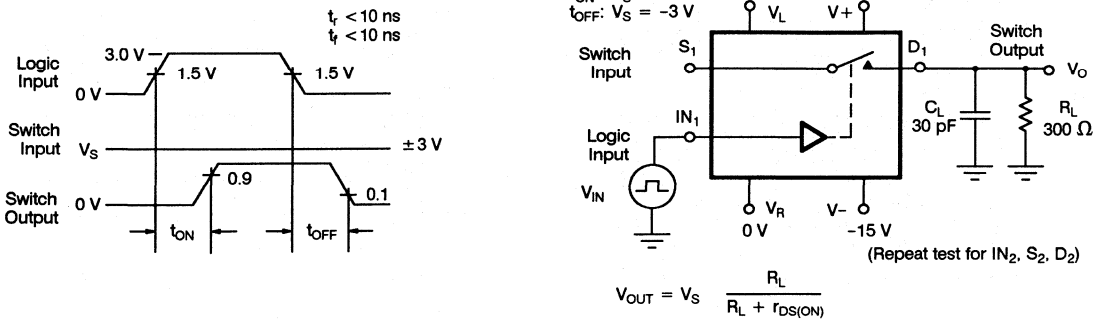

Figure 1. Switching Time

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

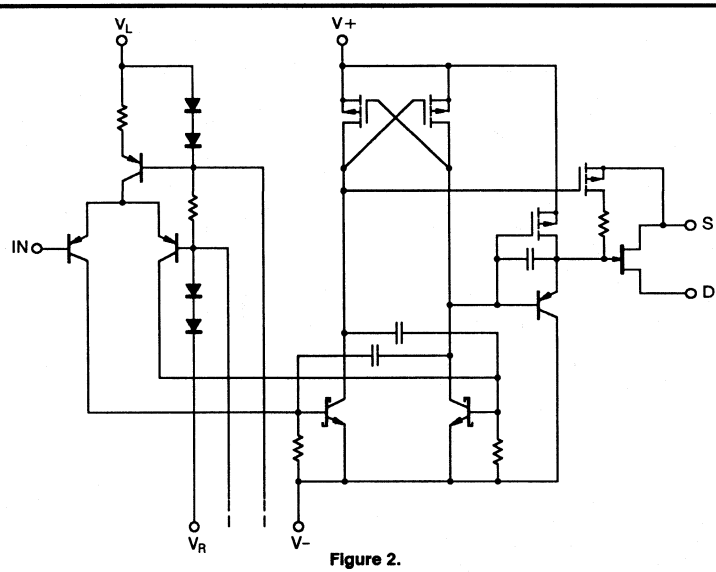

Figure 2.

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH}MIN/V_{INL}max (V)	V_S Analog Voltage Range (V)
10 Ω and 30 Ω	15**	-15	5	GND	2.0/0.8	-7.5 to 15
	10	-20	5	GND	2.0/0.8	-12.5 to 10
	12	-12	5	GND	2.0/0.8	-4.5 to 12
75 Ω	15**	-15	5	GND	2.0/0.8	-10 to 15
	10	-20	5	GND	2.0/0.8	-15 to 10
	12	-12	5	GND	2.0/0.8	-7 to 12

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

Siliconix incorporated

DG186/187/188
High-Speed Drivers with Dual SPDT JFET Switches

FEATURES

- Constant ON-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

The DG186-188 are precision single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON-resistance over the entire analog range.

The major design difference is the ON-resistance, being 10, 30, and 75 Ω for the DG186, DG187, and DG188 respectively. Reduced switching errors are achieved through low leakage current ($I_{S(OFF)} < 1$ nA for the DG187/188). Applications which benefit from flat ON-resistance include audio switching, video switching, and sample-and-holds.

Each device comprises four n-channel JFET transistors and a bipolar driver (TTL compatible) to achieve fast and accurate switch performance. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging for the DG186-188 includes a 14-pin side braze, flatpack, and 10-pin metal can options. Performance grades include both a military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature range. The flatpack option is only available in the military grade.

PIN CONFIGURATION

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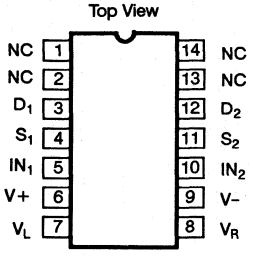
Dual-In-Line Package

Top View

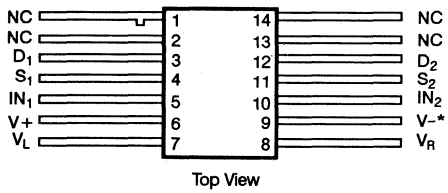


Order Numbers:

Side Braze:

DG186AP/883, DG186BP
DG187AP, DG187AP/883, DG187BP
DG188AP, DG188AP.883, DG188BP

Flat Package

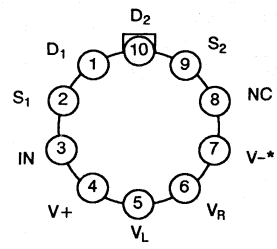


Top View

Order Numbers:

Refer to JAN38510 (page 1-7)

Top View



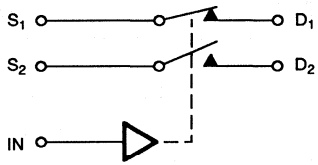
Metal Can Package

Order Numbers:

DG186AA/883, DG186BA
DG187AA, DG187AA/883, DG187BA
DG188AA, DG188AA.883, DG188BA

*Common to Substrate and Case

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



One SPDT Switch per Package

Truth Table*

Logic	SW 1	SW 2
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 36 V
V+ to V_D ..... 33 V
V_D to V- ..... 33 V
V_D to V_D ..... ±22 V
V_L to V- ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V- ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG186 ..... 200 mA
Current (S or D) DG187, DG188 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
Power Dissipation*
Metal Can** ..... 450 mW
14-Pin DIP*** ..... 825 mW
Flat Pack**** ..... 900 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a] (DG186)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	7.5		10 20		15 25	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.05		10 1000		15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		10 1000		15 300	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$		V_D = V_S = -7.5 V	Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration		Room	300					mA

SPECIFICATIONS[a] (DG186)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	240		400		425	ns
Turn-OFF Time	t_{OFF}			Room	140		200		225	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	21					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	17					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	17					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>55					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room			0.8		0.8	mA
Negative Supply Current	I-			Room		-3		-3		
Logic Supply Current	I_L			Room			3.2		3.2	
Reference Supply Current	I_R			Room		-2		-2		

SPECIFICATIONS[a] (DG187)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[e]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	22		30 60		50 75	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.06		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.13		1 100		5 100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		1 100		5 100	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		1 100		5 100	

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Siliconix incorporated

SPECIFICATIONS[a] (DG187)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 0.8 V or 2 V[e]		Room Hot	-0.02	-2 -200		-10 -200		nA
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-OFF Time	t_{OFF}			Room	95		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room			0.8		0.8	mA
Negative Supply Current	I-			Room		-3		-3		
Logic Supply Current	I_L			Room			3.2		3.2	
Reference Supply Current	I_R			Room		-2		-2		

SPECIFICATIONS[a] (DG188)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-10	15	-10	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	35		75 150		100 150	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.07		1 100		5 100	

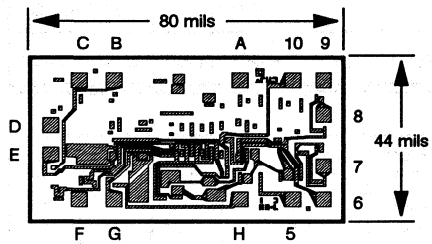
SPECIFICATIONS[a] (DG188)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 0.8 V or 2 V[e]	V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		1 100		5 100	nA
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.05		1 100		5 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 2 V		Room Hot	-0.03	-2 -200		-10 -200		
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	120		250		300	ns
Turn-OFF Time	t_{OFF}			Room	100		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room			0.8		0.8	mA
Negative Supply Current	I-			Room		-3		-3		
Logic Supply Current	I_L			Room			3.2		3.2	
Reference Supply Current	I_R			Room		-2		-2		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = Input voltage to perform proper function.
f. Room = 25°C, Hot and Full = as determined by the operating temperature suffix.

5

DIE TOPOGRAPHY (DRIVER)



Pad No.	Function
5	IN_1
6	V+
7	V_L
8	V_R
9	Not Connected
10	V- (Substrate

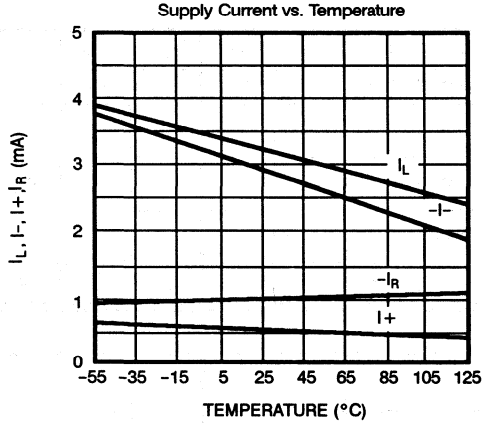
Interchip Pad Connections

A	Not Connected
B	From JFET 2, Source
C	Not Connected
D	Not Connected
E	To JFET 2, Gate
F	Not Connected
G	To JFET 1, Gate
H	From JFET 1, Source

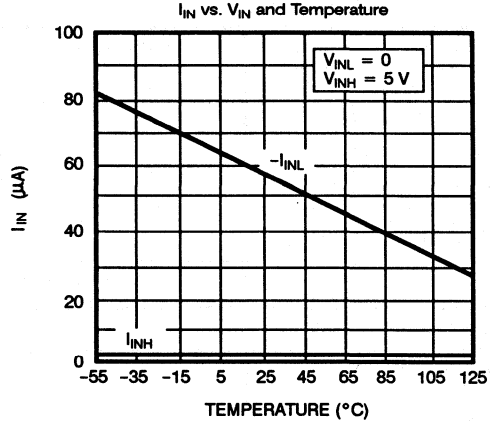
CMJC
4 Capacitors
4 Resistors
6 p-channel Depletion MOSFETs
4 n-channel Depletion MOSFETs
5 PNP bipolar Transistors
4 NPN bipolar Transistors
4 Diodes

TYPICAL CHARACTERISTICS

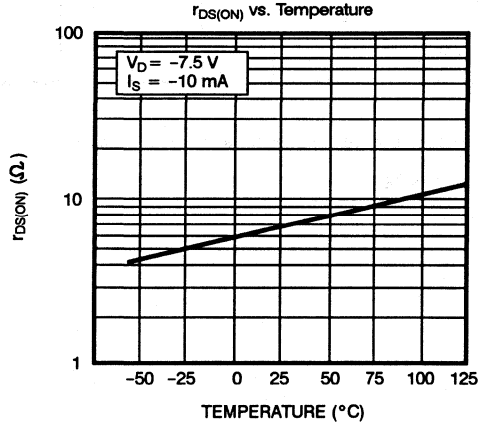
Supply Current vs. Temperature



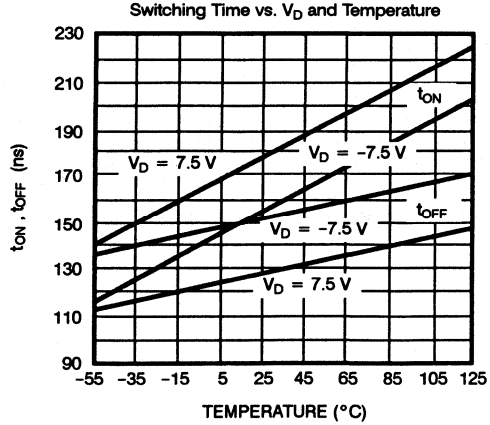
I_{IN} vs. V_{IN} and Temperature



10 Ω DG186
$r_{DS(ON)}$ vs. Temperature

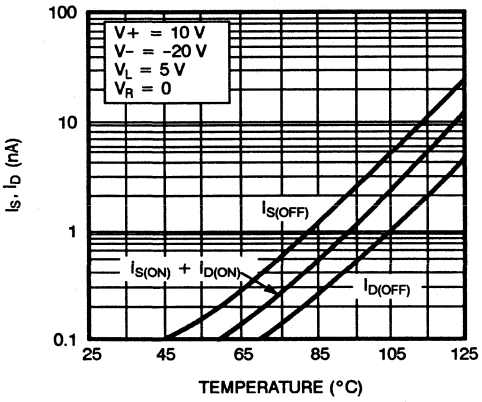


10 Ω DG186
Switching Time vs. V_D and Temperature

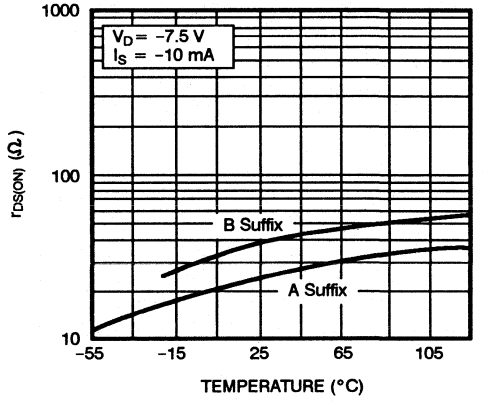


TYPICAL CHARACTERISTICS (Cont'd)

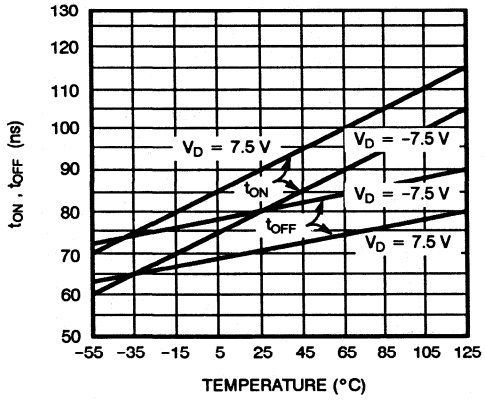
10 Ω DG186
Leakage vs. Temperature



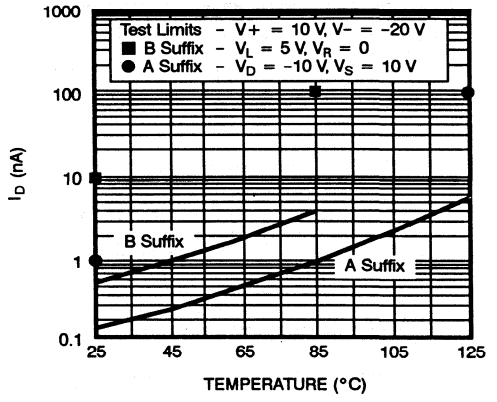
30 Ω DG187
$r_{DS(ON)}$ vs. Temperature



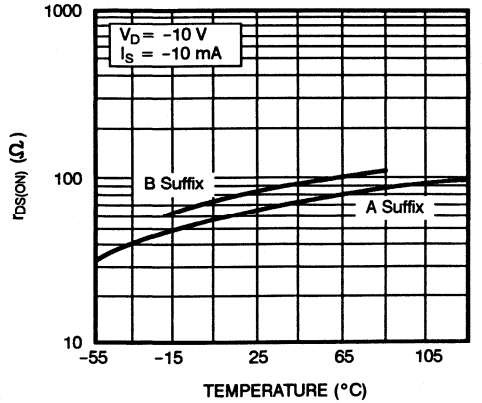
30 Ω DG187
Switching Time vs. V_D and Temperature



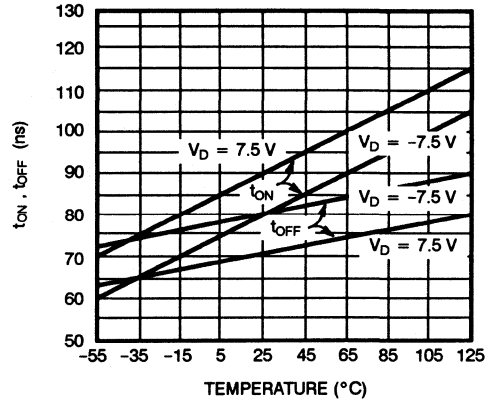
30 Ω DG187
$I_{D(OFF)}$ vs. Temperature



75 Ω DG188
$r_{DS(ON)}$ vs. Temperature



75 Ω DG188
Switching Time vs. V_D and Temperature



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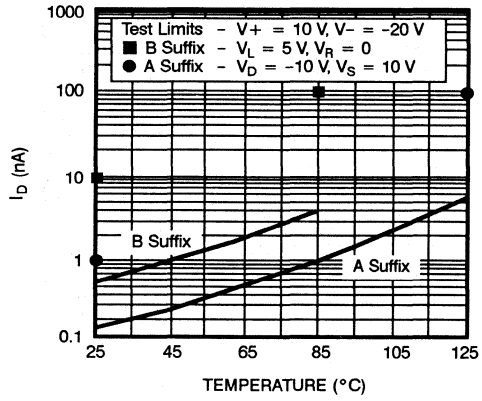
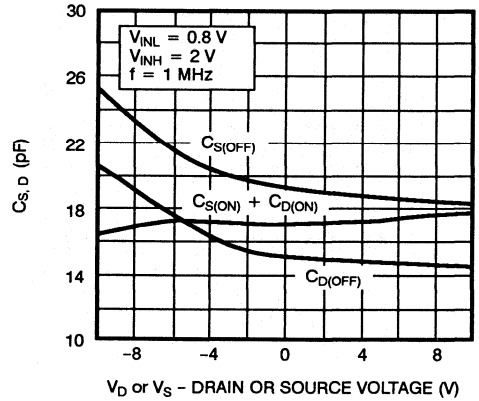
TYPICAL CHARACTERISTICS (Cont'd)

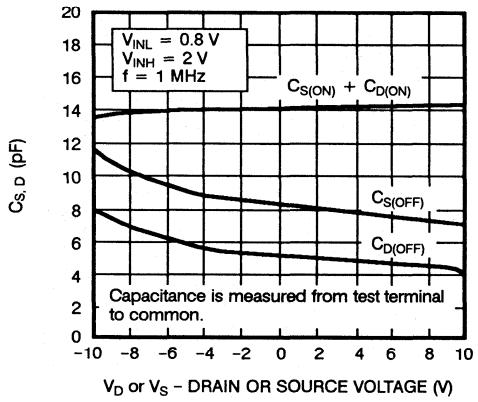
75 Ω DG188
$I_{D(OFF)}$ vs. Temperature



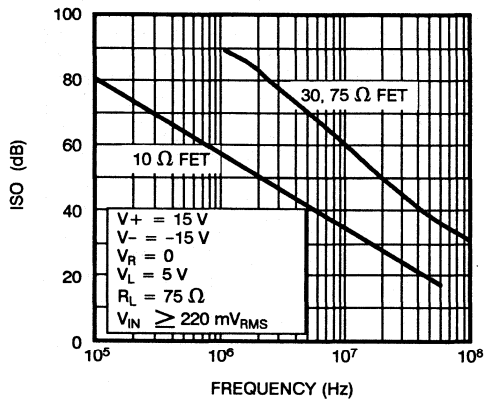
Capacitance vs. V_D or V_S (10 Ω FET)



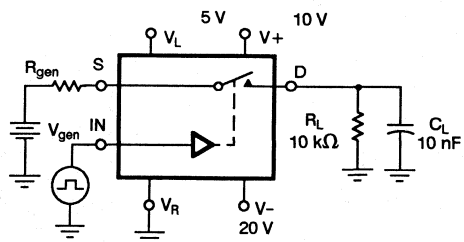
Capacitance vs. V_D or V_S (30 – 75 Ω FET)



OFF Isolation vs. Frequency



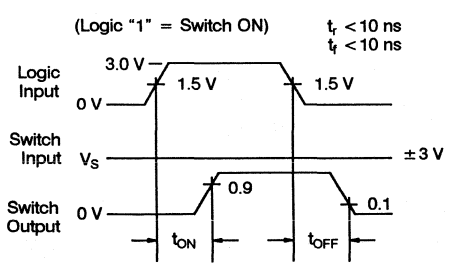
Typical delay, rise, fall settling times, and switching transients in this circuit.



If R_{gen}, R_L, or C_L is increased, there will be proportional increases in rise and/or fall times.

TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



Note:
Logic input waveform is inverted for switches that have the opposite logic sense control.

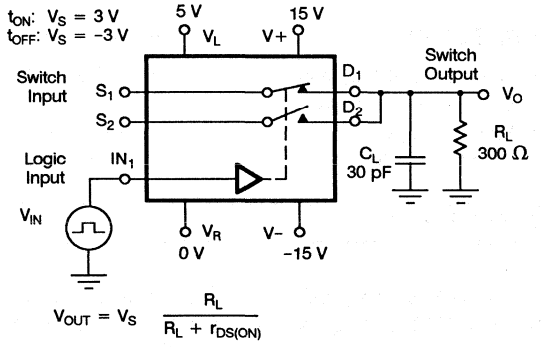


Figure 1. Switching Time

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

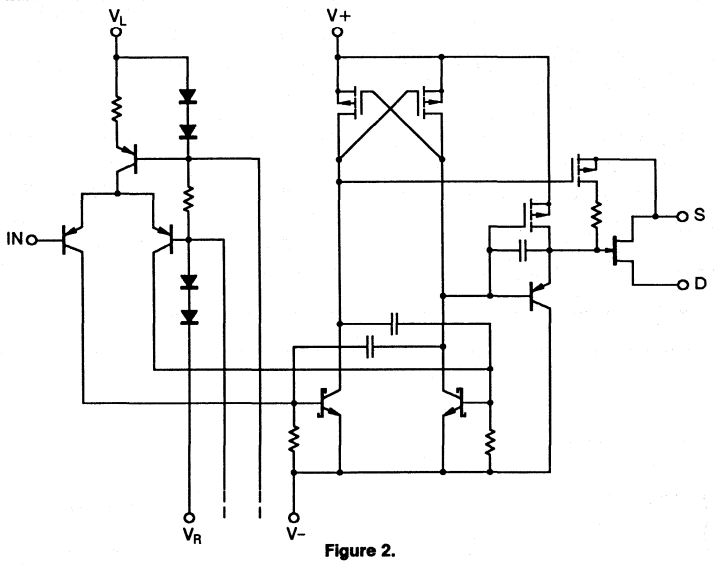


Figure 2.

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH}MIN/V_{INL}max (V)	V_S Analog Voltage Range (V)
10 Ω and 30 Ω	15**	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
75 Ω	15**	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

DG189/190/191
High-Speed Drivers with Dual SPDT JFET Switches

Siliconix incorporated

FEATURES

- Constant ON-Resistance Over Entire Analog Range
- Low Leakage
- Low Crosstalk

BENEFITS

- Low Distortion
- Eliminates Large Signal Errors
- High Bandwidth Capability

APPLICATIONS

- Audio Switching
- Video Switching
- Sample/Hold
- D/A Ladder Switches

DESCRIPTION

The DG189-191 are precision dual single-pole, double-throw (SPDT) analog switches designed to provide accurate switching of video and audio signals. This series, like the entire DG180 family, is ideally suited for applications requiring a constant ON-resistance over the entire analog range.

The major design difference is the ON-resistance, being 10, 30, and 75 Ω for the DG189, DG190, and DG191 respectively. Reduced switching errors are achieved through low leakage current ($I_{S(OFF)} < 1$ nA for the DG190/191). Applications which benefit from flat ON-resistance include audio switching, video switching, and sample and holds.

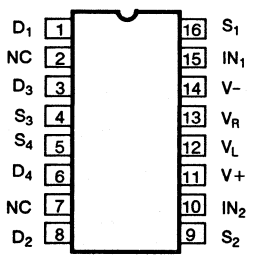
Each device comprises four n-channel JFET transistors and a bipolar driver (TTL compatible) to achieve fast and accurate switch performance. The driver is designed to achieve break-before-make switching action, eliminating the inadvertent shorting between channels and the crosstalk which would result. In the ON state, each switch conducts current equally well in either direction. In the OFF condition, the switches will block up to 20 V peak-to-peak, with feedthrough less than -60 dB at 10 MHz.

Packaging options for the DG189-191 include the 16-pin side braze, and the 14-pin flatpack. The flatpack version is only available for the DG190/191. Performance grades include both the military, A suffix (-55 to 125°C) and industrial, B suffix (-25 to 85°C) temperature ranges. The flatpack option is only available in the military grade.

PIN CONFIGURATION

Dual-In-Line Package

Top View

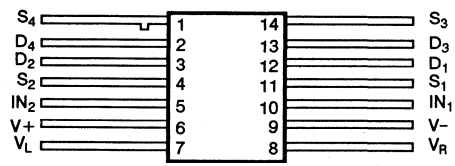


Order Numbers:

Side Braze:

DG189AP, DG189AP/883, DG189BP
DG190AP, DG190AP/883, DG190BP
DG191AP, DG191AP.883, DG191BP

Flat Package

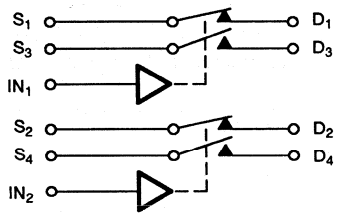


Top View

Order Numbers:

Refer to JAN38510 Information Chapter 1

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



Two SPDT Switches per Package*

Truth Table*

Logic	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 36 V
V+ to V_D ..... 33 V
V_D to V- ..... 33 V
V_D to V_D ..... ±22 V
V_L to V- ..... 36 V
V_L to V_{IN} ..... 8 V
V_L to V_R ..... 8 V
V_{IN} to V_R ..... 8 V
V_R to V- ..... 27 V
V_R to V_{IN} ..... 2 V
Current (S or D) DG180 ..... 200 mA
Current (S or D) DG181, DG182 ..... 30 mA
Current (All Other Pins) ..... 30 mA
Storage Temperature ..... -65 to 150°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
Power Dissipation*
16-Pin DIP** ..... 900 mW
Flat Pack*** ..... 900 mW

*All leads welded or soldered to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a] (DG189)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	7.5		10 20		15 25	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		10 1000		15 300	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.05		10 1000		15 300	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		10 1000		15 300	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.03		10 1000		15 300	
Channel ON Leakage Current	$I_{D(ON)} + I_{S(ON)}$		$V_D = V_S$ = -7.5 V	Room Hot	-0.1	-2 -200		-10 -200		
Saturation Drain Current	I_{DSS}	2 ms Pulse Duration		Room	300					mA

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Siliconix incorporated

SPECIFICATIONS[a] (DG189)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	240		400		425	ns
Turn-OFF Time	t_{OFF}			Room	140		200		225	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	21					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	17					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	17					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>55					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG190)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-7.5	15	-7.5	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	18		30 60		50 75	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.06		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.1		1 100		5 100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.06		1 100		5 100	

SPECIFICATIONS[a] (DG190)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 0.8 V or 2 V[e]		Room Hot	-0.02	-2 -200		-10 -200		nA
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	85		150		180	ns
Turn-OFF Time	t_{OFF}			Room	95		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

SPECIFICATIONS[a] (DG191)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-10	15	-10	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or 2 V[e]	I_S = -10 mA, V_D = -7.5	Room Full	35		75 150		100 150	Ω
Source OFF Leakage Current	$I_{S(OFF)}$		V_S = 10 V, V_D = -10 V V+ = 10 V, V- = -20 V	Room Hot	0.05		1 100		5 100	nA
			V_S = 7.5 V, V_D = -7.5 V	Room Hot	0.07		1 100		5 100	

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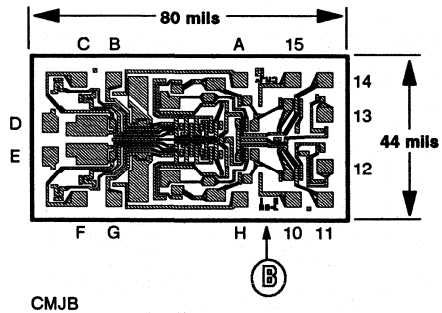
Siliconix incorporated

SPECIFICATIONS[a] (DG191)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_R = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B SUFFIX -25 to 85 °C MIN[b]	B SUFFIX -25 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 0.8 V or 2 V[e]	V_S = -10 V, V_D = 10 V V+ = 10 V, V- = -20 V	Room Hot	0.04		1 100		5 100	nA
			V_S = -7.5 V, V_D = 7.5 V	Room Hot	0.05		1 100		5 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = -7.5 V, V_{IN} = 2 V		Room Hot	-0.03	-2 -200		-10 -200		
DIGITAL INPUT										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room Hot	<0.01		10 20		10 20	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	-30	-250		-250		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	120		250		300	ns
Turn-OFF Time	t_{OFF}			Room	100		130		150	
Source-OFF Capacitance	$C_{S(OFF)}$	f = 1 MHz	V_S = -5 V, I_D = 0	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = -5 V, I_S = 0	Room	6					
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$		V_D = V_S = 0 V	Room	14					
OFF Isolation		f = 1 MHz, R_L = 75 Ω		Room	>50					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 0 V, or 5 V		Room	0.6		1.5		1.5	mA
Negative Supply Current	I-			Room	-2.7	-5		-5		
Logic Supply Current	I_L			Room	3.1		4.5		4.5	
Reference Supply Current	I_R			Room	-1	-2		-2		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = Input voltage to perform proper function.
f. Room = 25°C, Hot and Full = as determined by the operating temperature suffix.

DIE TOPOGRAPHY (DRIVER)



Pad No.	Function
10	IN_2
11	$V+$
12	V_L
13	V_R
14	$V-$ (Substrate)
15	IN_1

Interchip Pad Connections
With 2 JFET's

A	No Connection
B	No connection
C	To JFET 2, Gate
D	From JFET 2, Source
E	From JFET 1, Source
F	To JFET 1, Gate
G	No Connection
H	No Connection

With 4 JFET's

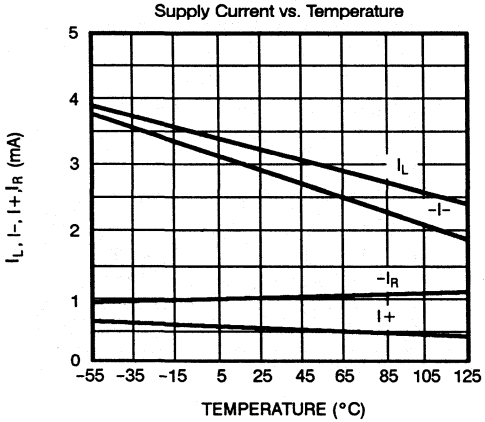
A	From JFET 1, Source
B	To JFET 1, Gate
C	To JFET 3, Gate
D	From JFET 3, Source
E	From JFET 4, Gate
F	To JFET 4, Gate
G	To JFET 2, Gate
H	From JFET 2, Source

CMJB
8 Capacitors
7 Resistors
12 p-channel Depletion MOSFETs
4 n-channel Depletion MOSFETs

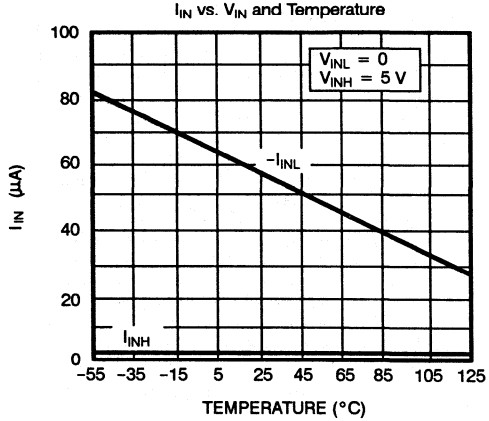
10 PNP bipolar Transistors
4 NPN bipolar Transistors
4 Diodes

TYPICAL CHARACTERISTICS

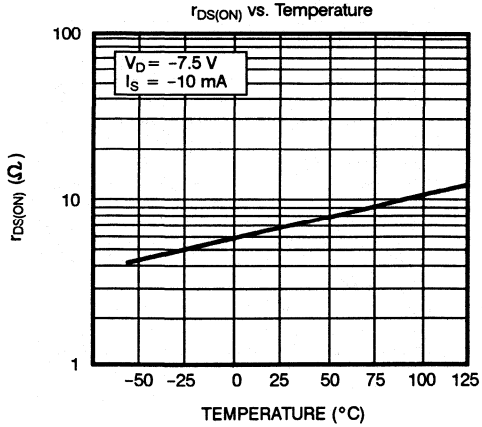
Supply Current vs. Temperature



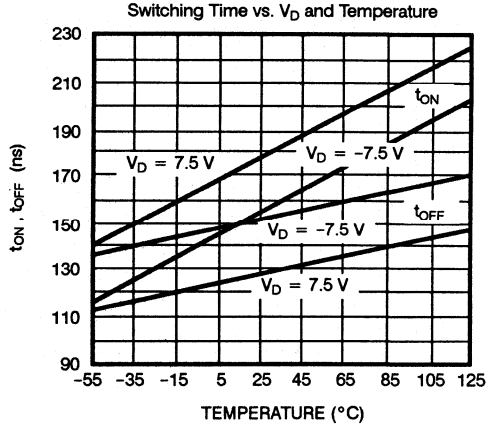
I_{IN} vs. V_{IN} and Temperature



10 Ω DG189
$r_{DS(ON)}$ vs. Temperature



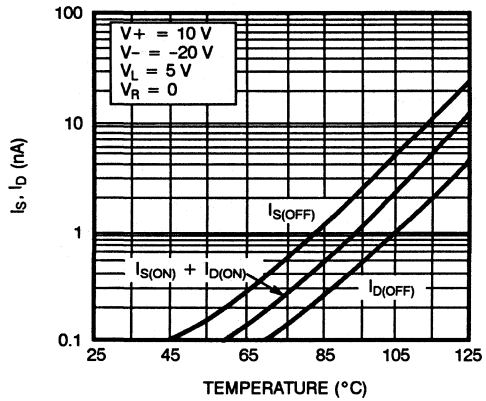
10 Ω DG189
Switching Time vs. V_D and Temperature



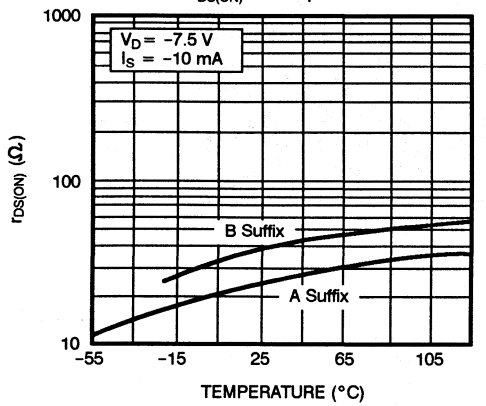
5

TYPICAL CHARACTERISTICS (Cont'd)

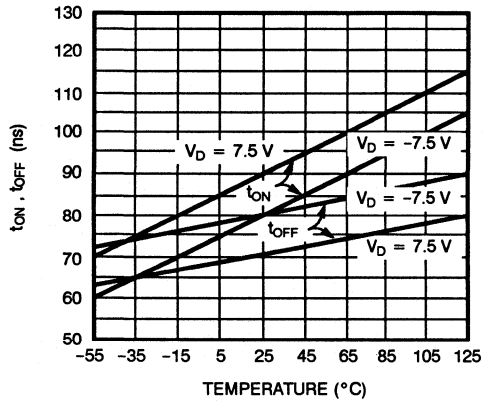
10 Ω DG189
Leakage vs. Temperature



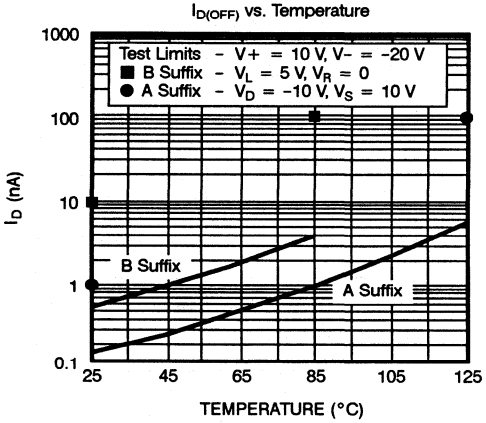
30 Ω DG190
$r_{DS(ON)}$ vs. Temperature



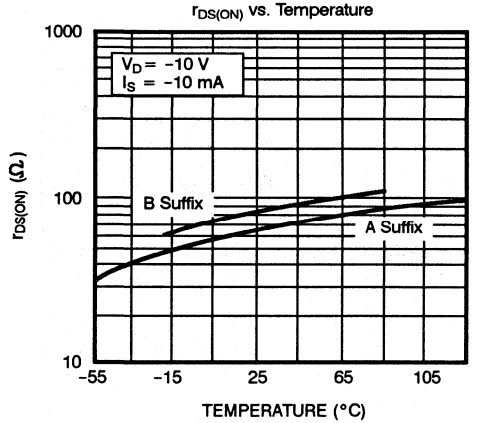
30 Ω DG190
Switching Time vs. V_D and Temperature



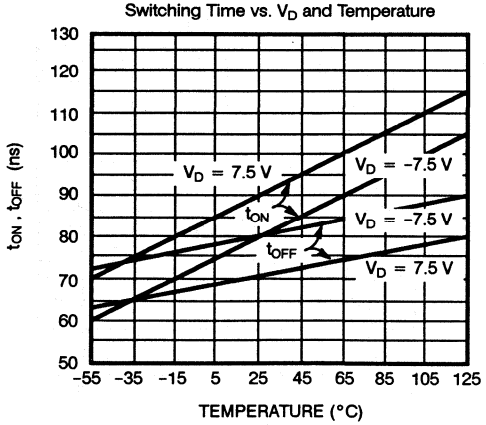
30 Ω DG190
$I_{D(OFF)}$ vs. Temperature



75 Ω DG191
$r_{DS(ON)}$ vs. Temperature

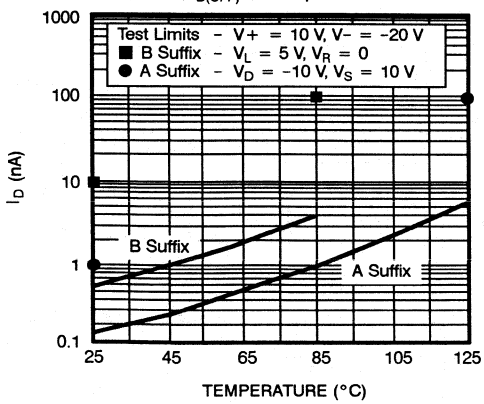


75 Ω DG191
Switching Time vs. V_D and Temperature

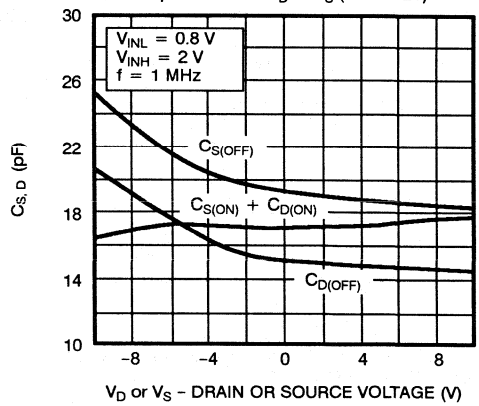


TYPICAL CHARACTERISTICS (Cont'd)

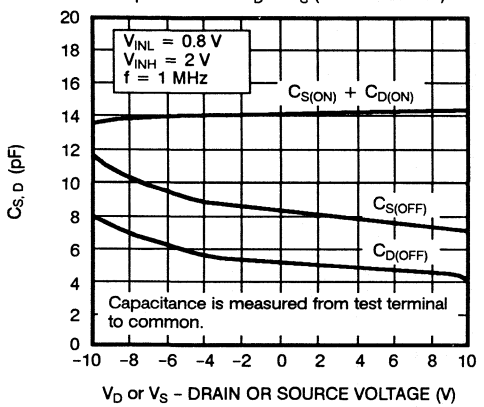
75 Ω DG191
$I_{D(OFF)}$ vs. Temperature



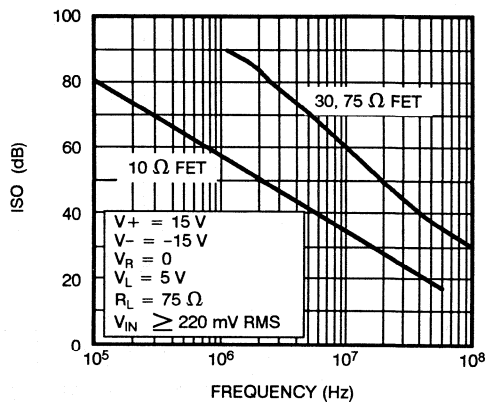
Capacitance vs. V_D or V_S (10 Ω FET)



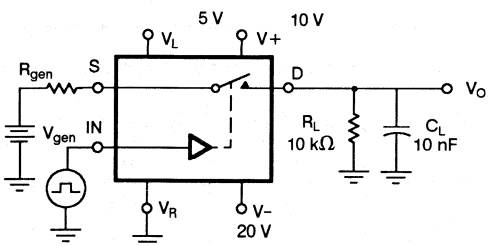
Capacitance vs. V_D or V_S (30 - 75 Ω FET)



OFF Isolation vs. Frequency



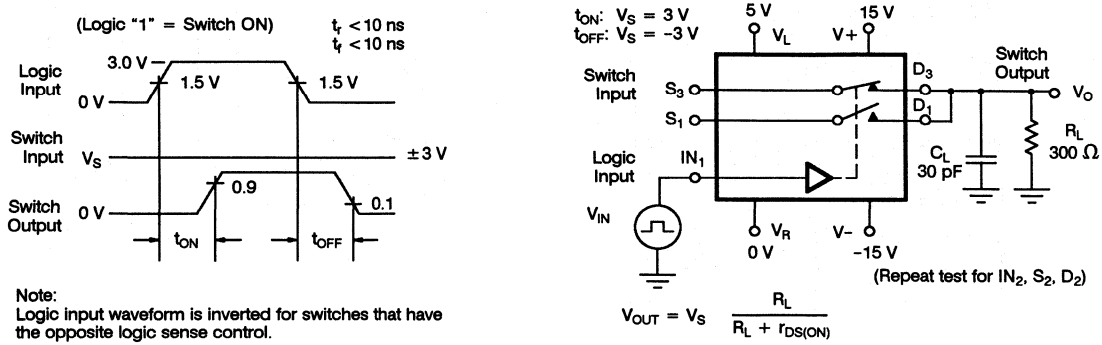
Typical delay, rise, fall settling times, and switching transients in this circuit.



If $R_{gen,}$, R_L, or C_L is increased, there will be proportional increases in rise and/or fall times.

TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



Note:
Logic input waveform is inverted for switches that have the opposite logic sense control.

Figure 1. Switching Time

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

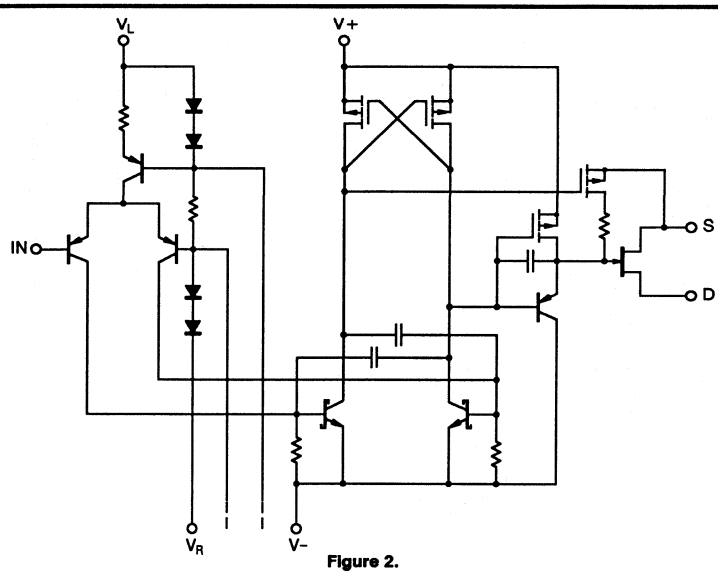


Figure 2.

APPLICATION HINTS*

Switch Family	V+ Positive Supply Voltage (V)	V− Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_R Reference Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH}MIN/V_{INL}max (V)	V_S Analog Voltage Range (V)
10 Ω and 30 Ω	15**	−15	5	GND	2.0/0.8	−7.5 to 15
	10	−20	5	GND	2.0/0.8	−12.5 to 10
	12	−12	5	GND	2.0/0.8	−4.5 to 12
75 Ω	15**	−15	5	GND	2.0/0.8	−10 to 15
	10	−20	5	GND	2.0/0.8	−15 to 10
	12	−12	5	GND	2.0/0.8	−7 to 12

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Electrical Parameter Chart based on V+ = 15 V, V_L = 5 V, V_R = GND

Siliconix incorporated

DG200A
Dual Monolithic SPST CMOS Analog Switch

FEATURES

- ±15 V Input Signal Range
- 44 V Maximum Supply Ratings
- ON-Resistance <70 Ω
- TTL and CMOS Compatibility
- 2500 V ESD Protection

BENEFITS

- Wide Dynamic Range
- Simple Interfacing
- Reduced External Component Count

APPLICATIONS

- Servo Control Switching
- Programmable Gain Amplifiers
- Audio Switching

DESCRIPTION

The DG200A is a dual, single-pole, single-throw analog switch designed to provide general purpose switching of analog signals. This device is ideally suited for designs requiring a wide analog voltage range coupled with low ON-resistance.

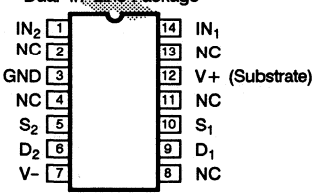
The DG200A is designed on Siliconix' improved PLUS-40 CMOS process which includes sandwich passivation and 2500 V ESD protection to MIL-M-3015.7 for ruggedness. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. In the ON condition, this bi-directional switch introduces no offset voltage of its own.

Packaging for the DG200A include a 14-pin CerDIP, metal can, and plastic DIP options. Performance grades include military, A suffix (–55 to 125°C), industrial, B suffix (–25 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges.

PIN CONFIGURATION

Dual-In-Line Package

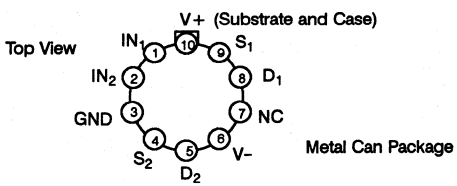


Top View

Order Numbers:

CerDIP: DG200AAK, DG200AAK/883
DG200ABK

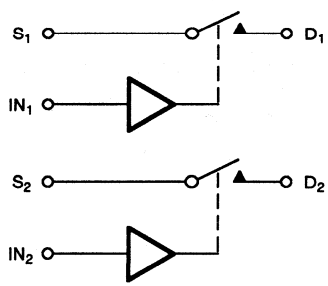
Plastic: DG200ACJ



Metal Can Package

Order Numbers:
DG200AAA, DG200AAA/883,
DG200ABA, JM38510/12301BIC

FUNCTIONAL BLOCK DIAGRAM



Two SPST Switches per Package*

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches Shown for Logic "1" Input

5

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
GND to V- ..... 25 V
Digital Inputs[1], V_S, V_D ..... (V-) -2 V to (V+) +2 V or ..... 30 mA, whichever occurs first.
Current (Any Terminal) Continuous ..... 30 mA
Current S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 100 mA
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C
Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C
Power Dissipation (Package)*
Metal Can** ..... 450 mW
14-Pin Ceramic DIP*** ..... 825 mW
14-Pin Plastic DIP**** ..... 470 mW

*All leads soldered or welded to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 11 mW/°C above 75°C.
****Derate 6.5 mW/°C above 25°C.

SPECIFICATIONS[a]

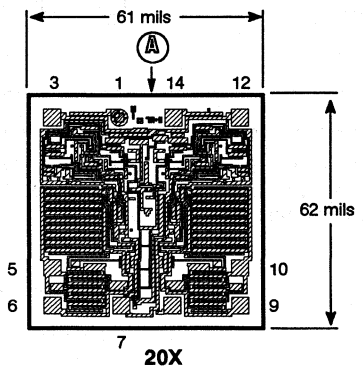
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, GND = 0 V		TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_D = ±10 V, V_{IN} = 0.8 V, I_S = -1 mA		Room Full	45		70 100		80 100	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2.4 V	V_S = 14 V, V_D = -14 V	Room Full	0.01		2 100		5 100	nA
			V_S = -14 V, V_D = 14 V	Room Full	-0.02	-2 -100		-5 -100		
Drain OFF Leakage Current	$I_{D(OFF)}$		V_D = 14 V, V_S = -14 V	Room Full	0.01		2 100		5 100	
			V_D = -14 V, V_S = 14 V	Room Full	-0.02	-2 -100		-5 -100		
Channel ON Leakage Current[f]	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 14 V, V_{IN} = 0.8 V		Room Full	0.1		2 200		5 200	
		V_S = V_D = -14 V, V_{IN} = 0.8 V		Room Full	-0.1	-2 -200		-5 -200		
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 2.4 V		Room Hot	0.0009	-0.5 -1		-1 -10		µA
		V_{IN} = 15 V		Room Hot	0.005		0.5 1		1 10	
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Room Hot	-0.0015	-0.5 -1		-1 -10		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	440		1000		1000	ns
Turn-OFF Time	t_{OFF}			Room	340		425		425	
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω		Room	-10					pC

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V	TEMP	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)									
Source-OFF Capacitance	$C_{S(OFF)}$	V_S = 0 V, V_{IN} = 5 V f = 140 kHz	Room	9					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_D = 0 V, V_{IN} = 5 V f = 140 kHz	Room	9					pF
Channel-ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_D = V_S = 0 V V_{IN} = 0 V	Room	25					pF
OFF Isolation[e]		V_{IN} = 5 V, Z_L = 75 Ω	Room	75					dB
Crosstalk (Channel-to-Channel)		V_S = 2 V, f = 1 MHz	Room	90					dB
POWER SUPPLIES									
Positive Supply Current	I+	Both Channels ON or OFF	Room	0.8		2		2	mA
Negative Supply Current	I-	V_{IN} = 0 V and 2.4 V	Room	-0.23	-1		-1		mA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. OFF isolation = 20 log V_S/V_D, V_S = input to OFF switch, V_D = output.
f. $I_{D(ON)}$ is leakage from driver into "ON" switch.
g. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY

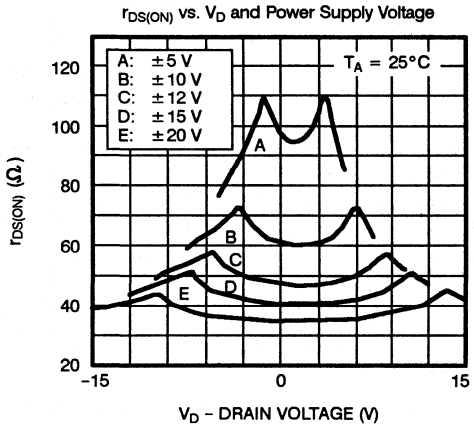


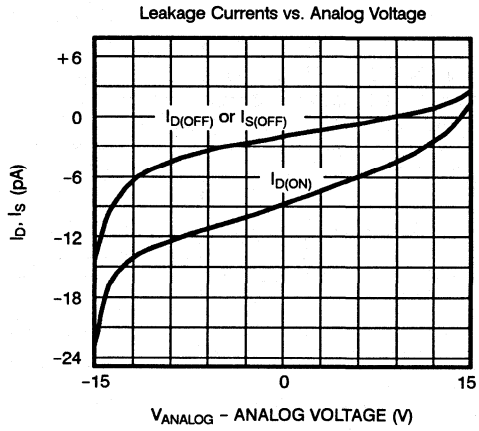
20X

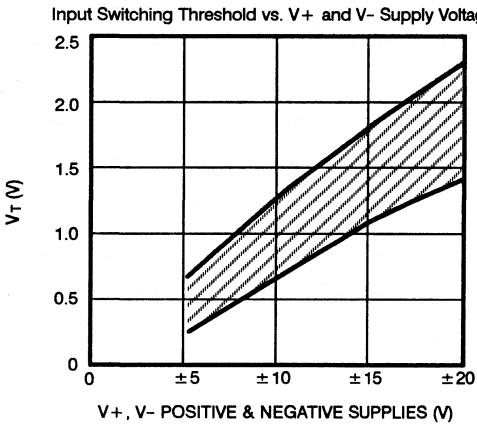
Pad No.	Function
1	Input 2
3	Ground
5	Source 2
6	Drain 2
7	V-
9	Drain 1
10	Source 1
12	V+ (Substrate)
14	Input 1

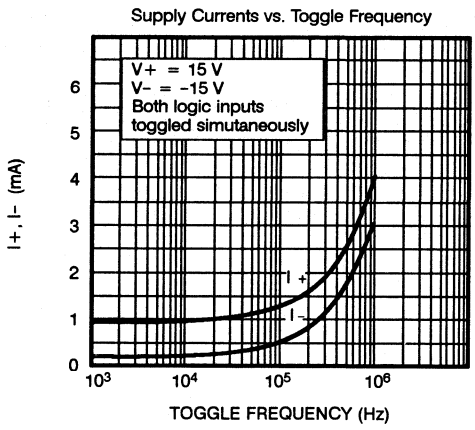
ICMEA
4 Capacitors
7 Resistors
25 p-channel enhancement MOSFETs
23 n-channel enhancement MOSFETs
8 Diodes

TYPICAL CHARACTERISTICS









TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveforms as shown. Note that V_S maybe + or - as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

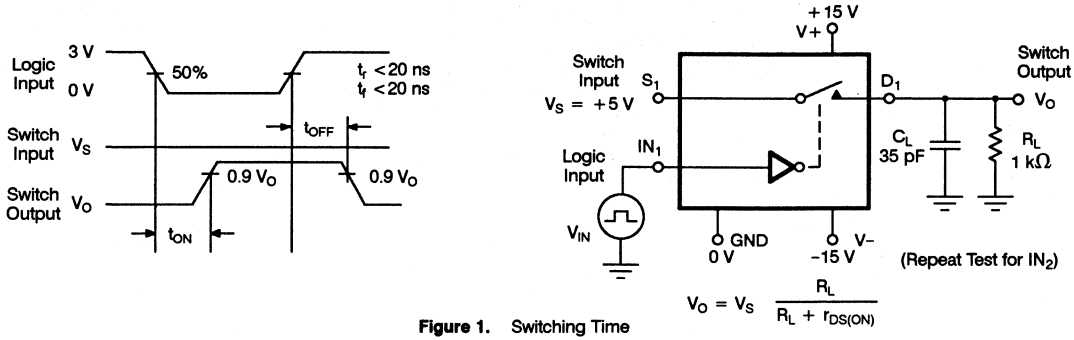
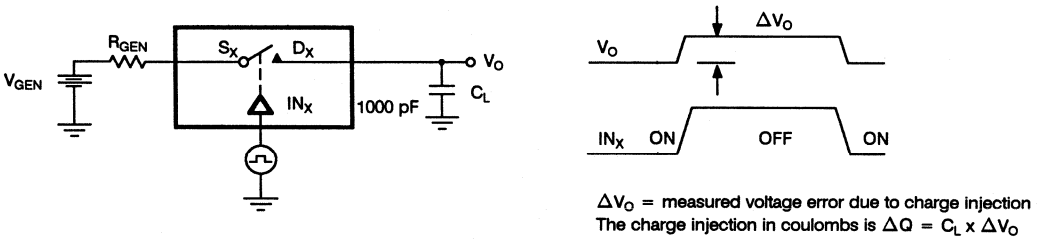


Figure 1. Switching Time

TEST CIRCUITS



ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$

Figure 2. Charge Injection

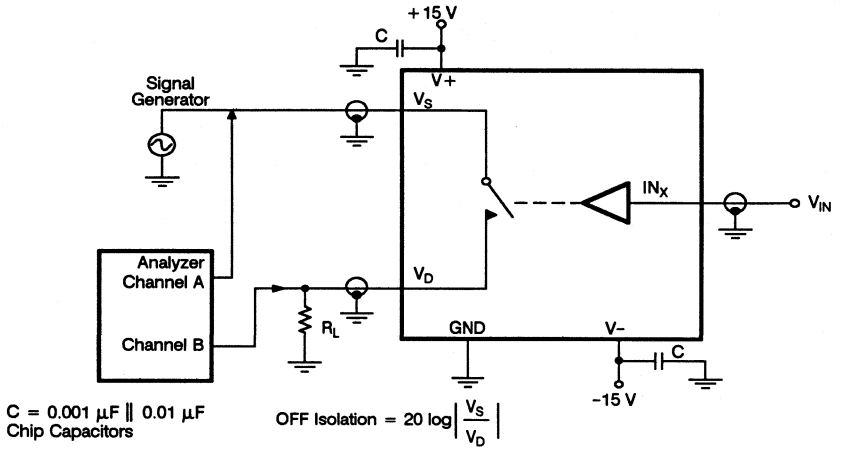


Figure 3. Off Isolation

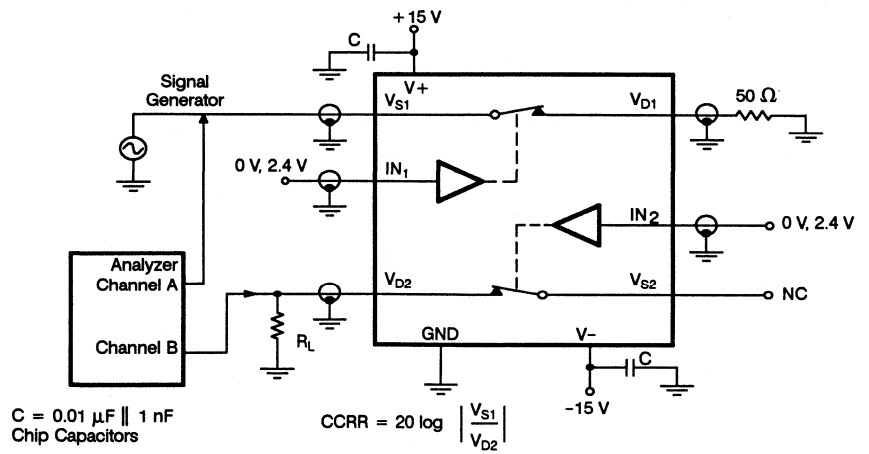


Figure 4. Channel-to-Channel Crosstalk

SCHEMATIC DIAGRAM (Typical Channel)

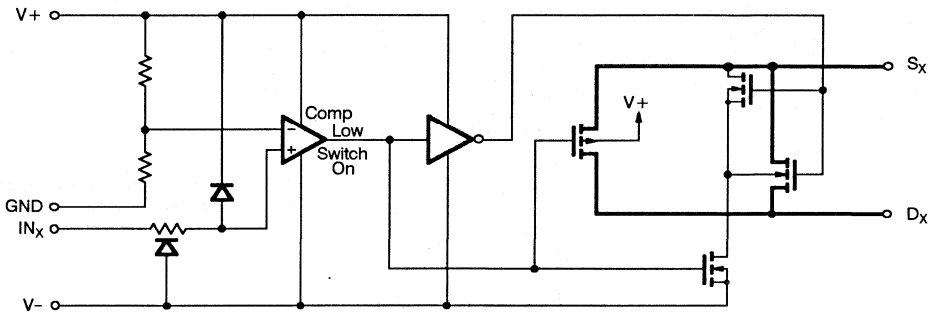
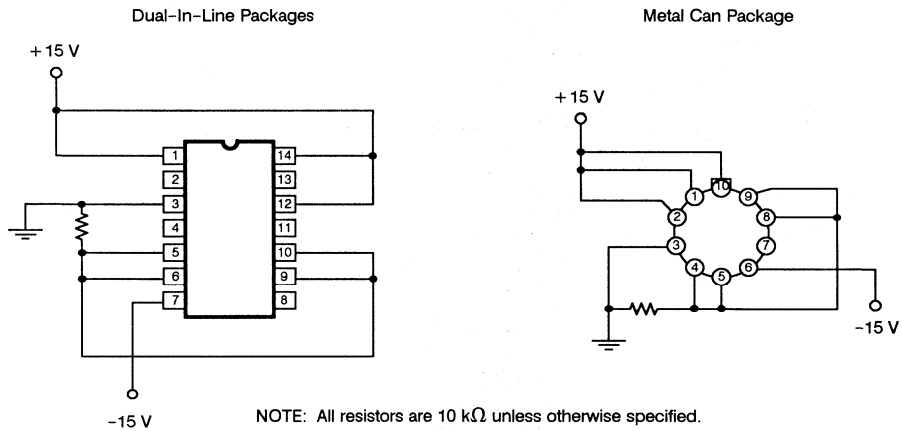


Figure 5.

BURN-IN CIRCUIT



NOTE: All resistors are 10 kΩ unless otherwise specified.

Figure 6.

DG201A/202

Quad Monolithic SPST CMOS Analog Switches

FEATURES

- ±15 Volt Input Range
- Low OFF Leakage ($I_{S(OFF)}$ 1 nA)
- Low On-resistance
- 44 V Maximum Supply Ratings
- TTL and CMOS Compatible
- Low Power Consumption
- Logic Inputs Accept Negative Voltages

BENEFITS

- Wide Input Range
- Low Distortion Switching
- Can be Driven from Comparators or Op Amps Without Limiting Resistors
- Multiple Sourced

APPLICATIONS

- Disk Drives
- Radar Systems
- Communications Systems
- Low Transient Sample/Holds

DESCRIPTION

The DG201A and DG202 are quad SPST analog switches designed to provide accurate switching over a wide range of input signals. By combining a low ON resistance and a wide signal range (±15 V) with low charge-transfer makes these devices well suited for industrial and military applications.

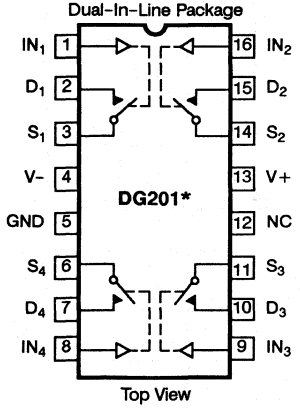
Built on Siliconix' high voltage metal gate process to achieve optimum switch performance, each switch conducts equally well in both directions when ON. When OFF these switches will block up to 30 V peak-to-peak and have a 44 V absolute maximum power supply rating. ON resistance is very flat over the full ±15 V analog range.

These two devices are differentiated by the type of switch actions, as shown in the functional block diagram. Package options for this series includes both the 16-pin plastic and CerDIP. Performance grades include the military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C), commercial, C suffix (0 to 70°C) and extended industrial, D suffix (-40 to 85°C) temperature ranges. Additionally, the DG201A is available in the 16-pin SO package. The DG441/DG442 upgrades are recommended for new designs.

5

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package

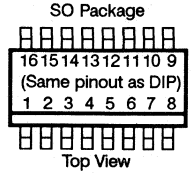


Top View

CerDIP: DG201AAK, DG201AAK/883
DG201ABK, DG201ACK
DG202AK/883

Plastic: DG201ACJ
DG202CJ

SO Package



Top View

Order Numbers:
DG201ADY

Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

*Switches shown for Logic "1" input

Siliconix incorporated

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[e] V_S, V_D ..... (V-) -2 V to (V+) +2 V
..... or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA
Storage Temperature (K, Z Suffix) ..... -65 to 150°C
(J, Y Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin CerDIP** ..... 900 mW
16-Pin Plastic Dip*** ..... 470 mW
20-Pin LCC**** ..... 750 mW
16-Pin SO***** ..... 640 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 25°C.
****Derate 10 mW/°C above 75°C.
*****Derate 7.6 mW/°C above 75°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = +15 V, V- = -15 V GND = 0		TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_D = ±10 V, I_S = 1 mA	V_{IN} = 0.8 V (DG201A)	Room	115		175		175	Ω
			V_{IN} = 2.4 V (DG202)	Full			250		250	
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2.4 V (DG201A), V_{IN} = 0.8 V (DG202)	V_S = 14 V, V_D = -14 V	Room Full	0.01		1 100		5 100	nA
			V_S = -14 V, V_D = 14 V	Room Full	-0.02	-1 -100		-5 -100		
Drain OFF Leakage Current	$I_{D(OFF)}$		V_D = 14 V, V_S = -14 V	Room Full	0.01		1 100		5 100	
			V_D = -14 V, V_S = 14 V	Room Full	-0.02	-1 -100		-5 -100		
Drain ON Leakage Current[f]	$I_{D(ON)}$	V_S = V_D = 14 V	V_{IN} = 0.8 V (DG201A)	Room Full	0.1		1 200		5 200	
			V_{IN} = 2.4 V (DG202)	Room Full	-0.15	-1 -200		-5 -200		
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 2.4 V		Room Full	-0.0004	-1 -1		-1 -10		µA
		V_{IN} = 15 V		Room Full	0.003		1 10		1 10	
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Room Full	-0.0004	-1 -10		-1 -10		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit		Room	480		600		600	ns
Turn-OFF Time	t_{OFF}			Room	370		450		450	

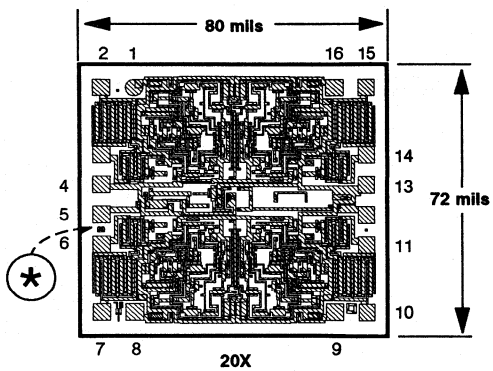
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = +15 V, V- = -15 V GND = 0	TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)									
Charge Injection	Q	C_L = 1000 pF, V_g = 0 V, R_g = 0 Ω	Room	20					pC
Source-OFF Capacitance	$C_{S(OFF)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room	5					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_S = 0 V, V_{IN} = 5 V, f = 1 MHz	Room	5					pF
Channel ON Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	V_D = V_S = 0 V, V_{IN} = 0 V, f = 1 MHz	Room	16					pF
OFF Isolation		V_{IN} = 5 V, Z_L = 75 Ω, V_S = 2 V, f = 100 kHz	Room	70					dB
Crosstalk (Channel-to-Channel)		V_{IN} = 5 V, Z_L = 75 Ω, V_S = 2 V, f = 100 kHz	Room	90					dB
POWER SUPPLY									
Positive Supply Current	I+	All Channels On or Off	Room	0.9		2		2	mA
Negative Supply Current	I-	All Channels On or Off	Room	-0.3	-1		-1		mA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
f. $I_{D(ON)}$ is leakage from driver to "ON" switch.
g. Room = 25°C, Full = as determined by the operating temperature suffix.

5

DIE TOPOGRAPHY



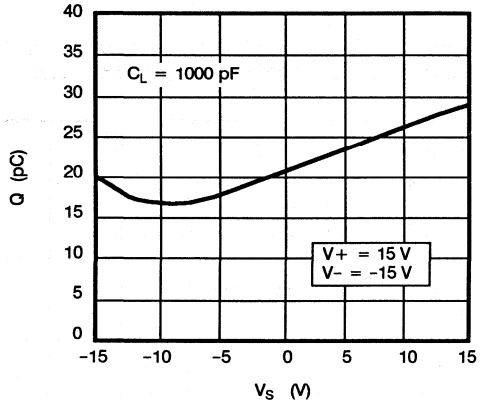
Pad No.	Function
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
12	NC
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

ICM*
8 Capacitors
9 Resistors
49 p-channel enhancement MOSFET
45 n-channel enhancement MOSFET

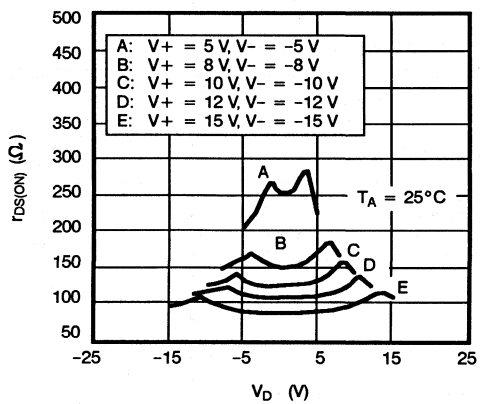
*B = DG201A
D = DG202

TYPICAL CHARACTERISTICS

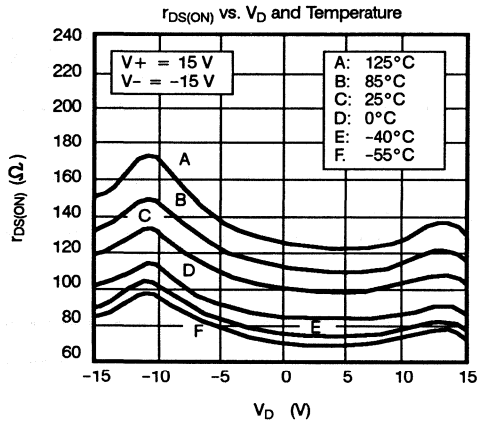
Charge Injection vs. Analog Voltage (V_S)



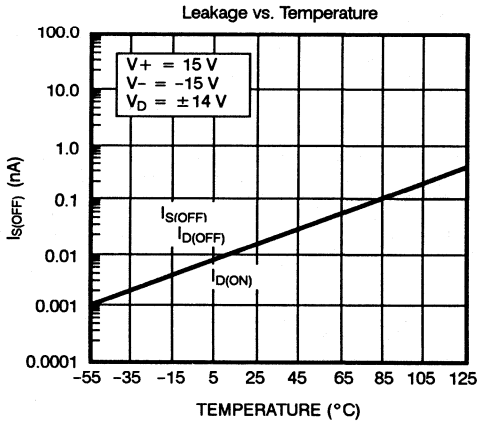
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



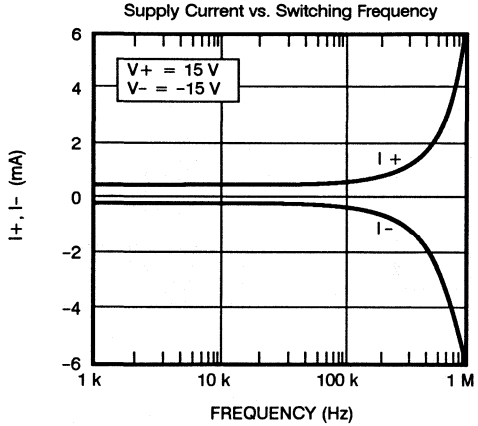
$r_{DS(ON)}$ vs. V_D and Temperature



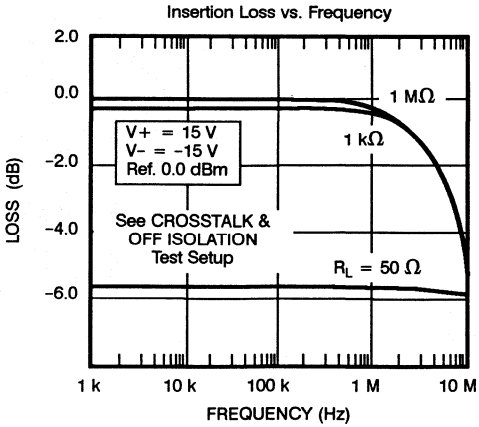
Leakage vs. Temperature



Supply Current vs. Switching Frequency

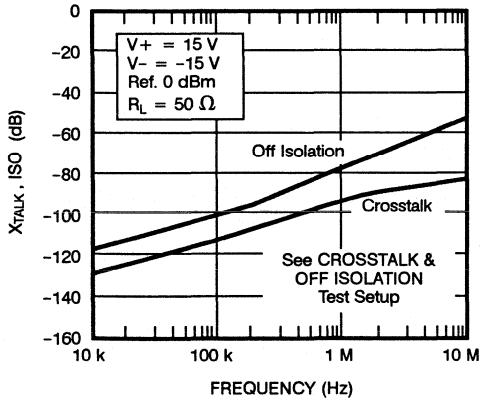


Insertion Loss vs. Frequency

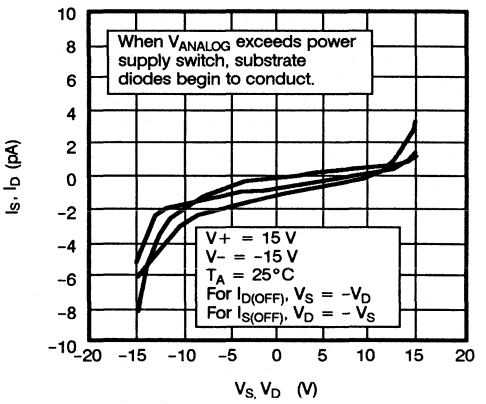


TYPICAL CHARACTERISTICS (Cont'd)

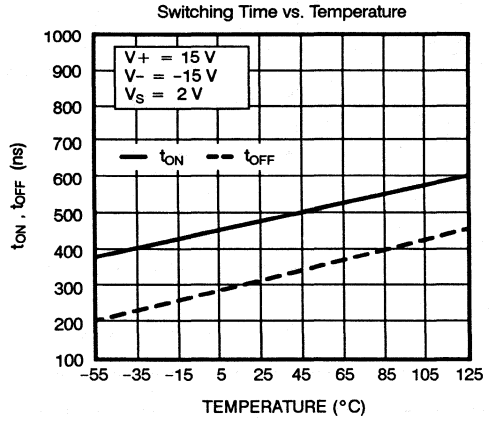
Crosstalk & Off Isolation vs. Frequency



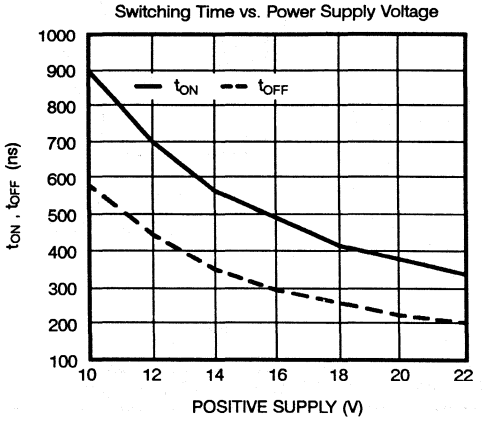
Leakage Current vs. Analog Voltage



Switching Time vs. Temperature

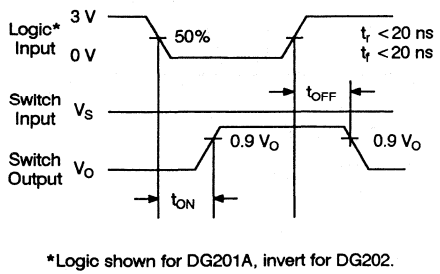


Switching Time vs. Power Supply Voltage

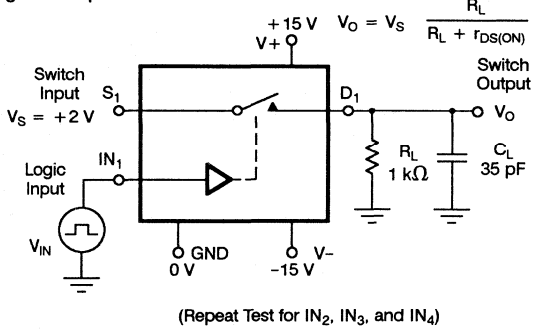


TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveforms as shown. Note that V_S maybe + or - as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



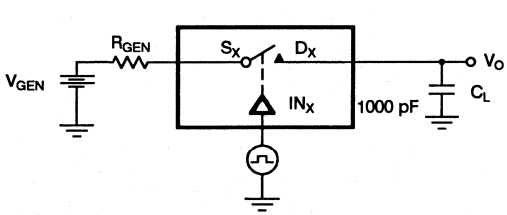
*Logic shown for DG201A, invert for DG202.

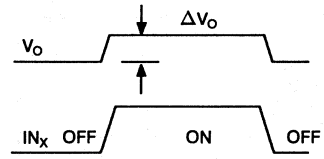


(Repeat Test for IN_2, IN_3, and IN_4)

Figure 1. Switching Times

TEST CIRCUITS (Cont'd)





ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$

Figure 2. Charge Injection

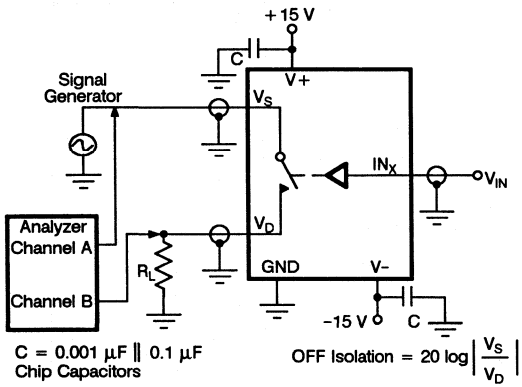


Figure 3. Off Isolation

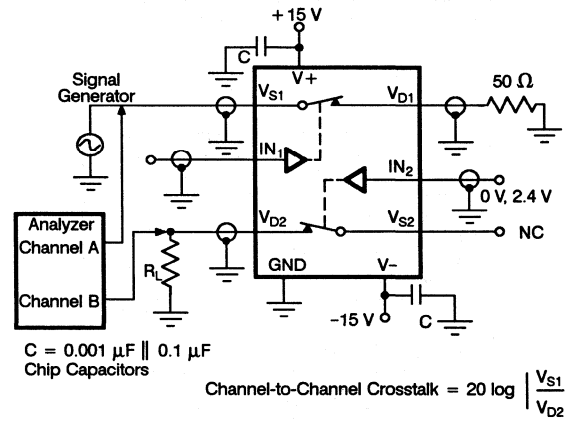


Figure 4. Channel-to-Channel Crosstalk

SCHEMATIC DIAGRAM (Typical Channel)

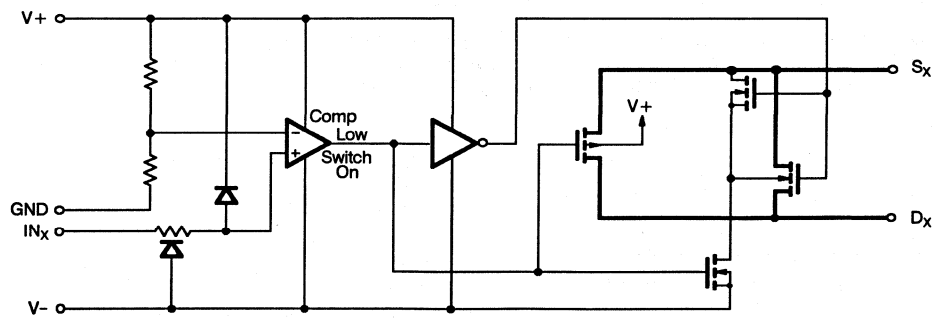


Figure 5.

APPLICATION HINTS*

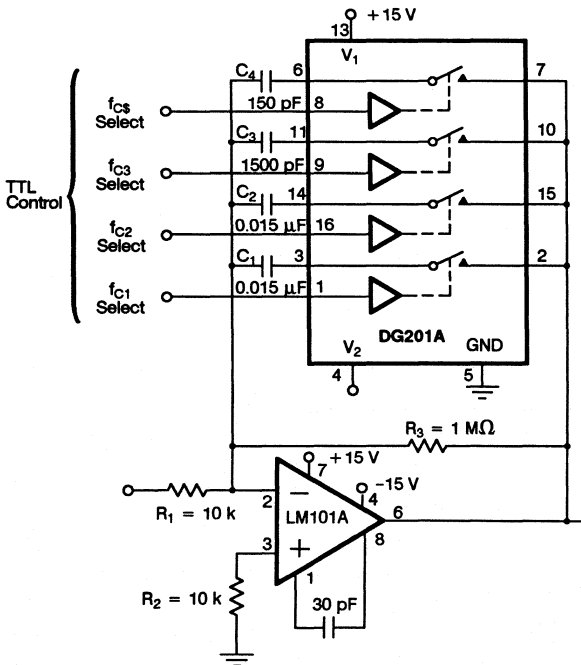
V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.2/0.6	-10 to10
8***	-8	2.0/0.5	-8 to 8

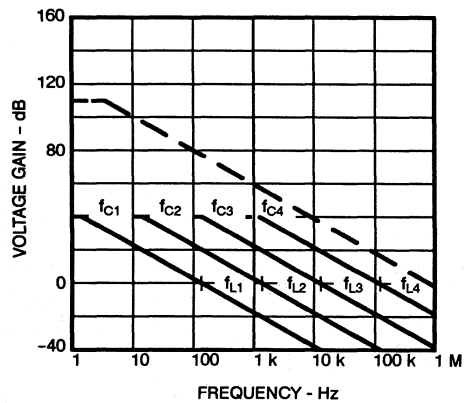
* Application Hints are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

** Specifications table based on V+ = 15 V, V- = -15 V.

*** Operation below ±8 V is not recommended.

APPLICATIONS





A_L (Voltage Gain Below Break Frequency) = $\frac{R_3}{R_1}$ = 100 (40 dB)

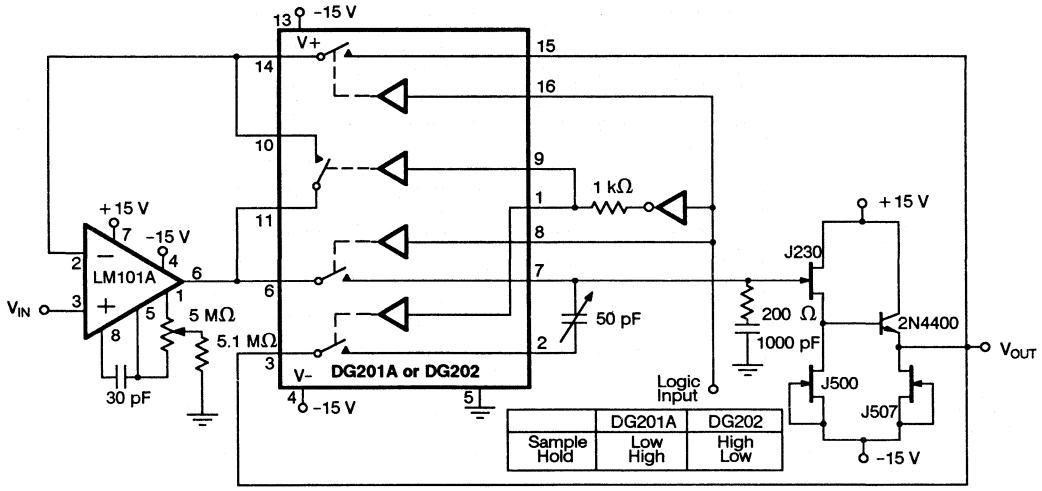
f_C (Break Frequency) = $\frac{1}{2\pi R_3 C_X}$

f_L (Unity Gain Frequency) = $\frac{1}{2\pi R_1 C_X}$

Max Attenuation = $\frac{r_{DS(ON)}}{10\text{ k}} \approx$ -40 dB

Figure 6. Active Low Pass Filter with Digitally Selected Break Frequency

5



Aquisition Time = 25 µS
Aperature Time = 1 µS
Sample to Hold Offset = 5 mV
Droop Rate = 5 mV/S

Figure 7. Sample-and-Hold

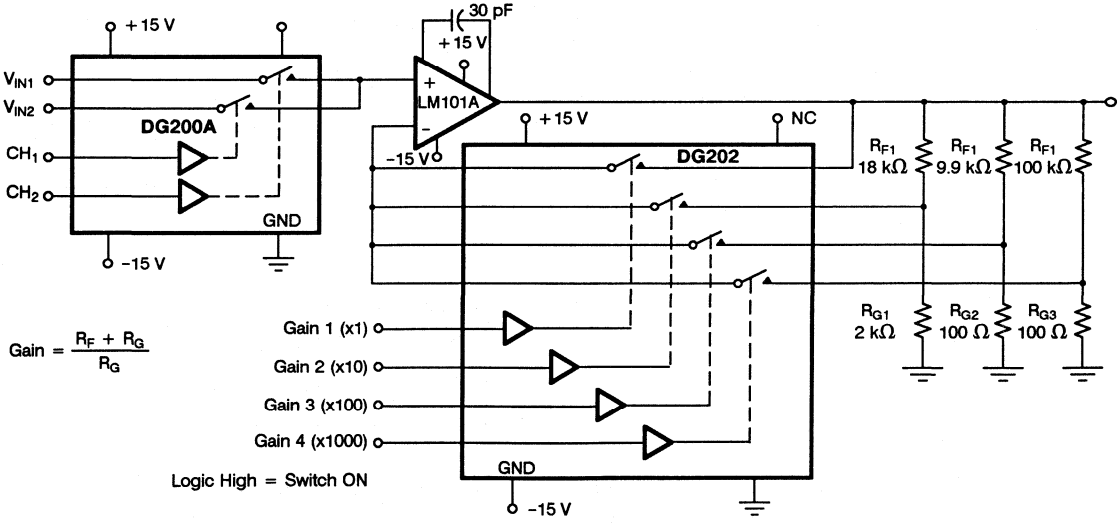


Figure 8. A Precision Amplifier with Digitally Programable Input and Gains

Siliconix incorporated

DG211/212

Low Cost 4-Channel Monolithic SPST CMOS Analog Switches

FEATURES

- ±15 V Analog Signal Range
- TTL Compatibility
- Logic Inputs Accept Negative Voltages
- ON-Resistance <175 Ω

BENEFITS

- Wide Signal Range
- Simple Logic Interface
- Reduced Power Consumption

APPLICATIONS

- Disk Drives
- Test Equipment
- Communication Systems

DESCRIPTION

The DG211 and DG2122 are low cost quad single-pole single-throw analog switches for use in general purpose switching applications in communication, instrumentation and process control. These devices differ only in that the digital control logic is inverted, as shown in the truth table. The use of both p- and n-channel devices minimizes ON-resistance variations over the analog signal range.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 40 V, both switches will handle ±15 V input signals with ease, and have a continuous current rating of 20 mA. An epitaxial layer prevents latchup.

Both devices feature true bi-directional performance (with no offset voltage) in the ON condition, and will block signals to 30 V peak-to-peak in the OFF condition.

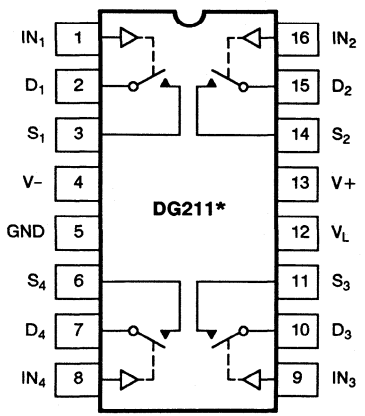
For new designs we recommend the silicon-gate DG444/445 upgrades.

Packaging for this series includes 16-pin plastic DIP and small outline options. Performance grades include both commercial, C suffix (0 to 70°C) and industrial, D suffix (–40 to 85°C) temperature ranges.

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLES

5

Dual-In-Line Package

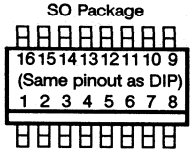


Top View

Order Numbers:
DG211CJ, DG212CJ

*Switches shown for Logic "1" input

SO Package



Top View

Order Numbers:
DG211DY, DG212DY

Truth Table

Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
V_{IN} to GND ..... V-, V+
V_L to GND ..... -0.3 V, 25 V
V_S or V_D to V+ ..... 0, -40 V
V_S or V_D to V- ..... 0, 40 V
V+ to GND ..... 25 V
V- to GND ..... -25 V
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature ..... -65 to 125°C
Operating Temperature (C Suffix) ..... 0 to 70°C
(D Suffix) ..... 40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 470 mW
16-Pin Small Outline*** ..... 600 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 6.5 mW/°C above 25°C.
***Derate 7.6 mW/°C above 75°C.

SPECIFICATIONS[a]

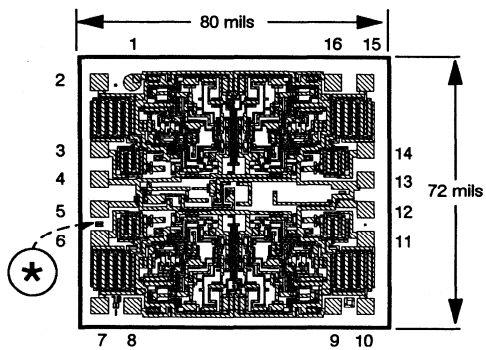
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = +15 V, V- = -15 V, V_L = 5 V GND = 0, V_{IN} = 2.4 V, 0.8 V[e]		TEMP[g]	C, D SUFFIX 0 to 70°C -40 to 85°C TYP[d]	MIN[b]	MAX[b]	UNIT
ANALOG SWITCH								
Analog Signal Range[d]	V_{ANALOG}			Full		-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V (DG211), 2.4 V (DG212) I_S = 1 mA, V_D = ±10 V			115		175	Ω
Source OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2.4 V (DG211)	V_S = 14 V, V_D = -14 V	25°C	0.01		5	nA
			V_S = -14 V, V_D = 14 V		-0.02	-5		
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 0.8 V (DG212)	V_D = 14 V, V_S = -14 V		0.01		5	
			V_D = -14 V, V_S = 14 V		-0.02	-5		
Drain ON Leakage Current[f]	$I_{D+S(ON)}$	V_{IN} = 0.8 V (DG211)	V_S = V_D = 14 V		0.1		5	
		V_{IN} = 2.4 V (DG212)	V_S = V_D = -14 V		-0.15	-5		
DIGITAL CONTROL								
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 2.4 V		25°C	-0.0004	-1		µA
		V_{IN} = 15 V			0.003		1	
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V			-0.0004	-1		
DYNAMIC CHARACTERISTICS								
Turn-ON Time	t_{ON}	See Switching Time Test Circuit, V_S = 2 V		25°C	460		1000	ns
Turn-OFF Time	t_{OFF1}				360		500	
	t_{OFF2}				450		450	
Source-OFF Capacitance[d]	$C_{S(OFF)}$	V_S = 0 V, V_{IN} = 5 V			5			pF
Drain-OFF Capacitance[d]	$C_{D(OFF)}$	f = 1 MHz			5			
Channel ON Capacitance[d]	C_{ON}	V_D = V_S = 0 V, V_{IN} = 0 V, f = 1 MHz			16			
OFF Isolation[f]		V_{IN} = 5 V, R_L = 1 kΩ			70			dB
Crosstalk (Channel-to-Channel)		C_L = 15 pF, V_S = 1 V_{RMS}, f = 100 kHz			90			

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = +15 V, V- = -15 V, V_L = 5 V GND = 0, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[g]	C, D SUFFIX 0 to 70°C -40 to 85°C TYP[d]	MIN[b]	MAX[b]	UNIT
POWER SUPPLIES							
Positive Supply Current	I+	V_{IN} = 0 or 5 V	25°C	0.35		0.48	mA
Negative Supply Current	I-			0.3		0.48	
Logic Supply Current	I_L			0.5		1.2	

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. OFF isolation = 20 log (V_{IN}/V_{OUT})
g. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
12	V_L
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

ICMC*
8 Capacitors
9 Resistors
49 p-channel enhancement MOSFET
45 n-channel enhancement MOSFET

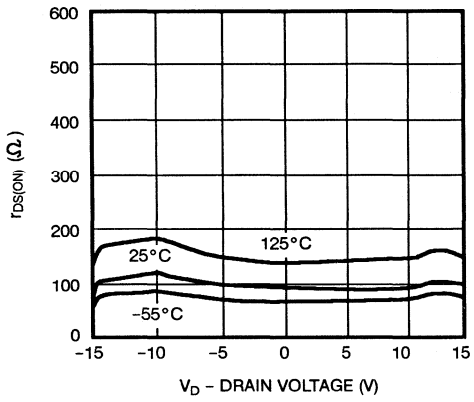
***A = DG211**
C = DG212

5

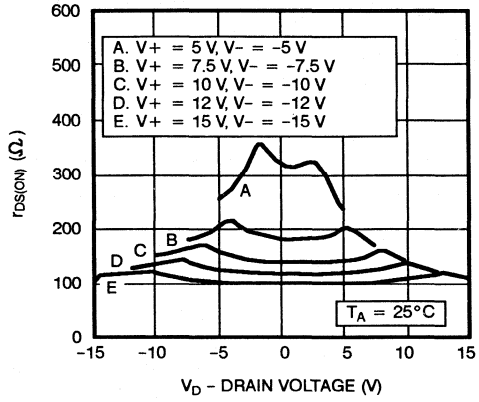
TYPICAL CHARACTERISTICS

The electrical characteristic table guarantees the DG211 and DG212 for operation at ±15 V, ±10%; however, functional operation occurs over the designed range of ±5 V to ± 20 V power supplies. These characteristic graphs show the effect of device parameters over several parameter permutations including power supply variations. These graphs are for design aid only and are not subject to production testing.

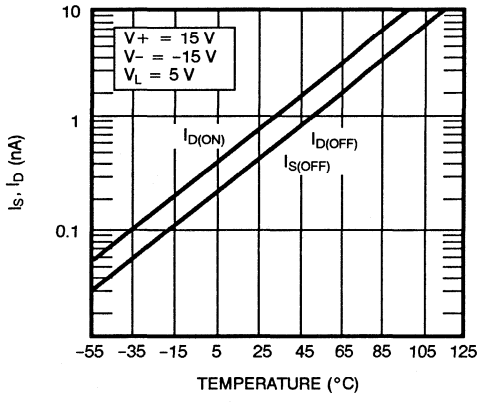
$r_{DS(ON)}$ vs. V_D and Temperature



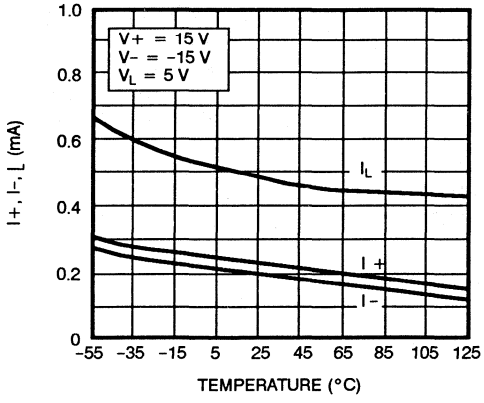
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



Leakage Currents vs. Temperature*



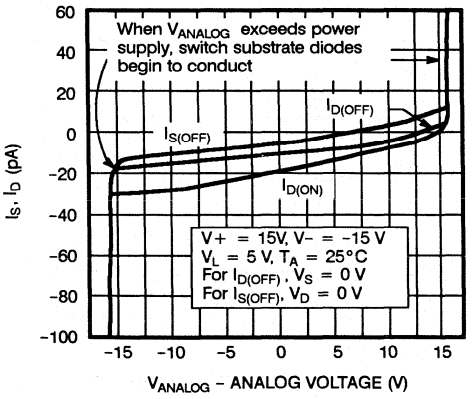
Supply Current vs. Temperature



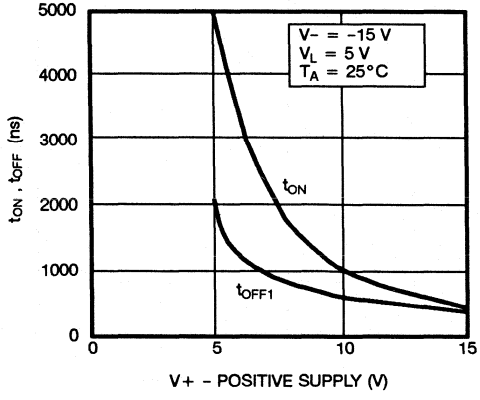
*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

TYPICAL CHARACTERISTICS (Cont'd)

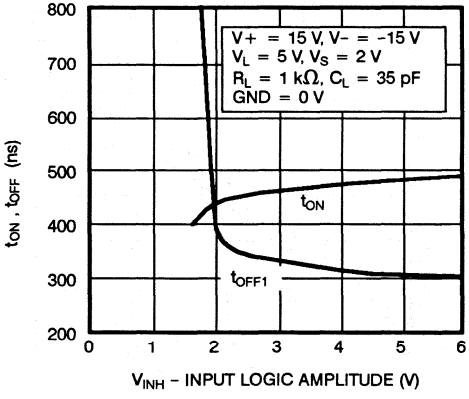
Leakage Current vs. Analog Voltage



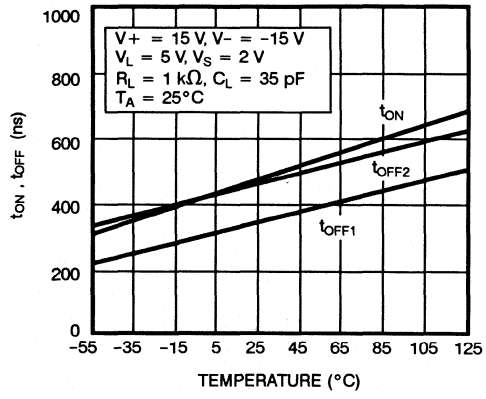
Switching Time vs. Positive Supply Voltage



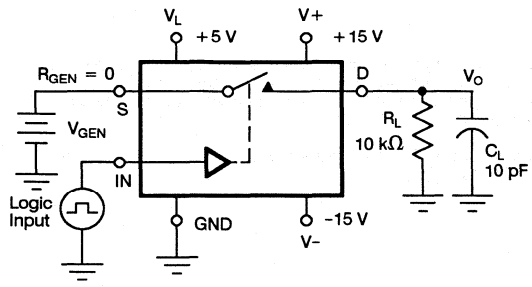
Switching Time vs. Input Logic Amplitude



Switching Time vs. Temperature

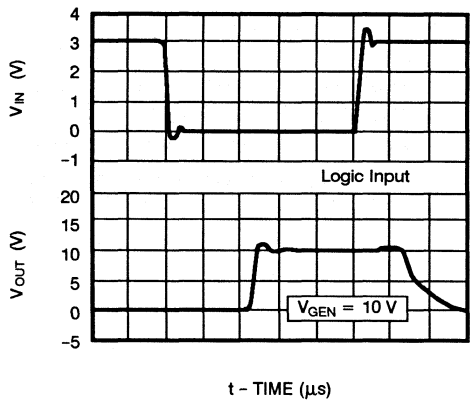


Typical delay, rise, fall settling times, and switching transients in this circuit.



If V_{GEN}, R_L, or C_L is increased, there will be a proportional increase in rise and/or fall RC times.

DG211



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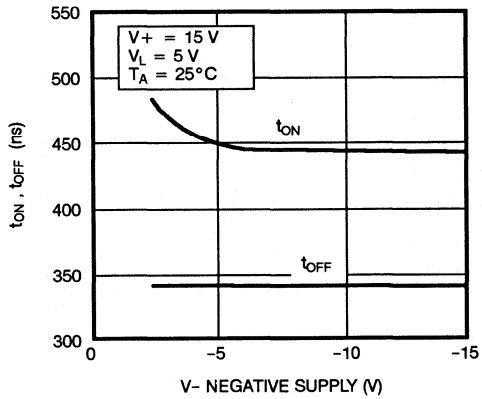
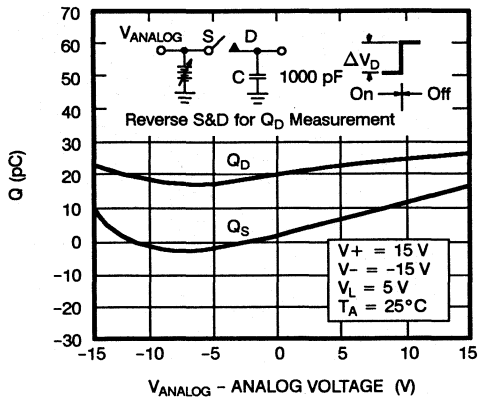
TYPICAL CHARACTERISTICS (Cont'd)

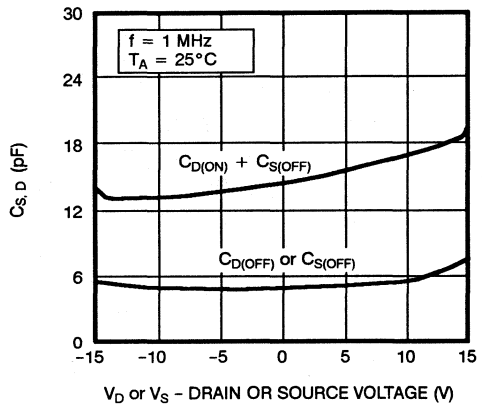
Switching Time vs. Negative Supply Voltage



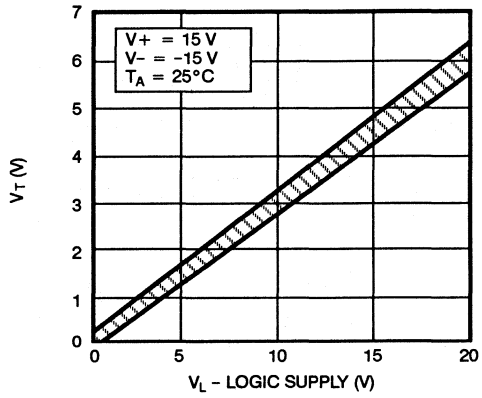
Charge Injection vs. Analog Voltage



Capacitance vs. V_D or V_S



Input Switching Threshold vs. Logic Supply Voltage

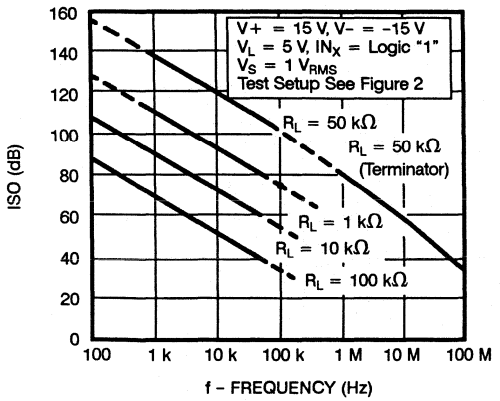


Some applications of the DG211 or DG212 will find the logic control inputs IN_X driven from the output of comparators or op-amps with nearly plus to minus 15 volt transitions. In these applications the user can shift the input logic transition voltage from the normal 1.6 V of TTL to zero volts by connecting the V_L pin to the GND pin. In this mode of operation the input offset voltage between IN_X and V_L (= GND) measure less than ±500 mV.

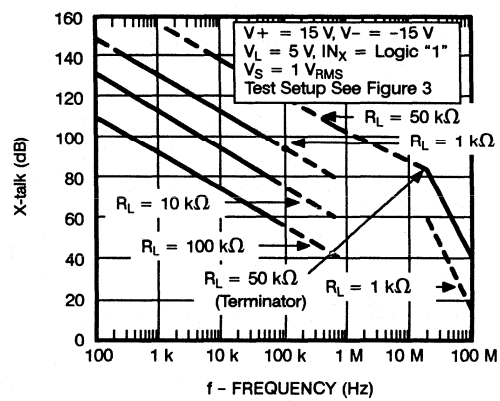
V_L = 5 V presets the input threshold voltage for TTL logic compatibility. Improved noise immunity for CMOS logic compatibility results by connecting V_L to the V_{DD} terminal of the CMOS logic.

TYPICAL CHARACTERISTICS (Cont'd)

OFF Isolation vs. Frequency



Channel-to-Channel Crosstalk vs. Frequency



TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

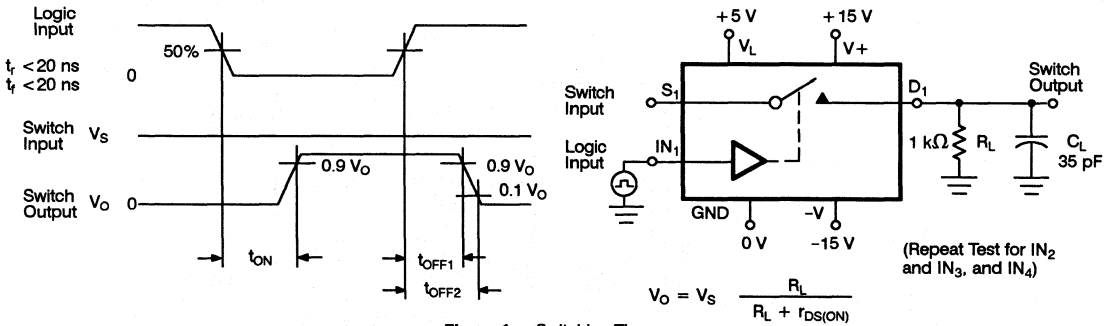


Figure 1. Switching Time

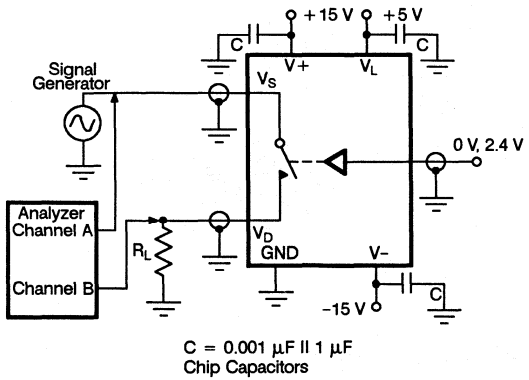


Figure 2. OFF Isolation vs. Frequency

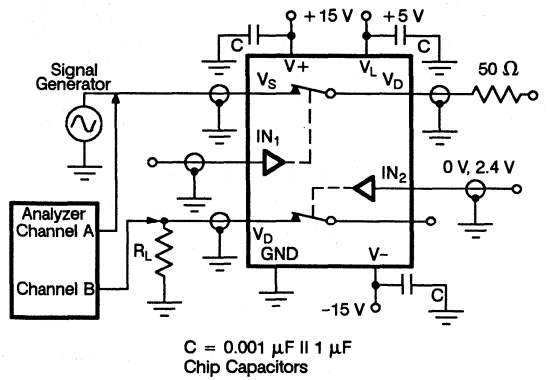


Figure 3. Crosstalk vs. Frequency

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

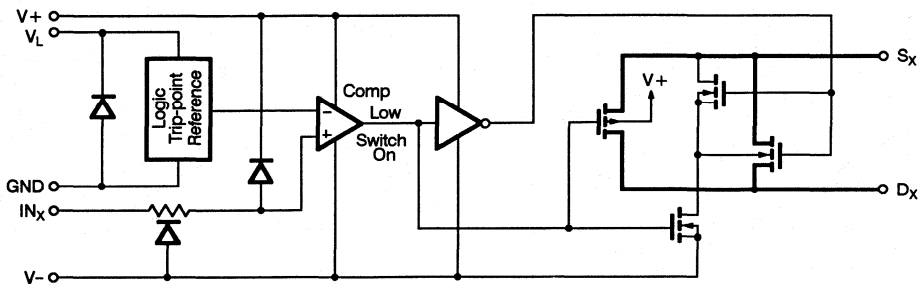


Figure 4.

APPLICATIONS

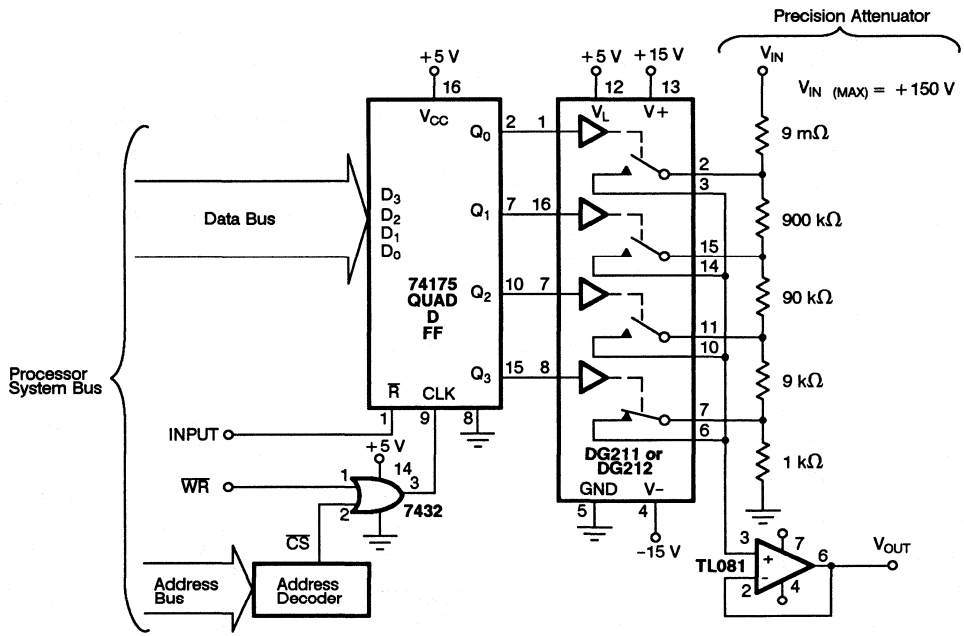


Figure 5. Microprocessor Controlled Analog Signal Attenuator

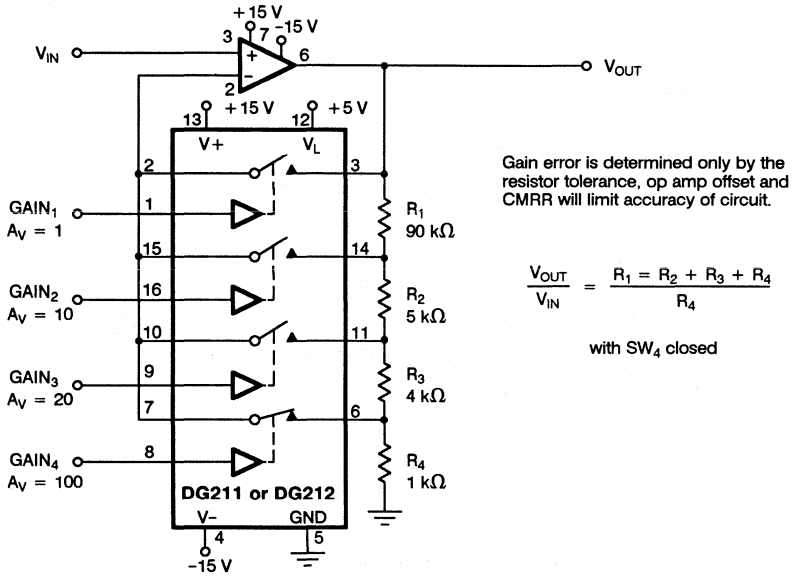


Figure 6. Precision-weighted Resistor Programmable-gain Amplifier

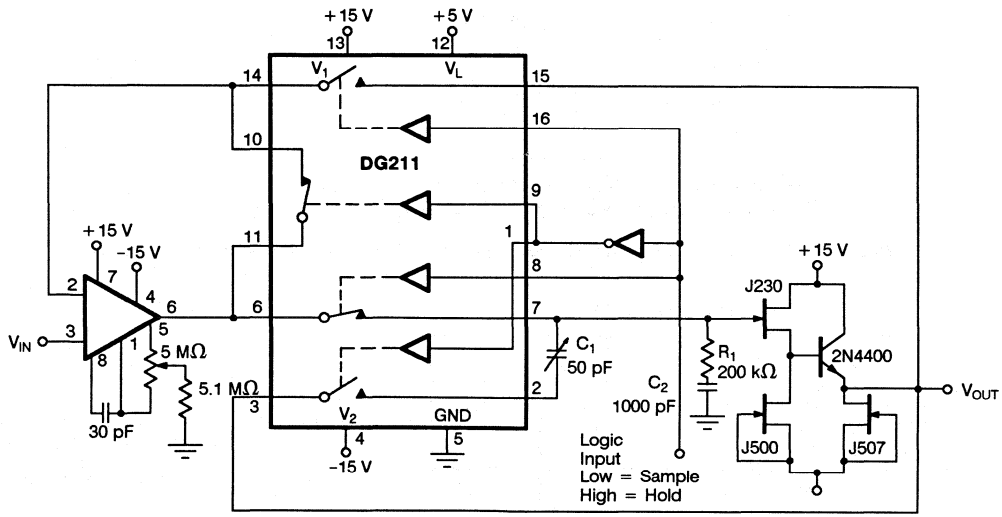
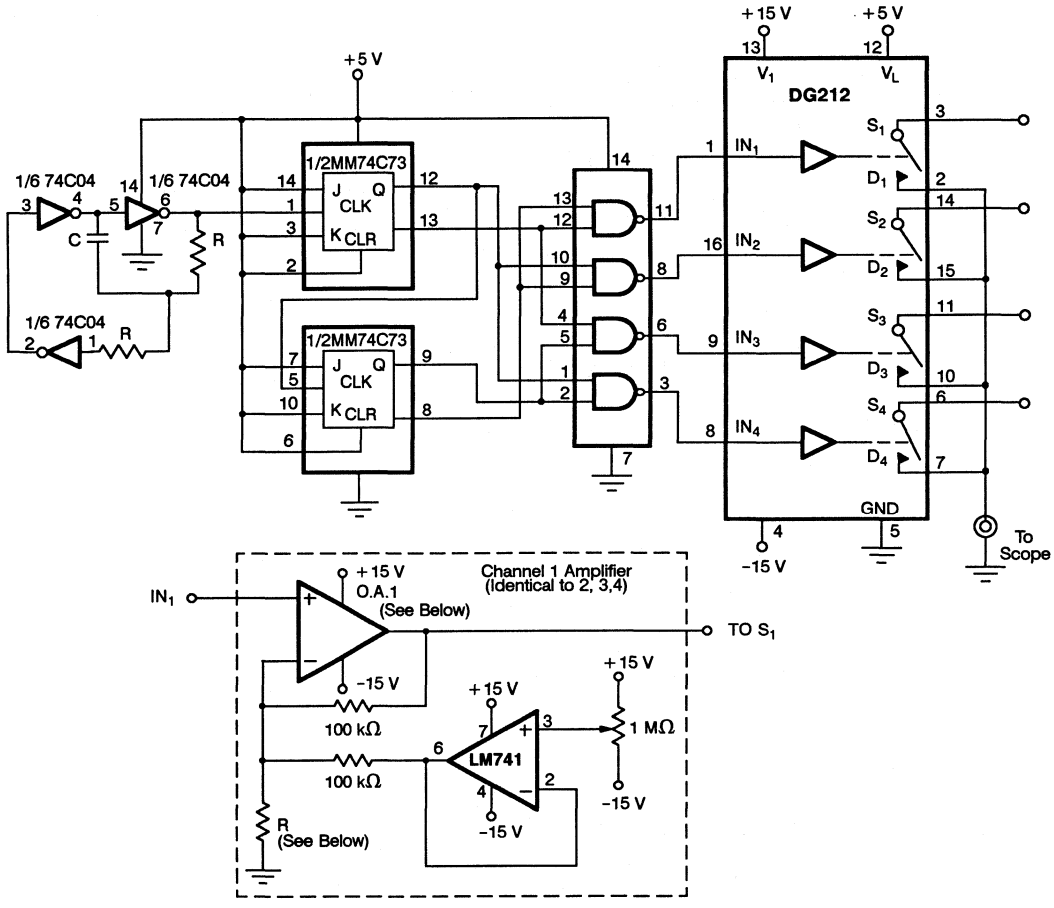


Figure 7. DG211 Sample-and-hold



O.A.1 is op amp with suitable bandwidth, slew rate, etc., for desired signals.
R is added for extra gain according to formula: Voltage Gain = $2 + \frac{100\,k}{R}$

Figure 8. The "Scope Extender" Which Displays 4-Channels Simultaneously on a Single Trace Scope

APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_L Logic Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min./ V_{INL} Max. (V)	V_S or V_D Analog Voltage Range (V)
20	-20	5	2.4/0.8	-20 to 20
15	-15	5	2.4/0.8	-15 to 15
12	-12	5	2.4/0.8	-12 to 12
10	-10	5	2.4/0.8	-10 to 10
8**	- 8	5	2.4/0.8	-8 to 8
10	-10	10	5/2	-10 to 10

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Operation below ±8 V is not recommended.

Siliconix incorporated

DG271

High-Speed Quad Monolithic SPST CMOS Analog Switch

FEATURES

- Fast Switching t_{ON}, t_{OFF} < 65 ns
- Charge Injection < 9 pC
- $r_{DS(ON)}$ < 50 Ω
- TTL Compatible

BENEFITS

- Faster System Operation
- Reduced Switching Glitches
- Low Impedance Operation

APPLICATIONS

- High Speed Switching
- Sample/Hold
- Digital Filters
- Op Amp Gain Switching
- Disk Drives

DESCRIPTION

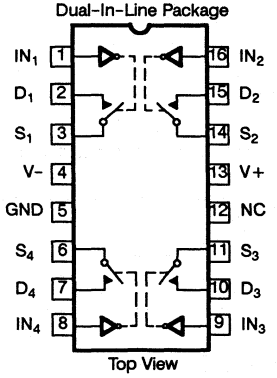
The DG271 high speed quad single-pole single-throw analog switch is intended for applications that require low ON resistance ($r_{DS(ON)}$ < 50 Ω), low leakage currents ($I_{S(ON)}$ < 1 nA), and fast switching speeds (t_{ON} < 65 ns).

Built on Siliconix' proprietary high voltage silicon gate process to achieve superior ON/OFF performance, each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. An epitaxial layer prevents latchup.

Packaging for this device includes the 16-pin CerDIP, plastic DIP, and small outline options. Performance grades include military, A suffix (–55 to 125°C), commercial, C suffix (0 to 30°C) and industrial D suffix (–40 to 85°C) temperature ranges.

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

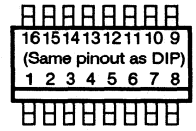
Dual-In-Line Package



Top View

Order Numbers:
CerDIP: DG271AK
DG271AK/883
Plastic: DG271CJ

Narrow Body
SO Package



Top View

Order Number:
DG271DY

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "0" ≥ 2.0 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
GND to V- ..... 25 V
Digital Inputs[e] V_S, V_D ..... (V–) –2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Storage Temperature (A & D Suffix) ..... –65 to 150°C
(C Suffix) ..... –65 to 125°C
Operating Temperature (A Suffix) ..... –55 to 125°C
(C Suffix) ..... 0 to 70°C
(D Suffix) ..... –40 to 85°C

Power Dissipation (Package)*
16-Pin CerDIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW
16-Pin Plastic SO**** ..... 600 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.5 mW/°C above 75°C.
****Derate 7.6 mW/°C above 75°C.

Siliconix incorporated

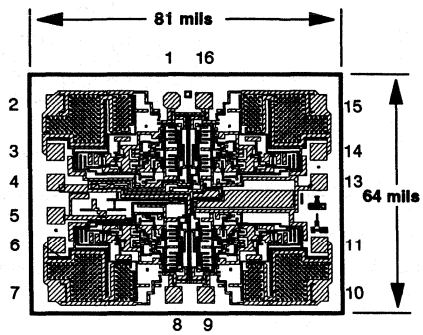
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = +15 V, V- = -15 V GND = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	C, D SUFFIX 0 to 70°C -40 to 85°C MIN[b]	C, D SUFFIX 0 to 70°C -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range	V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = 1 mA, V_D = ±10 V V_{IN} = 0.8 V		Room Full	32		50 75		50 75	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V_{IN} = 2 V	V_S = 14 V V_D = -14 V	Room Full	0.05	-1 -100	1 100	-1 -100	1 100	nA
			V_S = -14 V V_D = 14 V	Room Full	0.05	-1 -100	1 100	-1 -100	1 100	
	$I_{D(OFF)}$		V_D = 14 V V_S = -14 V	Room Full	0.05	-1 -100	1 100	-1 -100	1 100	
			V_D = -14 V V_S = 14 V	Room Full	0.05	-1 -100	1 100	-1 -100	1 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_{IN} = 0.8 V	V_D = V_S = 14 V	Room Full	0.05	-1 -200	1 200	-1 -200	1 200	
			V_D = V_S = -14 V	Room Full	0.05	-1 -200	1 200	-1 -200	1 200	
DIGITAL CONTROL										
Input Current with Voltage HIGH	I_{INH}	V_{IN} = 2 V		Room Full	0.010	-1 -10		-1 -10		µA
		V_{IN} = 15 V		Room Full	0.010		1 10		1 10	
Input Current with Voltage LOW	I_{INL}	V_{IN} = 0 V		Room Full	0.010	-1 -10		-1 -10		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Time Test Circuit V_S = ±10 V		Room Full	55		65 80		65 80	ns
Turn-OFF Time	t_{OFF}			Room Full	50		65 80		65 80	
Charge Injection	Q	C_L = 100 pF, V_{gen} = 0 V R_{gen} = 0 Ω		Room	9					pC
Source OFF Capacitance	$C_{S(OFF)}$	V_S = 0 V, V_{IN} = 5 V f = 1 MHz		Room	6					pF
Drain OFF Capacitance	$C_{D(OFF)}$			Room	8					
Channel ON Capacitance	C_D + C_S (ON)	V_D = V_S = 0 V, V_{IN} = 0 V		Room	24					
Off Isolation		R_L = 50 Ω f = 1 MHz		Room	75					dB
Crosstalk				Room	95					
SUPPLY										
Positive Supply Current	I+	All Channels ON or OFF		Room Full	4.3		7.5 11		7.5 11	mA
Negative Supply Current	I-			Room Full	-3.4	-6 -10		-6 -10		

SPECIFICATIONS[a]

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function. For logic "1" - V_{INH} = 2 V, for logic "0" - V_{INL} = 0.8 V.
f. Room = 25°C, Full as determined by operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function
1	Input 1
2	Drain 1
3	Source 1
4	V-
5	GND
6	Source 4
7	Drain 4
8	Input 4
9	Input 3
10	Drain 3
11	Source 3
13	V+ (Substrate)
14	Source 2
15	Drain 2
16	Input 2

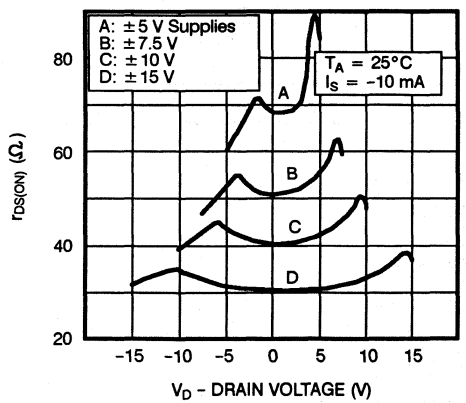
CSHB

4 Capacitors
6 Resistors
8 Diodes

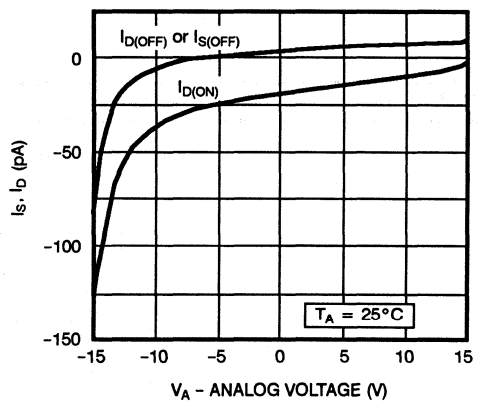
46 p-Channel Enhancement MOSFETs
54 n-Channel Enhancement MOSFETs

TYPICAL CHARACTERISTICS

$r_{DS(ON)}$ vs. V_D and Power Supply Voltage

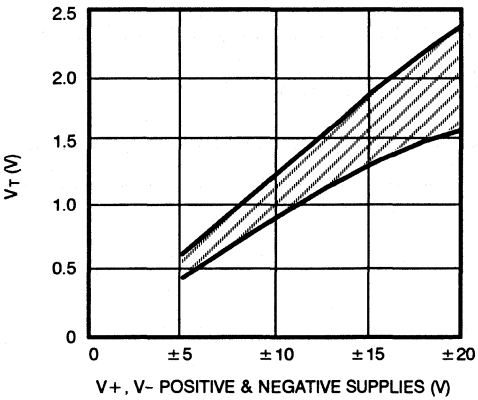


Leakage Currents vs. Analog Voltage

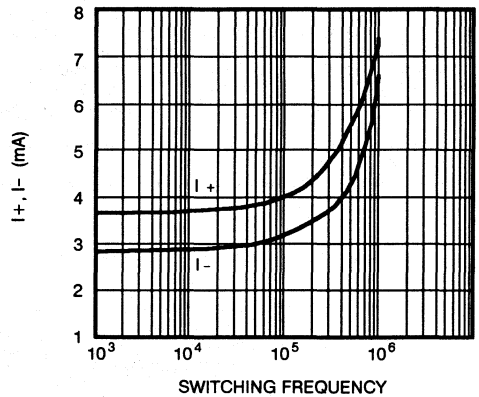


TYPICAL CHARACTERISTICS (Cont'd)

Input Switching Threshold vs. V+ and V- Supply Voltage

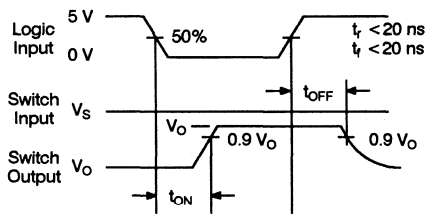


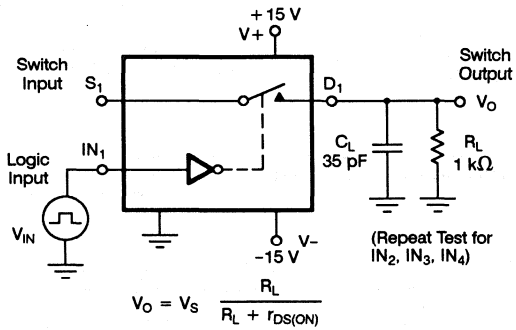
Supply Current vs. Switching Frequency



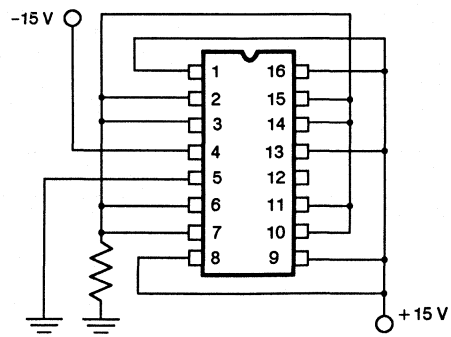
SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveforms as shown. Note that V_S maybe + or - as per switching time test circuit. V_O is the steady state output with switch ON. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.





BURN-IN CIRCUIT



Note: All resistors are 10 kΩ unless otherwise specified

DG300A/301A/302A/303A
CMOS Analog Switches

FEATURES

- Analog Signal Range ± 15 V
- Fast Switching (< 250 ns)
- Low $r_{DS(ON)}$ (< 50 Ω)
- Single Supply Operation
- Latchproof CMOS

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Operated Circuits

DESCRIPTION

The DG300A-DG303A family of monolithic CMOS switches feature three switch configuration options (SPST, SPDT, and DPST) for precision applications in communications, instrumentation and process control, where low leakage switching combined with low power consumption are required.

Designed on the Siliconix PLUS-40 CMOS process, these switches are latch proof, and are designed to block up to 30 Volts peak-to-peak when OFF. An epitaxial layer prevents latchup.

In the ON condition the switches conduct equally well in both directions (with no offset voltage) and minimize error conditions with their fairly flat ON-resistance.

Featuring low power consumption (a few mW) these switches are ideal for battery powered applications, without sacrificing switching speed. Designed for break-before-make switching action, these devices are quasi TTL and CMOS compatible. Single supply operation is allowed by connecting the V- rail to 0 volts.

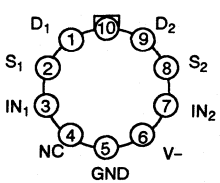
Package options for this series include 14-pin CerDIP and plastic DIP. Performance grades include the military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B suffix (-25 to 85°C) temperature ranges. Additionally, the DG300A and DG301A are available in 10-pin metal cans.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES

5

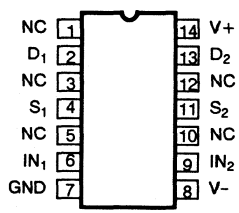
Metal Can Package

Top View
V+ (Substrate and Case)



Order Numbers:
DG300AAA/883
DG300ABA

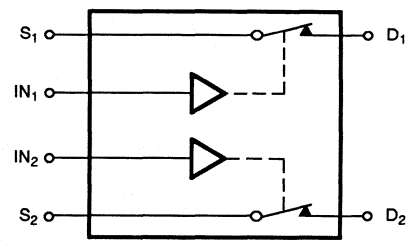
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG300AAK, DG300AAK/883, DG300ABK
Plastic: DG300ACJ

DG300A



Two SPST Switches per Package*

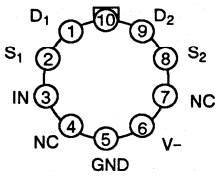
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 4.0 V
*Switches Shown for Logic "1" Input

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES (Cont'd)

Metal Can Package

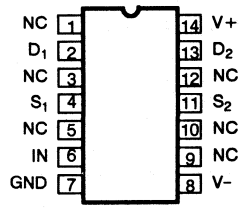
Top View
V+ (Substrate and Case)



Order Numbers:

DG301AAA, DG301AAA/883
DG301ABA

Dual-In-Line Package
Top View

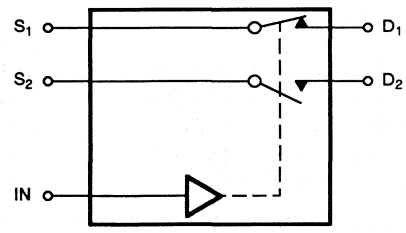


Order Numbers:

CerDIP: DG301AAK, DG301AAK/883, DG301ABK

Plastic: DG301ACJ

DG301A

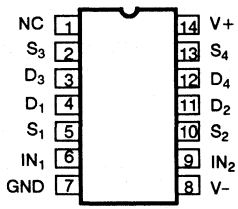


One SPDT Switch per Package*

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 4.0 V

Dual-In-Line Package
Top View

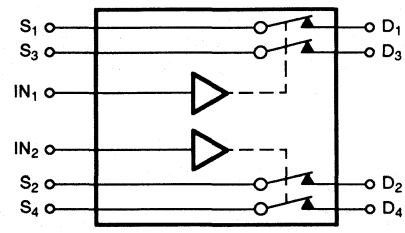


Order Numbers:

CerDIP: DG302AAK, DG302AAK/883

Plastic: DG302ACJ

DG302A

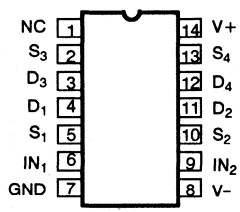


Two DPST Switches per Package*

Logic	Switch
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 4.0 V

Dual-In-Line Package
Top View

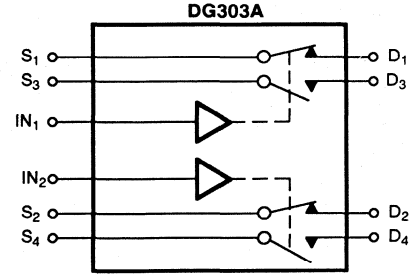


Order Numbers:

CerDIP: DG303AAK, DG303AAK/883, DG303ABK

Plastic: DG303ACJ

DG303A



Two SPDT Switches per Package*

Logic	SW_1 SW_2	SW_3 SW_4
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 4.0 V
*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[e], V_S, V_D ..... (V–) –2 V to (V+) +2V or ..... 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... –65 to 150°C

(C Suffix) ..... –65 to 125°C

Operating Temperature (A Suffix) ..... –55 to 125°C

(B Suffix) ..... –25 to 85°C

(C Suffix) ..... 0 to 70°C

Power Dissipation*

14-Pin Cerdip (K)** ..... 825 mW

14-Pin Plastic DIP (J)*** ..... 470 mW

10-Pin Metal Can (A)**** ..... 450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

****Derate 6 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V– = –15 V, GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		–15	15	–15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or V_{IN} = 4 V[f]	V_D = 10 V, I_S = –10 mA	Room	30		50		50	Ω
				Full			75		75	
			V_D = –10 V, I_S = 10 mA	Room	30		50		50	
				Full			75		75	
Source OFF leakage Current	$I_{S(OFF)}$		V_S = 14 V, V_D = –14 V	Room	0.1		1		5	nA
				Hot			100		100	
			V_S = –14 V, V_D = 14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = –14 V, V_D = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_S = 14 V, V_D = –14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain On Leakage Current	$I_{D(ON)}$		V_D = V_S = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_D = V_S = –14 V	Room	–0.1	–2	2	–5	5	
				Hot		–200	200	–200	200	
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room	–0.001	–1		–1		µA
				Full		–1				
		V_{IN} = 15 V		Room	0.001		1		1	
				Full			1			
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Room	–0.001	–1		–1		
				Full		–1				
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Test Time Circuit		Room	150		300			ns
Turn-OFF Time	t_{OFF}			Room	130		250			
Break-Before-Make Time	t_{BBM}	See Break-Before-Make Test Circuit DG301A/303A ONLY		Room	50					
Charge Injection	Q	C_L = 1 nF, R_{gen} = 0 Ω, V_{gen} = 0 V		Room	8					pC

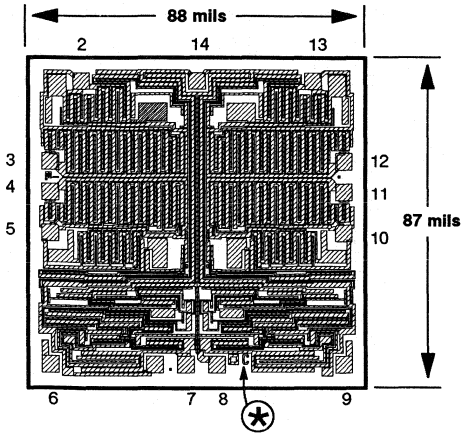
5

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)										
Source-OFF Capacitance	$C_{S(OFF)}$	V_{IN} = 0.8 V or	V_S = 0 V	Room	14					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_{IN} = 4 V	V_D = 0 V	Room	14					pF
Channel-ON Capacitance	$C_{D + S(ON)}$	f = 1 MHz	V_S = V_D = 0 V	Room	40					pF
Input Capacitance	C_{in}	f = 1 MHz	V_{IN} = 0 V	Room	6					pF
			V_{IN} = 15 V	Room	7					pF
OFF-Isolation[f]		V_{IN} = 0 V, R_L = 1 kΩ		Room	62					dB
Crosstalk (Channel-to-Channel)		V_S = 1 V_{rms}, f = 500 kHz		Room	74					dB
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 4 V (One Input)		Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I-	(All Others = 0)		Room Full	-0.001	-10 -100		-100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)		Room Full	0.001		10 100		100	µA
Negative Supply Current	I-			Room Full	-0.001	-10 -100		-100		µA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Signals S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
f. OFF-isolation: 20 log $\frac{V_S}{V_D}$ V_S = input to OFF switch, V_D = output.
g. V_{IN} = input voltage to perform proper function.
h. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

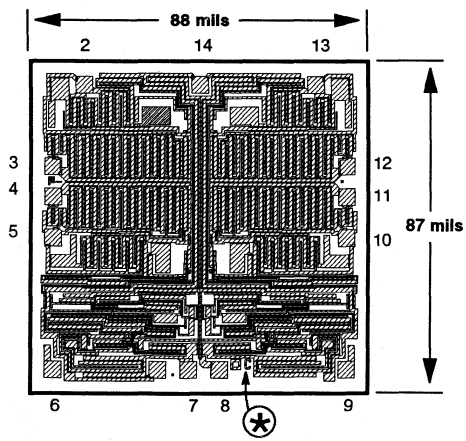
DIE TOPOGRAPHIES



Pad No.	Function DG300A	Pad No.	Function DG302A
2	D_1	2	S_3
3	S_1	3	D_3
4	NC	4	D_1
5	NC	5	S_1
6	IN_1	6	IN_1
7	GND	7	GND
8	V–	8	V–
9	IN_2	9	IN_2
10	NC	10	S_2
11	NC	11	D_2
12	S_2	12	D_4
13	D_2	13	S_4
14	V+ (Substrate)	14	V+ (Substrate)

ICMJA ***A = DG300A**
4 Capacitors — 18 p-channel Depletion MOSFETs
2 Resistors — 22 n-channel Depletion MOSFETs
4 Diodes

ICMJA ***A = DG302A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes



Pad No.	Function DG301A	Pad No.	Function DG303A
2	D_1	2	S_3
3	S_1	3	D_3
4	NC	4	D_1
5	NC	5	S_1
6	IN	6	IN_1
7	GND	7	GND
8	V–	8	V–
9	NC	9	IN_2
10	NC	10	S_2
11	NC	11	D_2
12	S_2	12	D_4
13	D_2	13	S_4
14	V+ (Substrate)	14	V+ (Substrate)

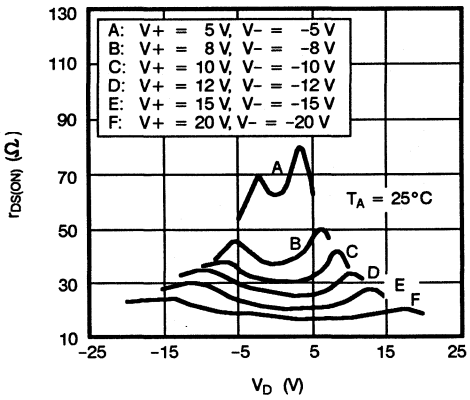
ICMJB ***B = DG301A**
4 Capacitors — 11 p-channel Depletion MOSFETs
1 Resistor — 15 n-channel Depletion MOSFETs
2 Diodes

ICMJC ***C = DG303A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes

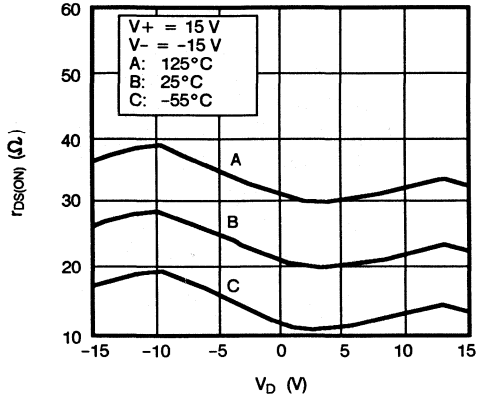
5

TYPICAL CHARACTERISTICS

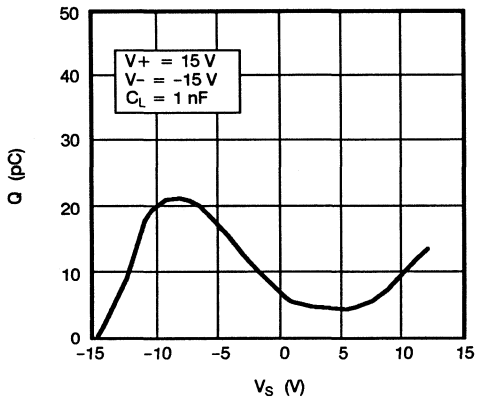
$r_{DS(ON)}$ vs. V_D and Power Supply



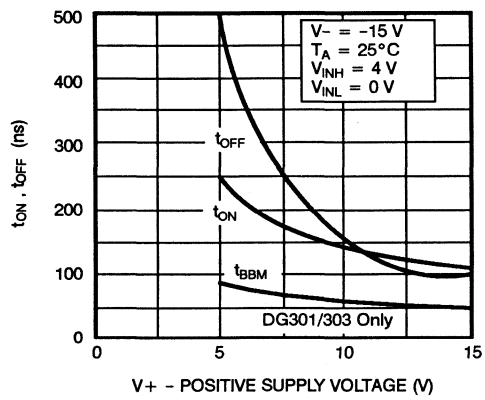
$r_{DS(ON)}$ vs. V_D and Temperature



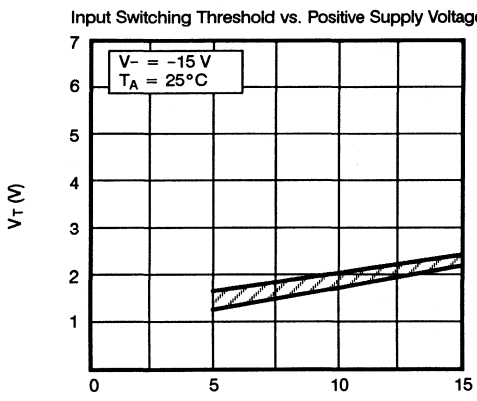
Charge Injection vs. Analog Voltage (V_S)



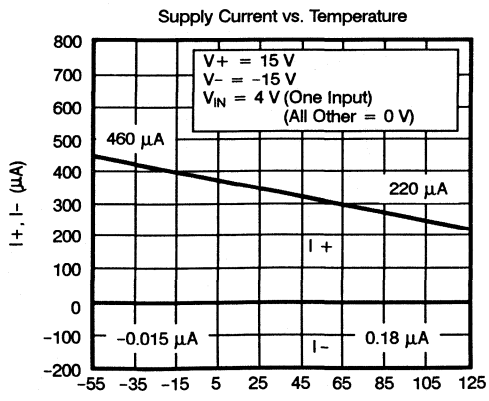
Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Input Switching Threshold vs. Positive Supply Voltage

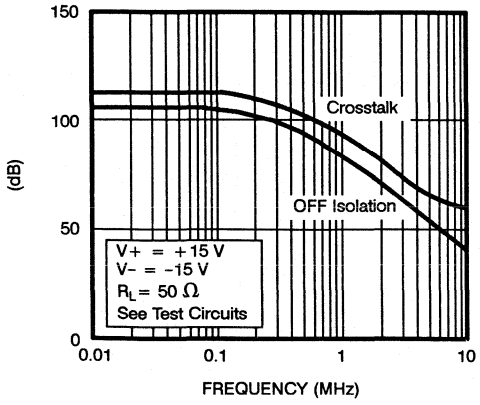


Supply Current vs. Temperature

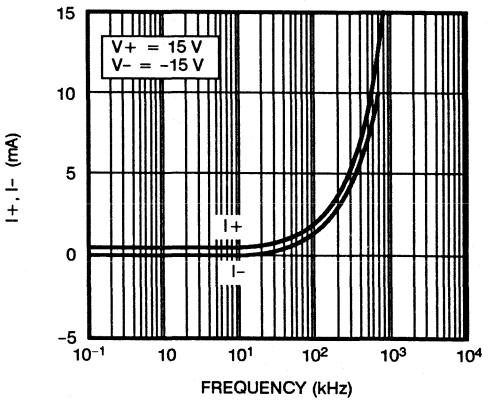


TYPICAL CHARACTERISTICS (Cont'd)

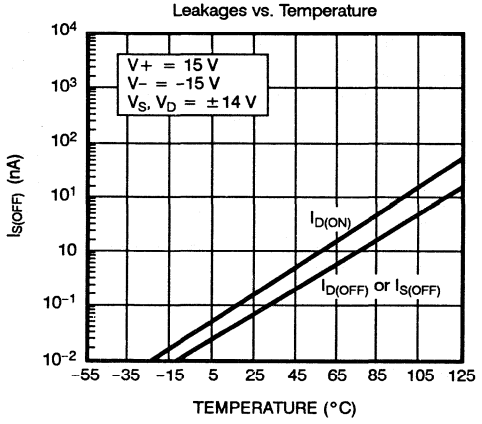
Off Isolation and Crosstalk vs. Frequency



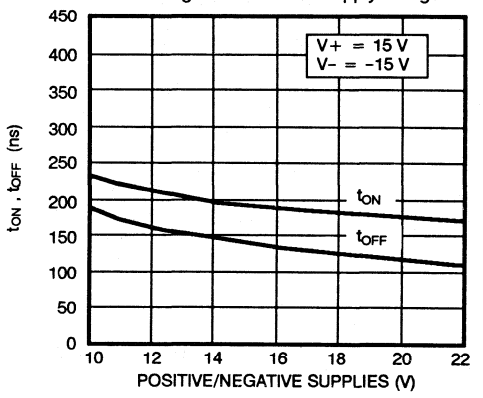
Supply Currents vs. Switching Frequency



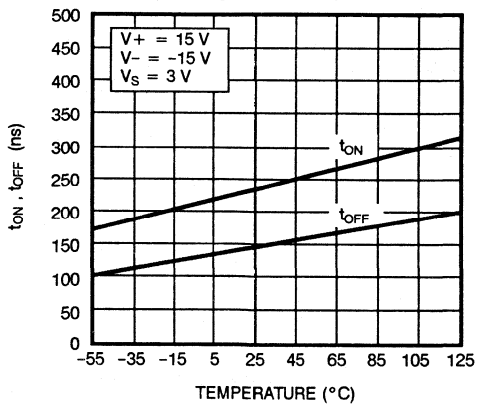
Leakages vs. Temperature



Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



5

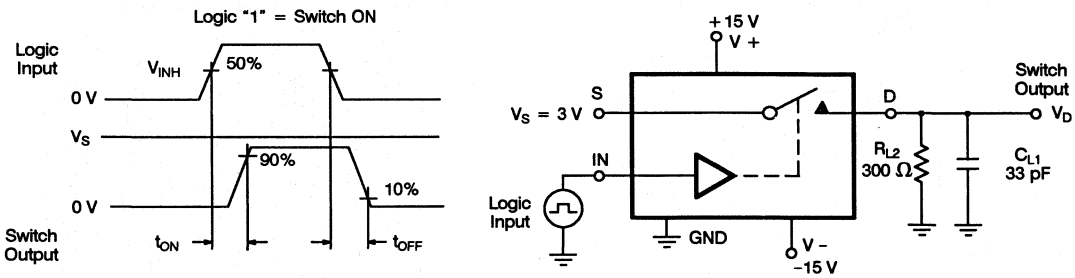


Figure 1. Switching Time

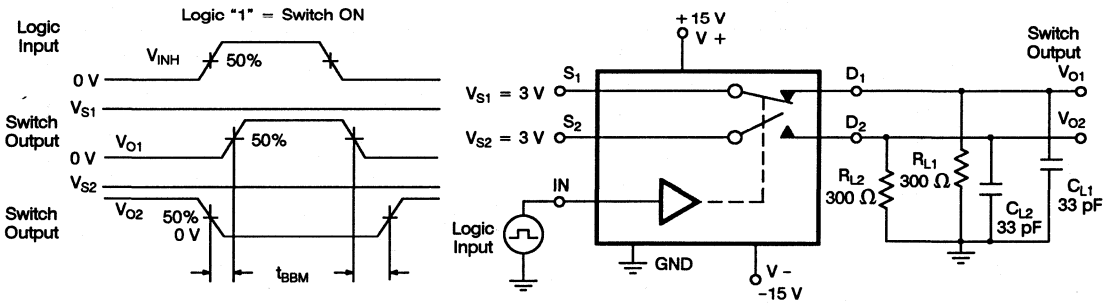


Figure 2. Break-Before-Make SPDT (DG301A, DG303A)

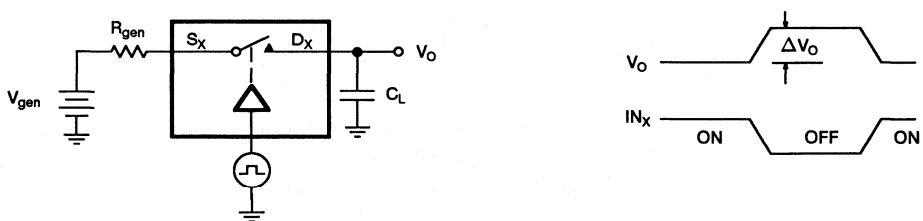


Figure 3. Charge Injection Test Circuit

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

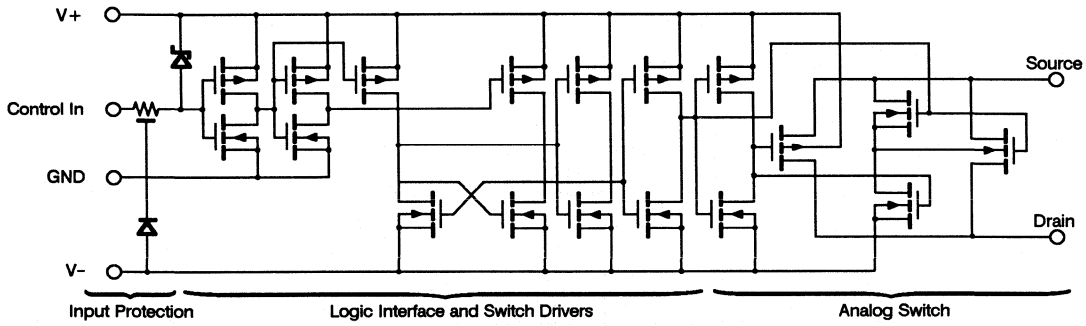


Figure 4.

APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Voltage (V)	V_{IN} Logic Input Voltage V_{INH}Min/V_{INL}Max (V)	V_S Analog Voltage Range (V)
15	-15	0	4/0.8	-15 to 15
20	-20	0	4/0.8	-20 to 20
15	0	0	4/0.8	0 to 15

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APPLICATIONS

The DG300A series of analog switches will switch positive analog signals while using a single positive supply. This facilitates their use in applications where only one supply is available. The trade-offs of using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. Typical curves for design aid are given in the following figures. The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 V.

Input Switching Threshold vs. Positive Supply Voltage

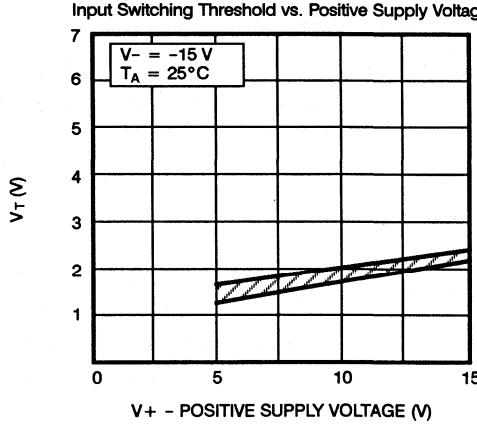


Figure 5.

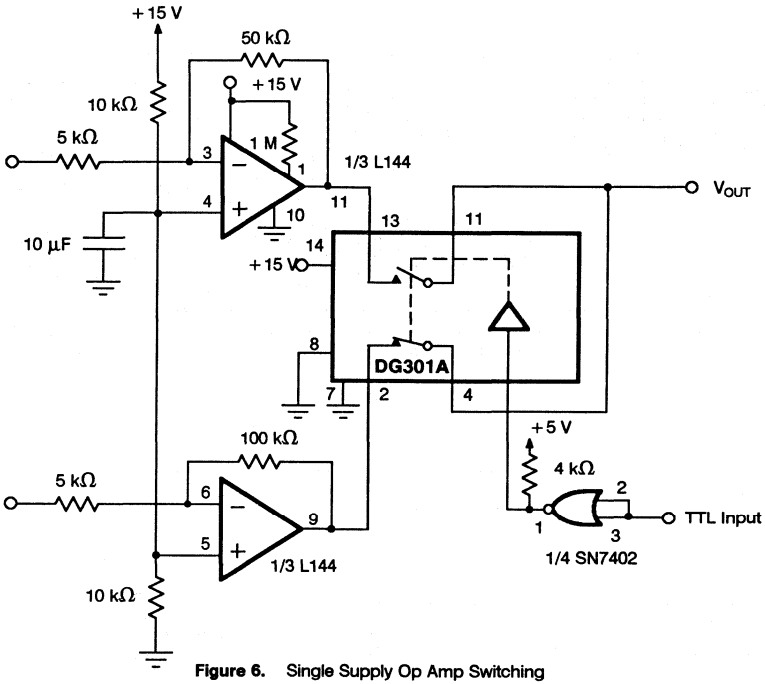
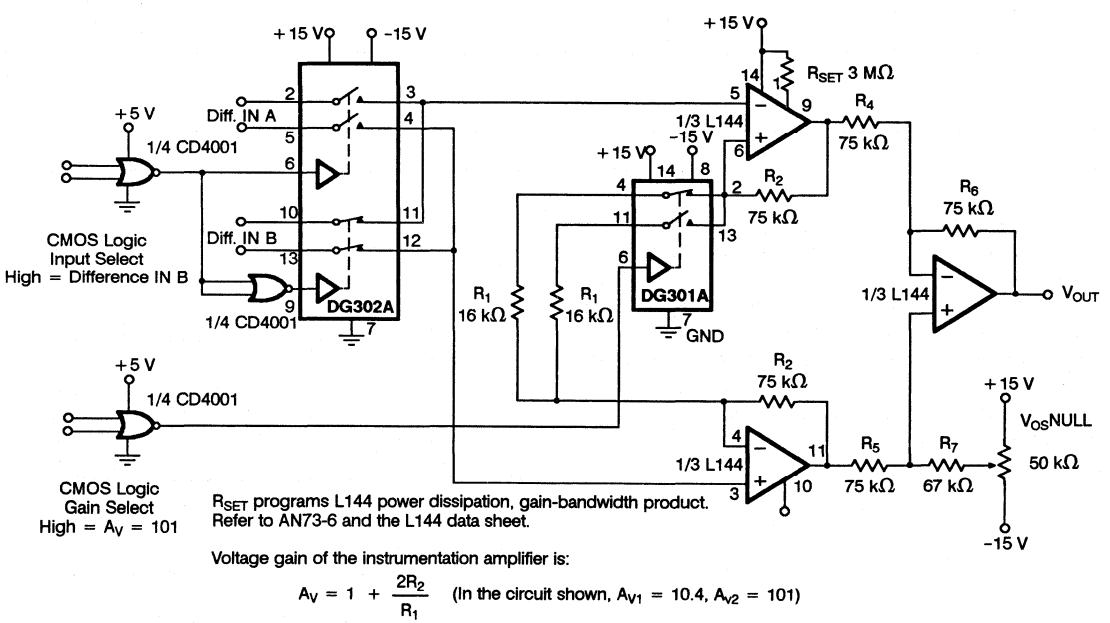


Figure 6. Single Supply Op Amp Switching



R_{SET} programs L144 power dissipation, gain-bandwidth product. Refer to AN73-6 and the L144 data sheet.

Voltage gain of the instrumentation amplifier is:

$$A_V = 1 + \frac{2R_2}{R_1} \quad \text{(In the circuit shown, } A_{V1} = 10.4, A_{V2} = 101\text{)}$$

Figure 7. Low Power Instrumentation Amplifier with Digitally Selectable Inputs and Gain

DG304A/305A/306A/307A
CMOS Analog Switches

FEATURES

- ±15 V Input Range
- Fast Switching (<250 ns)
- Low $r_{DS(ON)}$ (<50 Ω)
- Single Supply Operation
- CMOS Logic Levels

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable and Battery Operation

DESCRIPTION

The DG304A through DG307A series of monolithic CMOS switches were designed for applications in communications, instrumentation and process control. This series is well suited for applications requiring fast switching and nearly flat ON-resistance over the entire analog range.

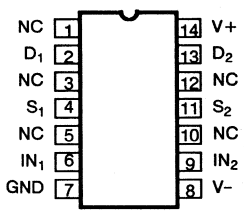
Designed on Siliconix PLUS-40 CMOS process to achieve low power consumption (a few milliwatts) and excellent ON/OFF switch performance, making these ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation (for positive switch voltages) is afforded by connecting the V- rail to 0 V.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. These switches are CMOS input compatible.

There are four devices in this series, which are differentiated by the type of switch action. Packaging for this series include the 14-pin CerDIP and plastic options. The 10-pin metal can option is also available for the DG305A. Performance grades include the military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B suffix (-25 to 85°C) temperature ranges.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES

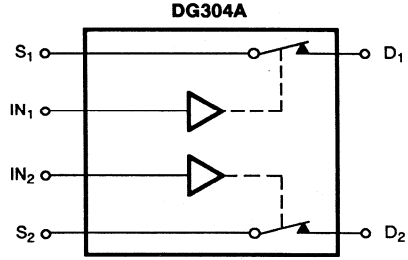
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG304AAK/883
Plastic: DG304ACJ

DG304A



Two SPST Switches per Package*

Logic	Switch
0	OFF
1	ON

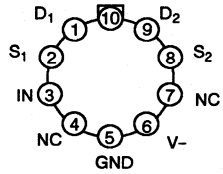
Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V
*Switches Shown for Logic "1" Input

5

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES (Cont'd)

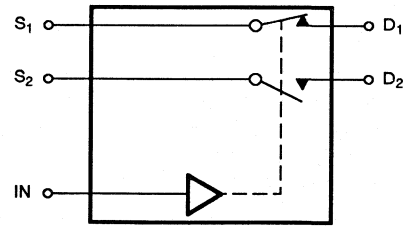
Metal Can Package

Top View
V+ (Substrate and Case)



Order Numbers:
DG305AAA

DG305A

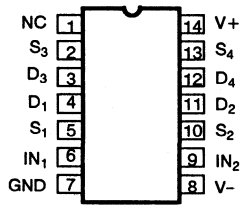


One SPDT Switch per Package*

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

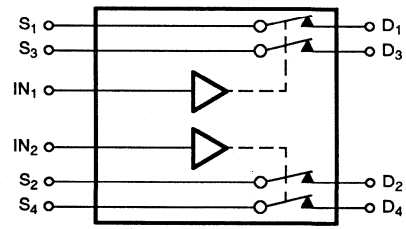
Logic "0" $\leq$ 3.5 V
Logic "1" $\geq$ 11 V

Dual-In-Line Package
Top View



Order Numbers:
Plastic: DG306ACJ

DG306A

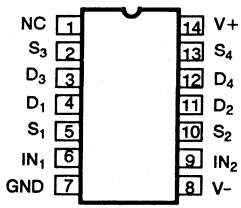


Two DPST Switches per Package*

Logic	Switch
0	OFF
1	ON

Logic "0" $\leq$ 3.5 V
Logic "1" $\geq$ 11 V

Dual-In-Line Package
Top View

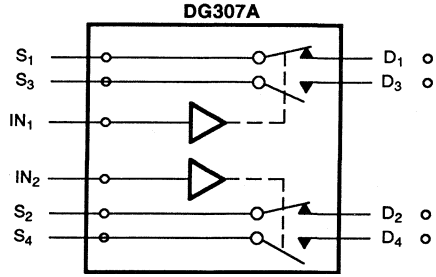


Order Numbers:

CerDIP: DG307AAK, DG307AAK/883, DG307ABK

Plastic: DG307ACJ

DG307A



Two SPDT Switches per Package*

Logic	SW_1 SW_2	SW_3 SW_4
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 3.5 V
Logic "1" $\geq$ 11 V

*Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[e], V_S, V_D ..... (V–) –2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... –65 to 150°C

(C Suffix) ..... –65 to 125°C

Operating Temperature (A Suffix) ..... –55 to 125°C

(B Suffix) ..... –25 to 85°C

(C Suffix) ..... 0 to 70°C

Power Dissipation*

14-Pin Cerdip (K)** ..... 825 mW

14-Pin Plastic DIP (J)*** ..... 470 mW

10-Pin Metal Can (A)**** ..... 450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

****Derate 6 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V– = –15 V, GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}	I_S = 10 mA, V_{IN} 3.5 or 11 V[g]		Full		–15	15	–15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$		V_D = 10 V, I_S = –10 mA	Room	30		50		50	Ω
				Full			75		75	
			V_D = –10 V, I_S = 10 mA	Room	30		50		50	
				Full			75		75	
Source OFF leakage Current	$I_{S(OFF)}$		V_S = 14 V, V_D = –14 V	Room	0.1		1		5	nA
				Hot			100		100	
		V_{IN} = 3.5 V or	V_S = –14 V, V_D = 14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 11 V[g]	V_S = –14 V, V_D = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_S = 14 V, V_D = –14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain On Leakage Current	$I_{D(ON)}$		V_D = V_S = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_D = V_S = –14 V	Room	–0.1	–2	2	–5	5	
				Hot		–200	200	–200	200	
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room	–0.001	–1		–1		µA
				Full		–1				
		V_{IN} = 15 V		Room	0.001		1		1	
				Full			1			
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Room	–0.001	–1		–1		
				Full		–1				
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching		Room	110		250			ns
Turn-OFF Time	t_{OFF}	Test Time Circuit		Room	70		150			
Break-Before-Make Time	t_{BBM}	See Break-Before-Make Test Circuit DG305A/307A ONLY		Room	50					
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 1 Ω, V_{gen} = 0 V		Room	30					pC

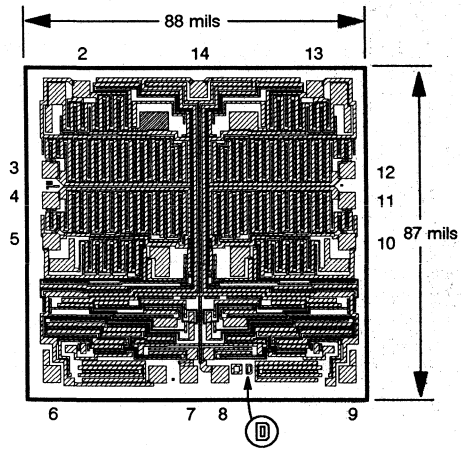
5

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)										
Source-OFF Capacitance	$C_{S(OFF)}$	V_{IN} = 3.5 V or	V_S = 0 V	Room	14					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_{IN} = 11 V[g]	V_D = 0 V	Room	14					
Channel-ON Capacitance	$C_{D + S(ON)}$	f = 1 MHz	V_S = V_D = 0 V	Room	40					
Input Capacitance	C_{in}	f = 1 MHz	V_{IN} = 0 V	Room	6					
			V_{IN} = 15 V	Room	7					
OFF-Isolation[f]		V_{IN} = 0 V, R_L = 1 kΩ		Room	62					dB
Crosstalk (Channel-to-Channel)		V_S = 1 V_{rms}, f = 500 kHz		Room	74					
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 4 V (One Input)		Room Full	0.001		10 100		100	µA
Negative Supply Current	I-	(All Others = 0)		Room Full	-0.001	-10 -100		-100		
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)		Room Full	0.001		10 100		100	
Negative Supply Current	I-			Room Full	-0.001	-10 -100		-100		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Signals S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
f. OFF-isolation: 20 log $\frac{V_S}{V_D}$ V_S = input to OFF switch, V_D = output.
g. V_{IN} = input voltage to perform proper function.
h. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

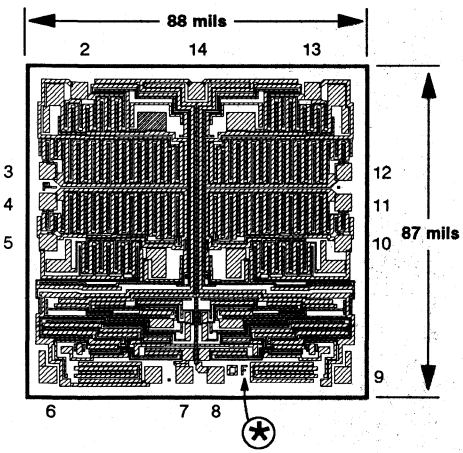
DIE TOPOGRAPHIES



Pad No.	Function DG304A	Pad No.	Function DG306A
2	D_1	2	S_3
3	S_1	3	D_3
4	NC	4	D_1
5	NC	5	S_1
6	IN_1	6	IN_1
7	GND	7	GND
8	V–	8	V–
9	IN_2	9	IN_2
10	NC	10	S_2
11	NC	11	D_2
12	S_2	12	D_4
13	D_2	13	S_4
14	V+ (Substrate)	14	V+ (Substrate)

ICMJD **D = DG304A**
4 Capacitors — 16 p-channel Depletion MOSFETs
2 Resistors — 20 n-channel Depletion MOSFETs
4 Diodes

ICMJD **D = DG306A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes



Pad No.	Function DG305A	Pad No.	Function DG307A
2	D_1	2	S_3
3	S_1	3	D_3
4	NC	4	D_1
5	NC	5	S_1
6	IN	6	IN_1
7	GND	7	GND
8	V–	8	V–
9	NC	9	IN_2
10	NC	10	S_2
11	NC	11	D_2
12	S_2	12	D_4
13	D_2	13	S_4
14	V+ (Substrate)	14	V+ (Substrate)

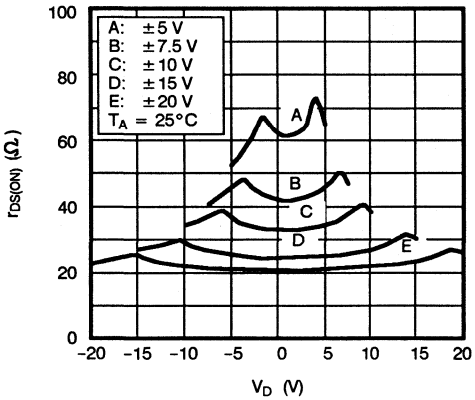
ICMJE ***E = DG305A**
4 Capacitors — 10 p-channel Depletion MOSFETs
1 Resistor — 14 n-channel Depletion MOSFETs
2 Diodes

ICMJF ***F = DG307A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes

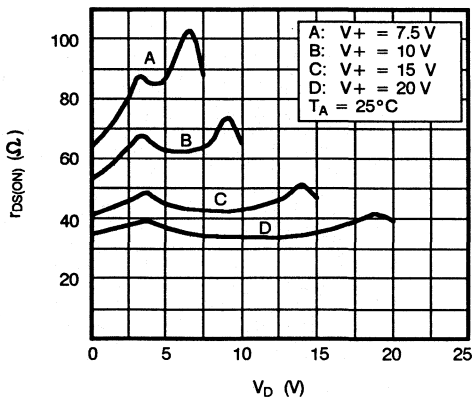
5

TYPICAL CHARACTERISTICS

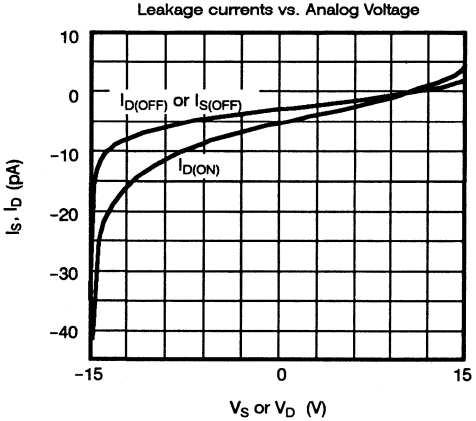
$r_{DS(ON)}$ vs. V_D and Power Supply



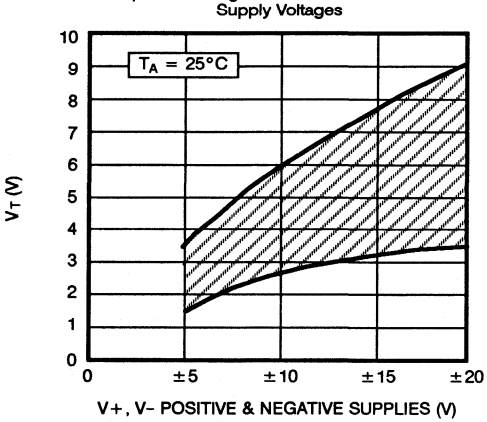
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage
V- = 0 V



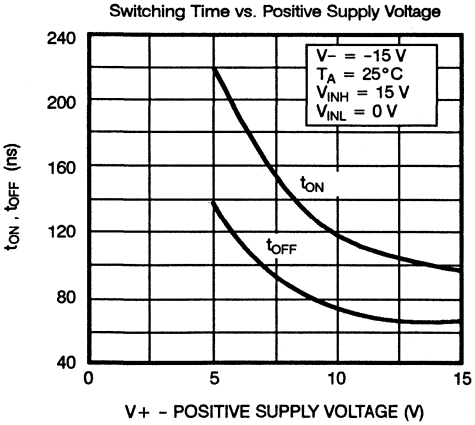
Leakage currents vs. Analog Voltage



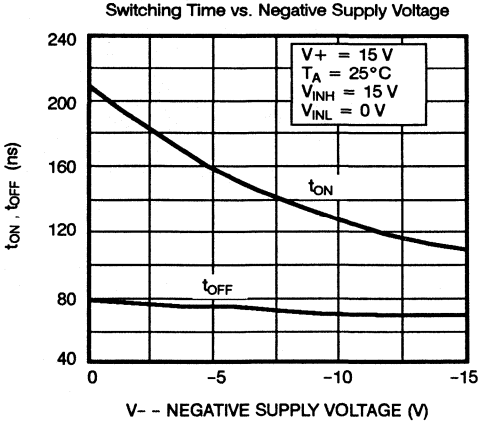
Input Switching Threshold vs. V+ and V- Supply Voltages



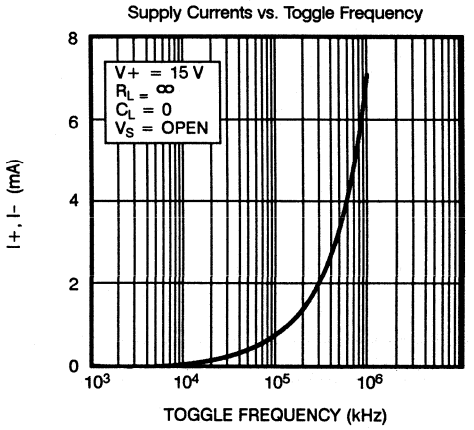
Switching Time vs. Positive Supply Voltage



Switching Time vs. Negative Supply Voltage



TYPICAL CHARACTERISTICS (Cont'd)



TEST CIRCUITS

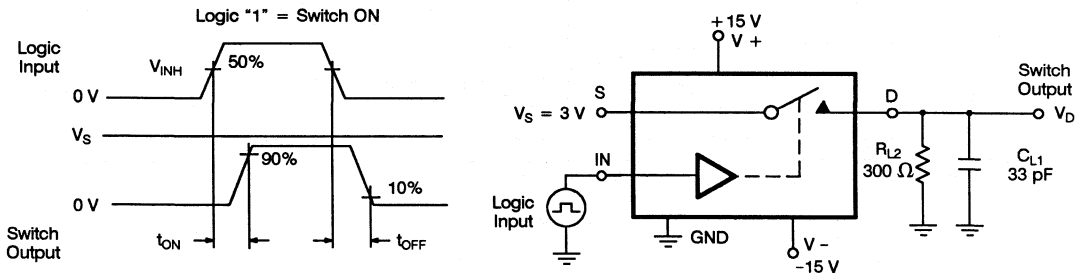


Figure 1. Switching Time

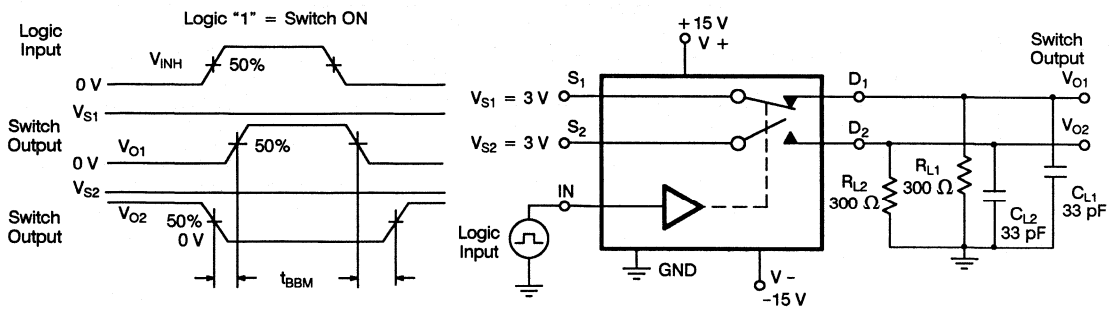
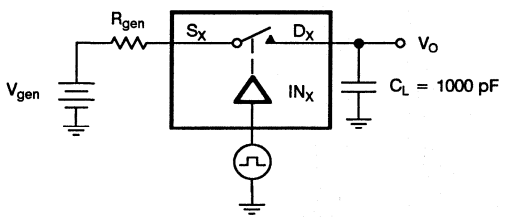
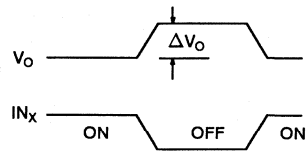


Figure 2. Break-Before-Make SPDT (DG305A, DG307A)

5

TEST CIRCUITS (Cont'd)





ΔV_O is the measured voltage error due to charge injection.
The Charge injection in coulombs is $\Delta Q = C_L \times \Delta V_O$.

Figure 3. Charge Injection Test Circuit

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

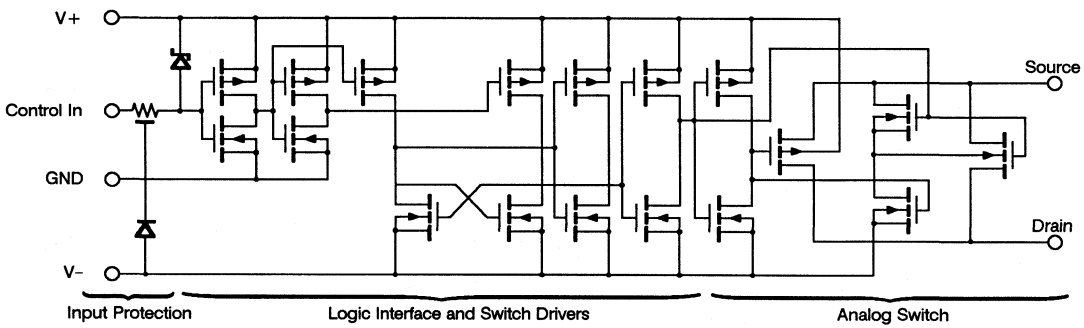


Figure 4.

APPLICATION HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH}Min/V_{INL}Max (V)	V_S Analog Voltage Range (V)
15 20 15	-15 -20 0	11/3.5 11/3.5 11/3.5	-15 to 15 -20 to 20 0 to 15

APPLICATIONS

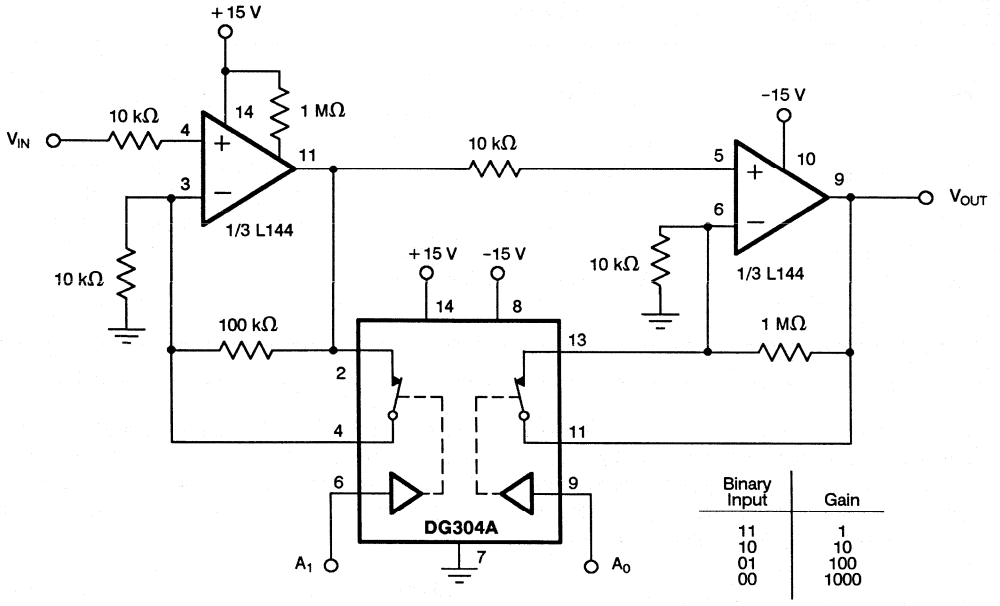


Figure 5. Low Power Binary to 10^n Gain Low Frequency Amplifier

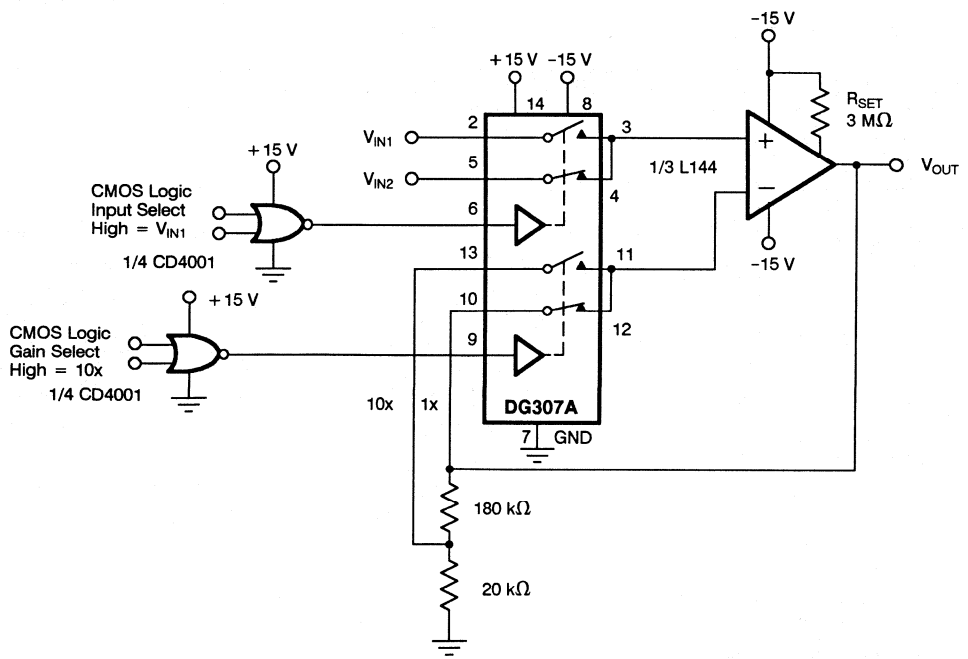


Figure 6. Low Power Non-inverting Amplifier with Digitally Selectable Inputs and Gain

DG308A/309
Quad Monolithic SPST CMOS Analog Switches

Siliconix incorporated

FEATURES

- ±15 V Input Range
- Low ON-Resistance (<60 Ω Typ.)
- Fast Switching (<130 ns)
- Low Power Dissipation (<30 μW Typ.)
- CMOS Logic Compatible

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Low Signal Error
- Wide Dynamic Range
- Single or Dual Supply Capability
- Static Protected Logic Inputs

APPLICATIONS

- Portable, Battery Instrumentation
- Communication Systems
- Computer Peripherals
- High Speed Multiplexing

DESCRIPTION

The DG308A and DG309 are quad single-pole single-throw analog switches designed for high speed switching applications in communications, instrumentation, and process control. This series is well suited for applications requiring nearly a constant ON-resistance over the entire analog range.

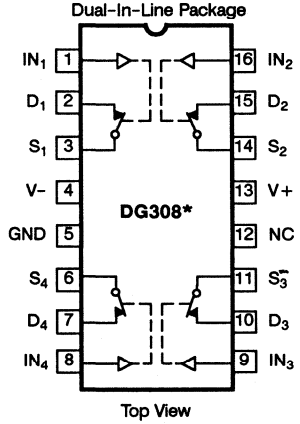
Featuring low ON-resistance (< 60 Ω) and fast switching (<130 ns), the DG308A is supplied in the "normally open" configuration while DG309 is supplied "normally closed". Input thresholds are CMOS compatible.

Designed with the Siliconix PLUS-40 CMOS process to combine low power dissipation with a high breakdown voltage rating of 44 V, each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. An epitaxial layer prevents latch up.

Packaging includes a 16-pin CerDIP and plastic DIP. Performance grades include military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B and D suffixes (-25, -40 to 85°C) temperature ranges. Additionally, both are offered in a 16-pin small outline package.

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package



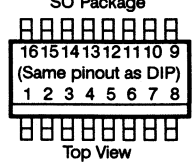
Top View

Order Numbers:

CerDIP: DG308AAK, DG308AAK/883
DG308ABK, DG308ACK
DG309AK/883

Plastic: DG308ACJ or DG309CJ

Narrow Body SO Package



Top View

Order Numbers:
DG308ADY, DG309DY

Four SPST Switches per Package

Truth Table

Logic	Switch DG308A	Switch DG309
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5 V
Logic "1" ≥ 11 V

* Switches shown for logic "1" input.

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[e], V_S, V_D ..... (V–) –2 V to (V+) +2V or ..... 20 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 20 mA

(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA

Storage Temperature (A & B Suffix) ..... –65 to 150°C

(C & D Suffix) ..... –65 to 125°C

Operating Temperature (A Suffix) ..... –55 to 125°C

(B Suffix) ..... –25 to 85°C

(C Suffix) ..... 0 to 70°C

(D Suffix) ..... –40 to 85°C

Power Dissipation*

16-Pin Cerdip** ..... 900 mW

16-Pin Plastic DIP*** ..... 470 mW

16-Pin Plastic SO**** ..... 950 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

****Derate 7.7 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V– = –15 V GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		–15	15	–15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 11 V (DG308A)	V_D = 10 V, I_S = 1 mA	Room	60		100		100	Ω
				Full			150		125	
		V_{IN} = 3.5 V (DG309)	V_D = –10 V, I_S = 1 mA	Room	60		100		100	
				Full			150		125	
Source OFF leakage Current	$I_{S(OFF)}$		V_S = 14 V, V_D = –14 V	Room	0.1		1		5	nA
				Full			100		100	
		V_{IN} = 11 V (DG308A)	V_S = –14 V, V_D = 14 V	Room	–0.1	–1	1	–5	5	
				Full		–100	100	–100	100	
Drain OFF Leakage Current	$I_{D(OFF)}$	V_{IN} = 3.5 V (DG309)	V_D = 14 V, V_S = –14 V	Room	0.1	–1	1	–5	5	
				Full		–100	100	–100	100	
			V_D = –14 V, V_S = 14 V	Room	–0.1	–1	1	–5	5	
				Full		–100	100	–100	100	
Drain On Leakage Current	$I_{D(ON)}$	V_{IN} = 11 V (DG308A)	V_D = V_S = 14 V	Room	0.1	–1	1	–5	5	
				Full		–100	100	–200	200	
		V_{IN} = 3.5 V (DG309)	V_D = V_S = –14 V	Room	–0.1	–2	2	–5	5	
				Full		–100	100	–200	200	
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 15 V		Full	0.001		1		1	µA
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Full	–0.001	–1		–1		
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching		Room	130		200		200	ns
Turn-OFF Time	t_{OFF}	Test Time Circuit		Room	90		150		150	
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 0Ω, V_{gen} = 0 V		Room	–10					pC

5

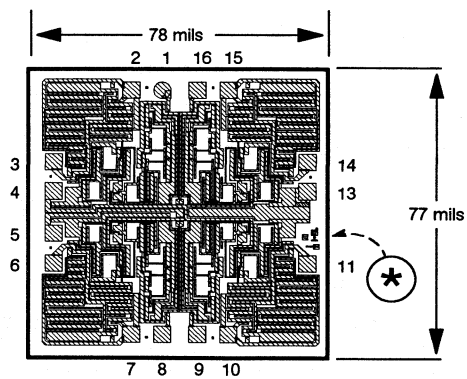
Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)										
Source-OFF Capacitance	$C_{S(OFF)}$	f = 140 kHz	V_S = 0 V, V_{IN} = 0 V (DG308A), V_{IN} = 15 V (DG309)	Room	11					pF
Drain-OFF Capacitance	$C_{D(OFF)}$		V_D = 0 V, V_{IN} = 0 V (DG308A), V_{IN} = 15 V (DG309)	Room	8					
Channel-ON Capacitance	$C_{D + S(ON)}$		V_S = V_D = 0 V, V_{IN} = 15 V (DG308A), V_{IN} = 0 V (DG309)	Room	27					
OFF-Isolation[f]		Z_L = 75 Ω, V_S = 2 V_{p-p}, f = 500 kHz, V_{IN} = 0 V (DG308A), V_{IN} = 15 V (DG309)		Room	78					dB
POWER SUPPLIES										
Positive Supply Current	I+	All Channels ON or OFF		Room Full	0.001		10 100		10 100	µA
Negative Supply Current	I-	V_{IN} = 0 V or 15 V		Room Full	-0.001	-10 -100		-100		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Signals S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
f. OFF-isolation: $20 \log \frac{V_S}{V_D}$ V_S = input to OFF switch, V_D = output.
g. V_{IN} = input voltage to perform proper function.
h. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



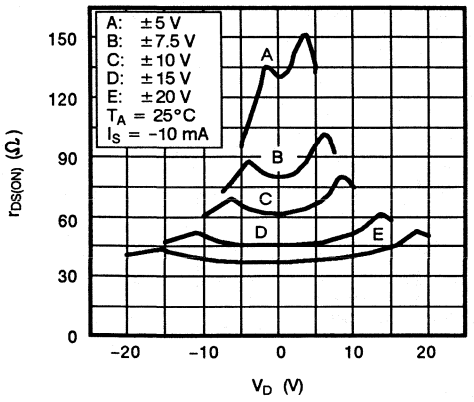
Pad No.	Function
1	IN_1
2	D_1
3	S_1
4	V-
5	GND
6	S_4
7	D_4
8	IN_4
9	IN_3
10	D_3
11	S_3
13	V+ (Substrate)
14	S_2
15	D_2
16	IN_2

ICMF* ***A = DG308A, *B = DG309**

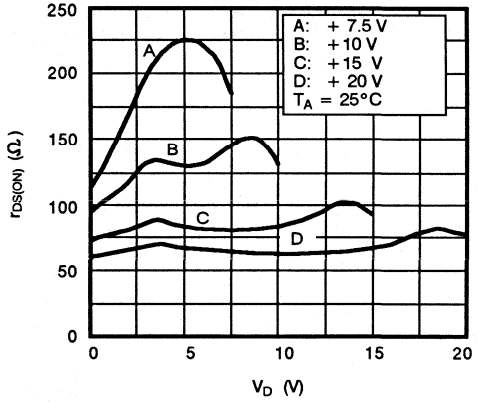
4 Resistors
8 Diodes
36 p-channel Depletion MOSFETs
40 n-channel Depletion MOSFETs

TYPICAL CHARACTERISTICS

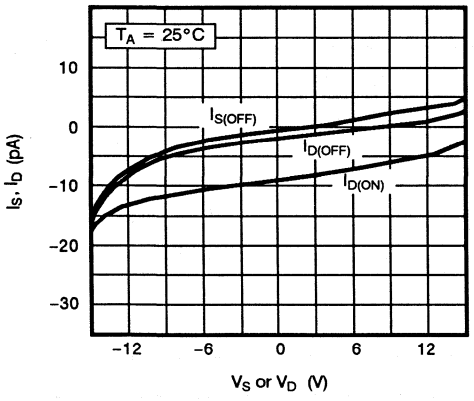
$r_{DS(ON)}$ vs. V_D and Power Supply



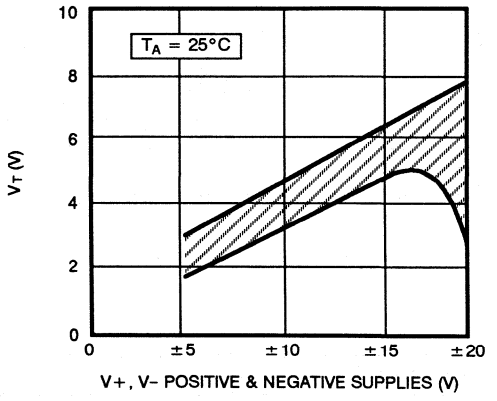
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage
V− = 0 V



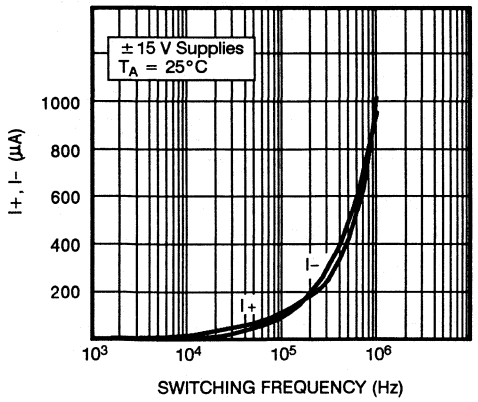
Leakage currents vs. Analog Voltage



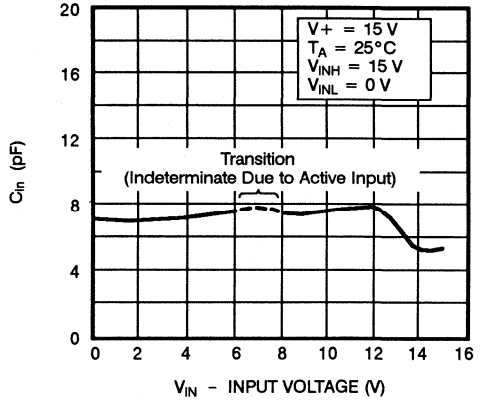
Input Switching Threshold vs. V+ and V− Supply Voltages



Supply currents vs. Switching Frequency
(All Inputs Active)



Input Capacitance vs. Input Voltage



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TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

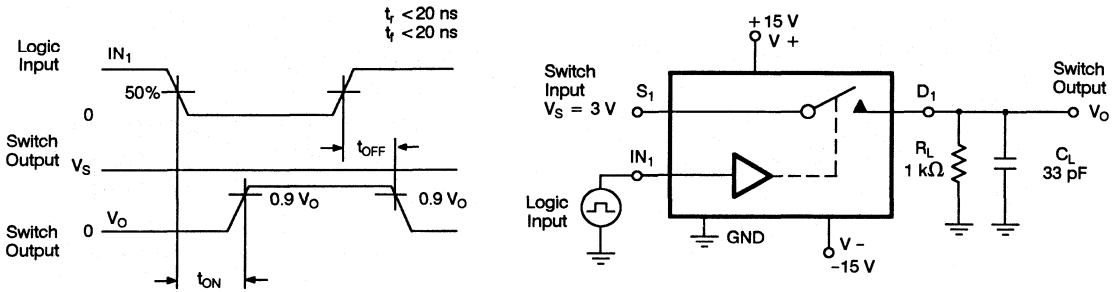


Figure 1. Switching Time

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

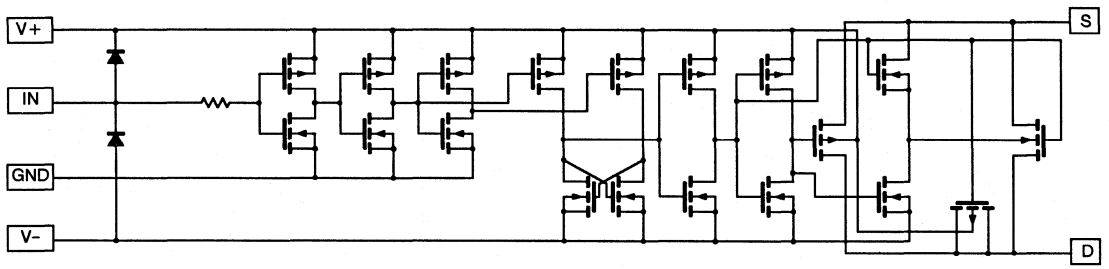


Figure 2.

APPLICATIONS

Single Supply Operation

The DG308A and DG309 will switch positive analog signals while using a single positive supply. This will allow use in many applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) Increased $r_{DS(ON)}$; 2) slower switching speed. typical curve for aid in designing with single supplies are supplied in the figure below. As stated in the absolute maximum ratings section of the data sheet, the analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 volts.

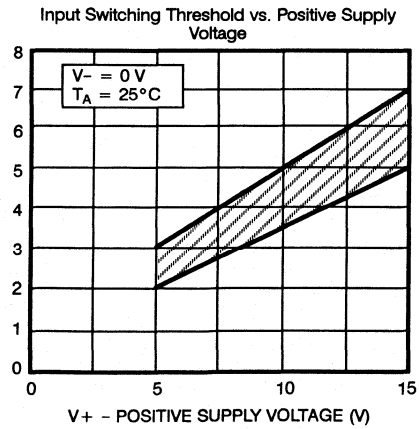


Figure 3.

Siliconix incorporated

DG381A/384A/387A/390A
General Purpose CMOS Analog Switches

FEATURES

- ±15 V Input Range
- Low $r_{DS(ON)}$ (<75 Ω)
- Single Supply Operation
- Pin and Function Compatible with the JFET DG180 Family

BENEFITS

- Full Rail-to-Rail Analog Signal Range
- Minimizes Signal Error
- Low Power Dissipation

APPLICATIONS

- Low Level Switching Circuits
- Programmable Gain Amplifiers
- Portable Battery Operation

DESCRIPTION

The DG38XA series of monolithic CMOS analog switches was designed for applications in instrumentation, communications, and process control. This series is suited for applications requiring fast switching and nearly flat ON resistance over the entire voltage range.

Designed on Siliconix' PLUS-40 CMOS process, the DG38XA series achieves low power consumption (3 mW typical) and excellent ON/OFF switch performance. This switch is ideal for battery powered applications, without sacrificing switching speed. Break-before-make switching action is guaranteed, and an epitaxial layer prevents latchup. Single supply operation is allowed by connecting the V- rail to 0 volts.

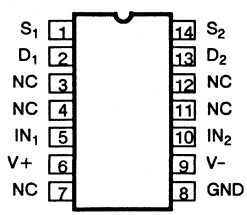
Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. These switches are quasi TTL and CMOS logic compatible.

Packaging for this series includes the 14-pin CerDIP for the DG381A/DG387A, and the 16-pin CerDIP for the DG384A/DG390A. A 10-pin metal can option is available for the DG387A. All devices are available in the plastic DIP version. Performance grades include the military, A suffix (-55 to 125°C), commercial, C suffix (0 to 70°C), and industrial, B suffix (-25 to 85°C) temperature ranges.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES

5

Dual-In-Line Package
Top View

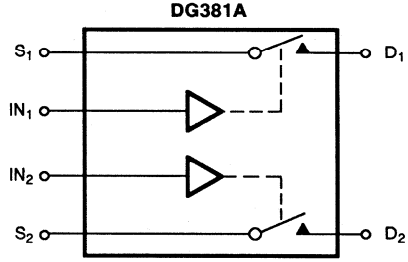


Order Numbers:

CerDIP: DG381AAK/883
DG381ABK

Plastic: DG381ACJ

DG381A



Two SPST Switches per Package**

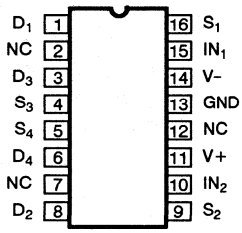
Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

**Switches Shown for Logic "1" Input

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS, AND TRUTH TABLES (Cont'd)

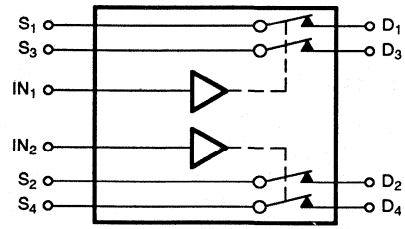
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG384AAK/883
Plastic: DG384ACJ

DG384A



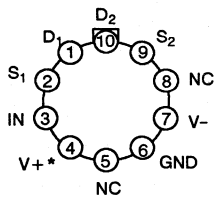
Two DPST Switches per Package**

Logic	Switch
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

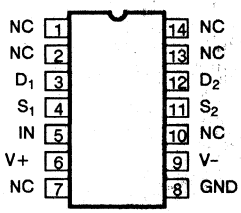
**Switches Shown for Logic "1" Input

Metal Can Package
Top View



Order Numbers:
DG387AAA/883
*(Substrate & Case)

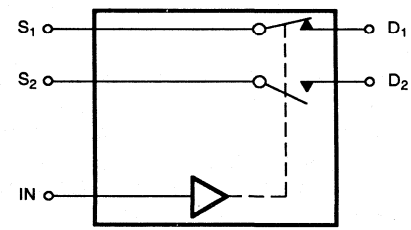
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG387AAK/883
Plastic: DG387ACJ

DG387A



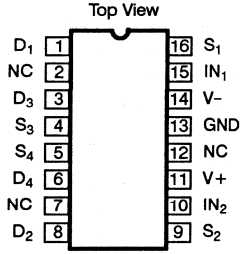
One SPDT Switch per Package**

Logic	SW_1	SW_2
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

**Switches Shown for Logic "1" Input

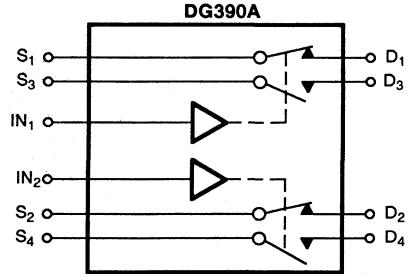
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG390AAK, DG390AAK/883
DG390ABK, DG390ACK
Plastic: DG390ACJ

DG390A



Two SPDT Switches per Package**

Logic	SW_1 SW_2	SW_3 SW_4
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

**Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[e], V_S, V_D ..... (V–) –2 V to (V+) +2V or 30 mA, whichever occurs first

Current, Any Terminal Except S or D ..... 30 mA

Continuous Current, S or D ..... 30 mA

(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA

Storage Temperature (A & B Suffix) ..... –65 to 150°C

(C Suffix) ..... –65 to 125°C

Operating Temperature (A Suffix) ..... –55 to 125°C

(B Suffix) ..... –25 to 85°C

(C Suffix) ..... 0 to 70°C

Power Dissipation*

14-Pin Cerdip (K)** ..... 825 mW

14-Pin Plastic DIP (J)*** ..... 470 mW

10-Pin Metal Can (A)**** ..... 450 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 11 mW/°C above 75°C.

***Derate 6.5 mW/°C above 25°C.

****Derate 6 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V– = –15 V, GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	D SUFFIX –40 to 85 °C MIN[b]	D SUFFIX –40 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}	I_S = 10 mA, V_{IN} = 0.8 V to 4 V[f]		Full		–15	15	–15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V_{IN} = 0.8 V or V_{IN} = 4 V[f]	V_D = 10 V, I_S = –10 mA	Room	30		50		50	Ω
				Full			75		75	
			V_D = –10 V, I_S = 10 mA	Room	30		50		50	
				Full			75		75	
Source OFF leakage Current	$I_{S(OFF)}$		V_S = 14 V, V_D = –14 V	Room	0.1		1		5	nA
				Hot			100		100	
			V_S = –14 V, V_D = 14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain OFF Leakage Current	$I_{D(OFF)}$		V_S = –14 V, V_D = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_S = 14 V, V_D = –14 V	Room	–0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
Drain On Leakage Current	$I_{D(ON)}$		V_D = V_S = 14 V	Room	0.1	–1	1	–5	5	
				Hot		–100	100	–100	100	
			V_D = V_S = –14 V	Room	–0.1	–2	2	–5	5	
				Hot		–200	200	–200	200	
DIGITAL CONTROL										
Input Current with Input Voltage HIGH	I_{INH}	V_{IN} = 5 V		Room	–0.001	–1		–1		µA
				Full		–1				
		V_{IN} = 15 V		Room	0.001		1		1	
				Full			1			
Input Current with Input Voltage LOW	I_{INL}	V_{IN} = 0 V		Room	–0.001	–1		–1		
				Full		–1				
DYNAMIC CHARACTERISTICS										
Turn-ON Time	t_{ON}	See Switching Test Time Circuit		Room	150		300			ns
Turn-OFF Time	t_{OFF}			Room	130		250			
Break-Before-Make Time	t_{BBM}	See Break-Before-Make Test Circuit DG387A/390A ONLY		Room	50					
Charge Injection	Q	C_L = 0.01 µF, R_{gen} = 0 Ω, V_{gen} = 0 V		Room	10					pC

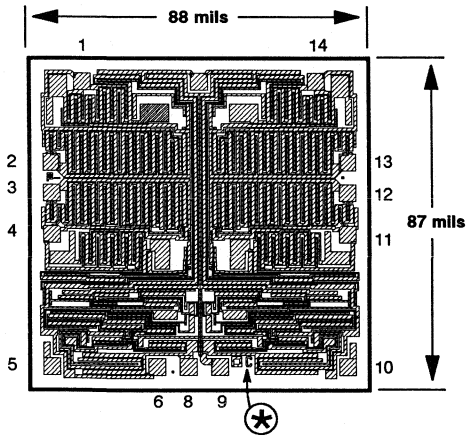
5

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)										
Source-OFF Capacitance	$C_{S(OFF)}$	V_{IN} = 0.8 V or	V_S = 0 V	Room	14					pF
Drain-OFF Capacitance	$C_{D(OFF)}$	V_{IN} = 4 V	V_D = 0 V	Room	14					
Channel-ON Capacitance	$C_{D + S(ON)}$	f = 1 MHz	$V_S = V_D$ = 0 V	Room	40					
Input Capacitance	C_{in}	f = 1 MHz	V_{IN} = 0 V	Room	6					
			V_{IN} = 15 V	Room	7					
OFF-Isolation[f]		V_{IN} = 0 V, R_L = 1 kΩ		Room	62					dB
Crosstalk (Channel-to-Channel)		V_S = 1 V_{rms}, f = 500 kHz		Room	74					
POWER SUPPLIES										
Positive Supply Current	I+	V_{IN} = 4 V (One Input)		Room Full	0.23		0.5 1.0		1	mA
Negative Supply Current	I-	(All Others = 0)		Room Full	-0.001	-10 -100		-100		µA
Positive Supply Current	I+	V_{IN} = 0.8 V (All Inputs)		Room Full	0.001		10 100		100	
Negative Supply Current	I-			Room Full	-0.001	-10 -100		-100		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Signals S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
f. OFF-isolation: 20 log $\frac{V_S}{V_D}$ V_S = input to OFF switch, V_D = output.
g. V_{IN} = input voltage to perform proper function.
h. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY

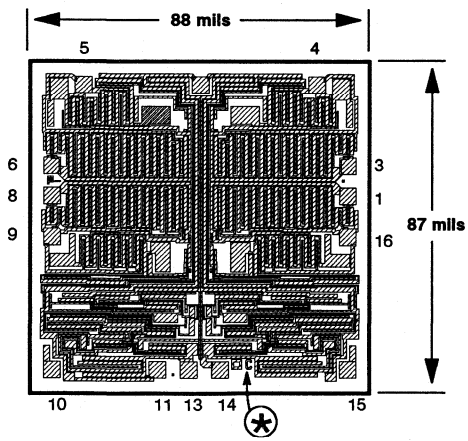


Pad No.	Function DG381A
1	S_1
2	D_1
3	NC
4	NC
5	IN_1
6	V+
8	GND
9	V–
10	IN_2
11	NC
12	NC
13	D_2
14	S_2

Pad No.	Function DG387A
1	NC
2	NC
3	D_1
4	S_1
5	IN
6	V+
8	GND
9	V–
10	NC
11	S_2
12	D_2
13	NC
14	NC

ICMJC ***C = DG381A**
4 Capacitors — 18 p-channel Depletion MOSFETs
2 Resistors — 22 n-channel Depletion MOSFETs
4 Diodes

ICMJB ***B = DG387A**
4 Capacitors — 11 p-channel Depletion MOSFETs
1 Resistor — 15 n-channel Depletion MOSFETs
2 Diodes



Pad No.	Function DG384A
1	D_1
3	D_3
4	S_3
5	S_4
6	D_4
8	D_2
9	S_2
10	IN_2
11	V+
13	GND
14	V–
15	IN_1
16	S_1

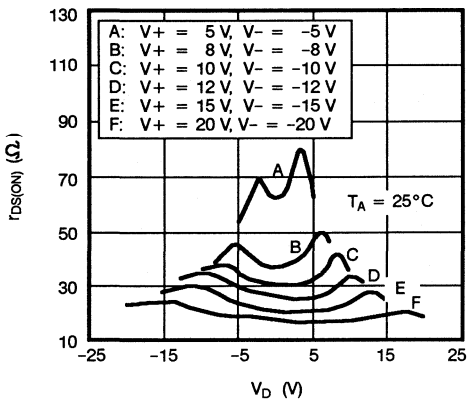
Pad No.	Function DG390A
1	D_1
3	D_3
4	S_3
5	S_4
6	D_4
8	D_2
9	S_2
10	IN_2
11	V+
13	GND
14	V–
15	IN_1
16	S_1

ICMJA ***A = DG384A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes

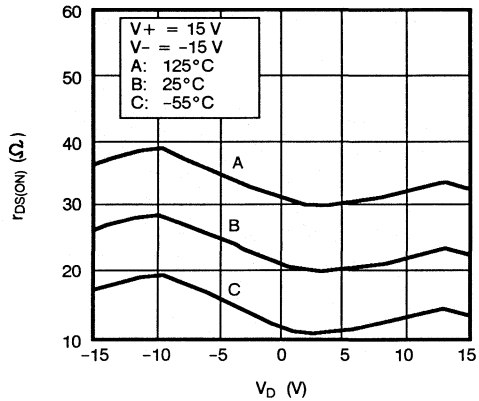
ICMJC ***C = DG390A**
8 Capacitors — 22 p-channel Depletion MOSFETs
2 Resistors — 30 n-channel Depletion MOSFETs
4 Diodes

TYPICAL CHARACTERISTICS

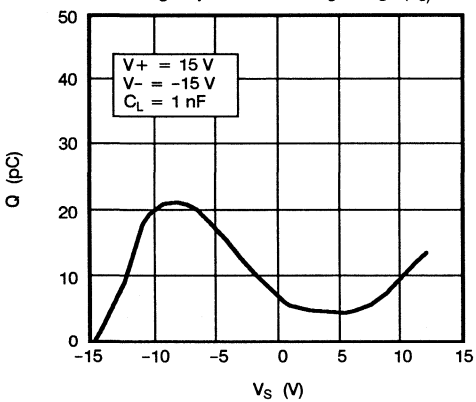
$r_{DS(ON)}$ vs. V_D and Power Supply



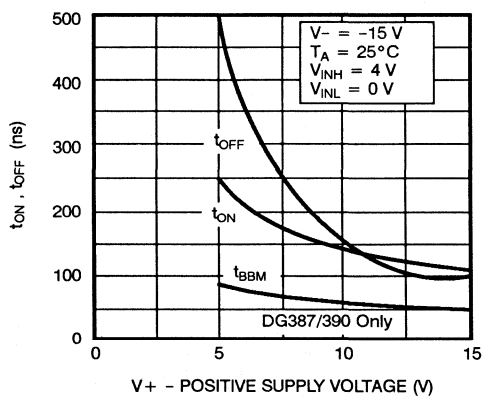
$r_{DS(ON)}$ vs. V_D and Temperature



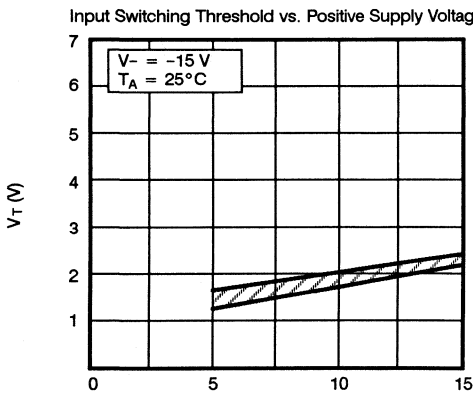
Charge Injection vs. Analog Voltage (V_S)



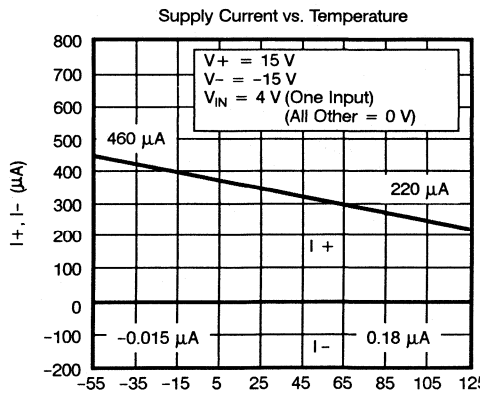
Switching Time and Break-Before-Make Time vs. Positive Supply Voltage



Input Switching Threshold vs. Positive Supply Voltage

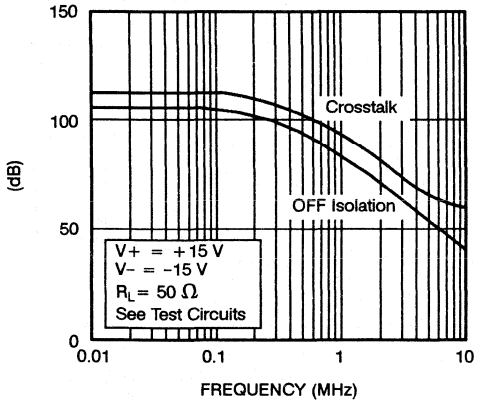


Supply Current vs. Temperature

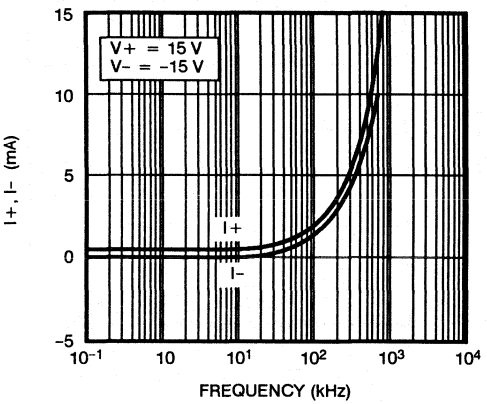


TYPICAL CHARACTERISTICS (Cont'd)

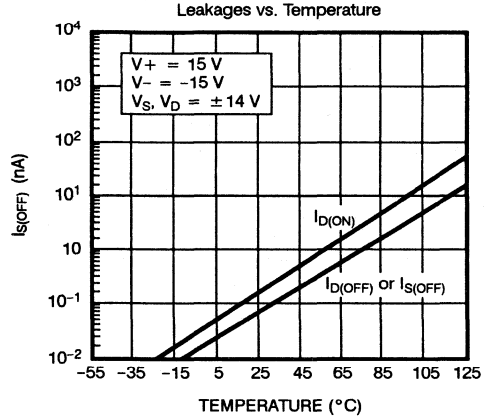
Off Isolation and Crosstalk vs. Frequency



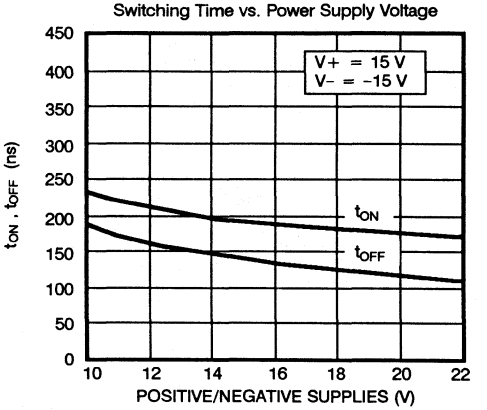
Supply Currents vs. Switching Frequency



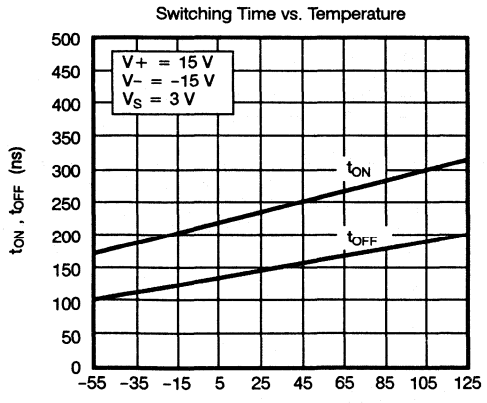
Leakages vs. Temperature



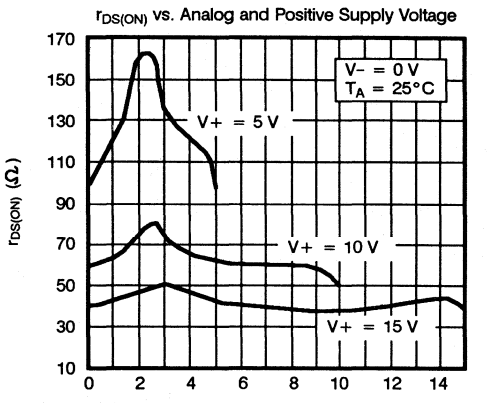
Switching Time vs. Power Supply Voltage



Switching Time vs. Temperature



rDS(ON) vs. Analog and Positive Supply Voltage



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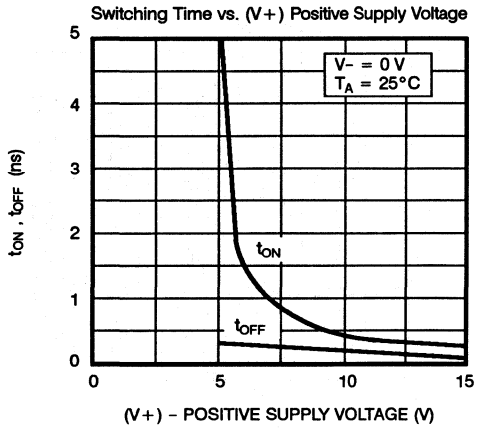
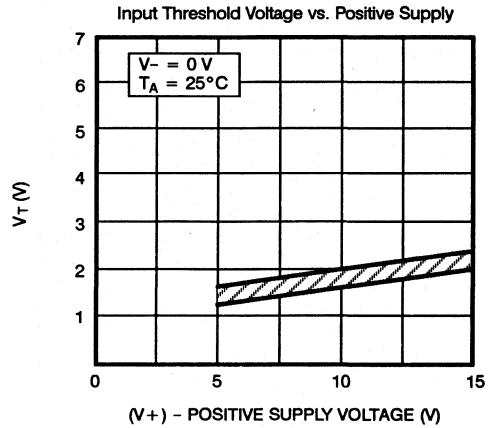
TYPICAL CHARACTERISTICS (Cont'd)





TEST CIRCUITS

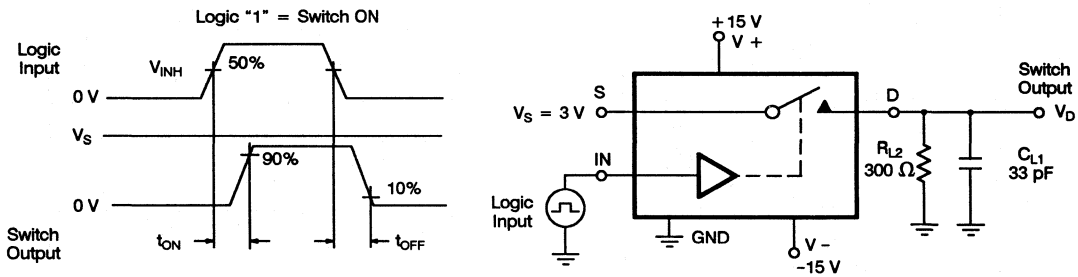


Figure 1. Switching Time

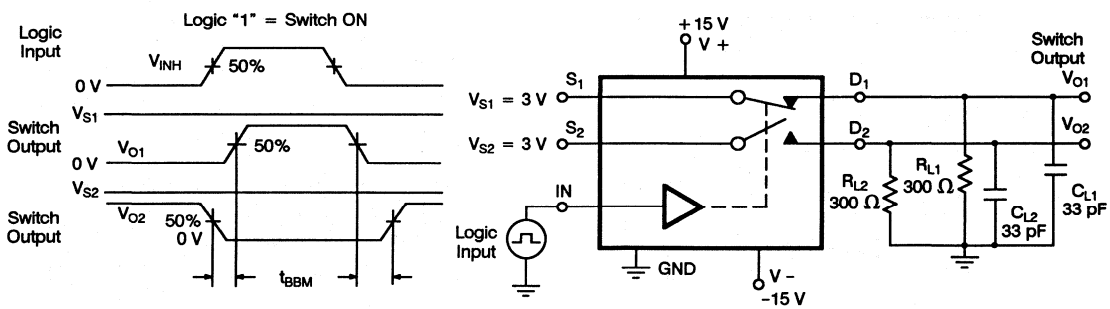


Figure 2. Break-Before-Make SPDT (DG387A, DG390A)

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

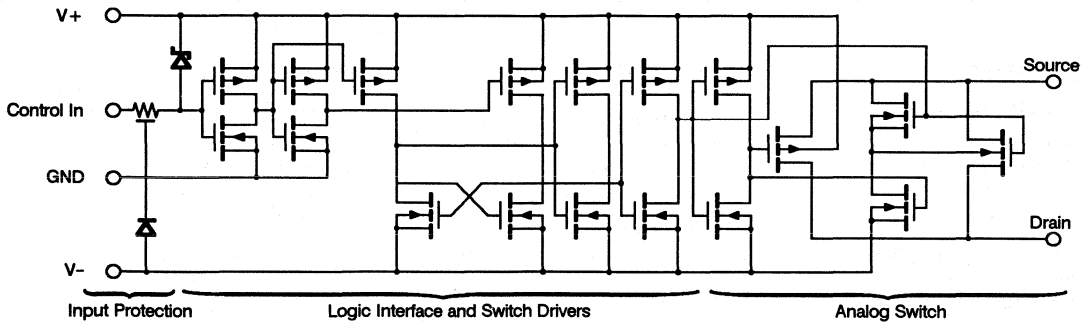


Figure 3.

APPLICATIONS

The DG38XA series of analog switches will switch positive analog signals while using a single positive supply. This allows their use in applications where only one supply is available. The trade-offs or performance given up while using single supplies are: 1) increased $r_{DS(ON)}$, 2) slower switching speed. Typical curves for aid in designing with single supplies are supplied (see Typical Characteristics). The analog voltage should not go above or below the supply voltages which in single operation are V+ and 0 volts.

In the integrator of Figure 4, R_D controls the discharge rate of the capacitor so that the pulsed or continuous current ratings are not exceeded. During reset SW_1 is closed and SW_2 is open. Opening SW_2 with SW_1 also open will hold the integrator output at its present value.

5

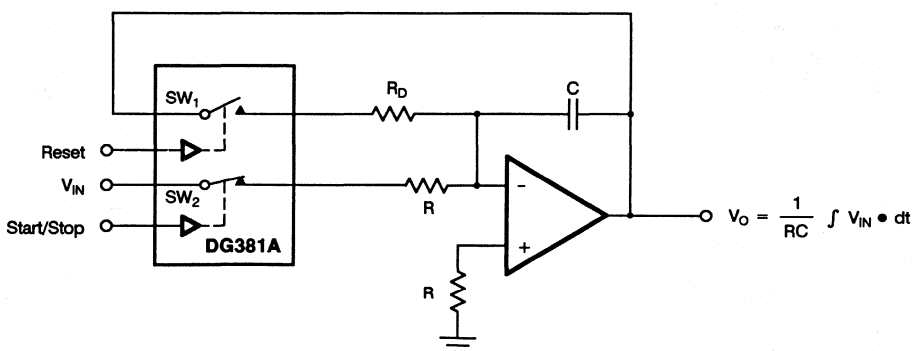


Figure 4. Inegrator with Reset and Start/Stop

DG401/403/405
Low-Power – High-Speed CMOS Analog Switches

Siliconix incorporated

FEATURES

- ± 15 V Input Range
- ON-resistance < 35 Ω
- Fast Switching Action
  t_{ON} < 150 ns
  t_{OFF} < 100 ns
- Ultra Low Power Requirements
  (P_D < 35 μW)
- TTL, CMOS Compatible

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- High Performance Audio and Video Switching
- Sample and Hold Circuits
- Battery Operation

DESCRIPTION

The DG401 Series of monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (< 35 μW) with high speed (t_{ON} < 150 ns), the DG401 Series is ideally suited for portable and battery powered industrial and military applications.

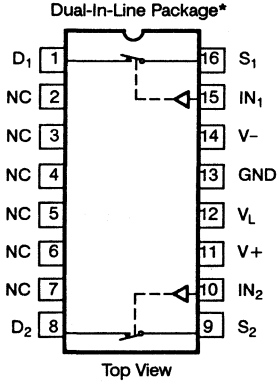
Built on the Siliconix proprietary high voltage silicon gate process to achieve high voltage rating and superior switch ON/OFF performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is very flat over the full ± 15 V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams. Package options are the 16-pin plastic or CerDIP. Performance grades include industrial, D suffix (-40 to 85°C), and military, A suffix (-55 to 125°C). Additionally, the DG403 and DG405 are available in the narrow body surface mount package, SO-16.

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package*



Top View

Order Numbers:

CerDIP: DG401AK
DG401AK/883
Plastic: DG401DJ

*Switches shown for logic "1" input

DG401

Two SPST Switches per Package

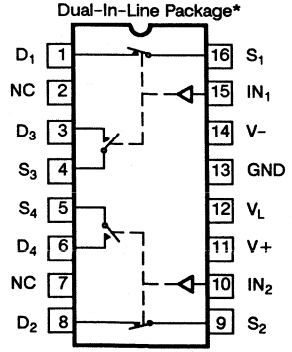
Truth Table*

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE (Cont'd)

Dual-In-Line Package*

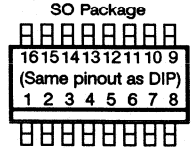


Top View

Order Numbers:

CerDIP: DG403AK
DG403AK/883
Plastic: DG403DJ

SO Package



Top View

Order Number:
DG403DY

DG403

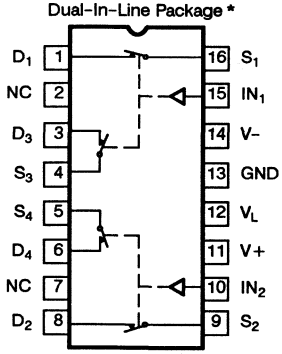
Two SPDT Switches per Package

Truth Table*

Logic	Switch 1 Switch 2	Switch 3 Switch 4
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

Dual-In-Line Package *

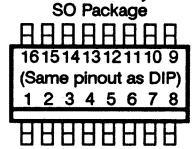


Top View

Order Numbers:

CerDIP: DG405AK
DG405AK/883
Plastic: DG405DJ

Narrow Body
SO Package



Top View

Order Number:
DG405DY

DG405

Two DPST Switches per Package

Truth Table*

Logic	Switch
0	OFF
1	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

*Switches shown for logic "1" input

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
GND to V- ..... 25 V
V_L ..... (GND - 0.3 V) to (V+) +0.3 V
Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+ plus 2 V)
or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin CerDIP*** ..... 900 mW
16-Pin SO**** ..... 600 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C
***Derate 12 mW/°C above 75°C
****Derate 7.6 mW/°C above 75°C

[1]Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

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Siliconix incorporated

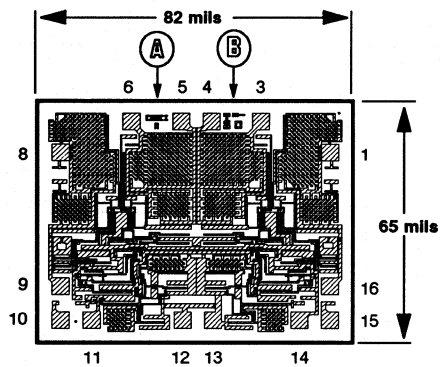
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[d]	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V I_S = -10 mA, V_D = ±10 V	Room Full	20		35 45		45 55	Ω
Delta Drain-Source ON-resistance	$\Delta r_{DS(ON)}$	V+ = 16.5 V, V- = -16.5 V I_S = -10 mA, V_D = 5, 0, -5 V	Room Full	3		3 5		3 5	
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Full	-0.01	-0.25 -20	0.25 20	-0.5 -20	0.5 20	nA
	$I_{D(OFF)}$		Room Full	-0.01	-0.25 -20	0.25 20	-0.5 -20	0.5 20	
Channel ON Leakage Current	$I_{D(ON)}$	V± = ±16.5 V V_D = V_S = ±15.5 V	Room Full	-0.04	-0.4 -40	0.4 40	-1 -40	1 40	
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Full	0.005	-1	1	-1	1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Full	0.005	-1	1	-1	1	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF	Room	100		150		150	ns
Turn-OFF Time	t_{OFF}	See Figure 1A	Room	60		100		100	
Break-Before-Make Time Delay (DG403)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	20	10		10		
Charge Injection	Q	C_L = 10,000 pF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
OFF Isolation Reject Ratio	DIRR	R_L = 100 Ω, C_L = 5 pF f = 1 MHz	Room	72					dB
Crosstalk (Channel-to-Channel)	CCRR	R_L = 100 Ω, C_L = 5 pF f = 1 MHz	Room	90					
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 0 V	Room	12					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	12					
Channel ON Capacitance	$C_{D+S(ON)}$		Room	39					
POWER SUPPLIES									
Positive Supply Curent	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V	Room Full	0.01		1 5		1 5	µA
Negative Supply Current	I-		Room Full	-0.01	-1 -5		-1 -5		
Logic Supply Current	I_L		Room Full	0.01		1 5		1 5	
Ground Current	I_{GND}		Room Full	-0.01	-1 -5		-1 -5		

SPECIFICATIONS[a] (Cont'd)

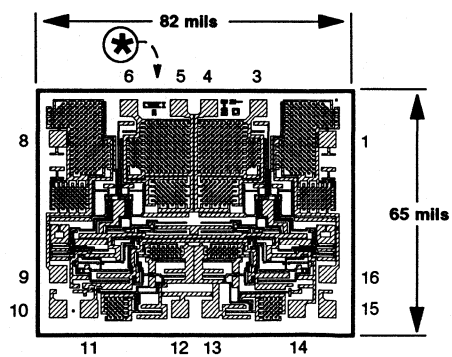
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Full = as determined by the operating temperature suffix.

DIE TOPOGRAPHIES



Pad No.	Function
1	D_1
2	NC
3	NC
4	NC
5	NC
6	NC
7	NC
8	D_2
9	S_2
10	IN_2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

CSHCA/B = DG401
4 Capacitors
4 Resistors
16 p-channel enhancement MOSFETs
20 n-channel enhancement MOSFETs
4 Diodes



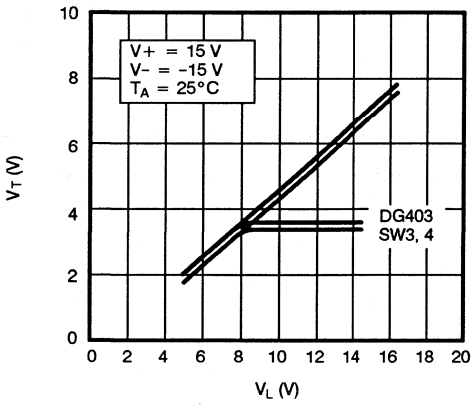
Pad No.	Function
1	D_1
2	NC
3	D_3
4	S_3
5	S_4
6	D_4
7	NC
8	D_2
9	S_2
10	IN_2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

CSHC*
8 Capacitors
4 Resistors
22 p-channel enhancement MOSFETs
30 n-channel enhancement MOSFETs
4 Diodes
*A = DG403
B = DG405

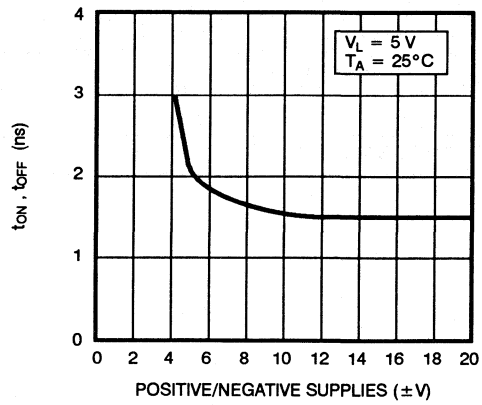
5

TYPICAL CHARACTERISTICS

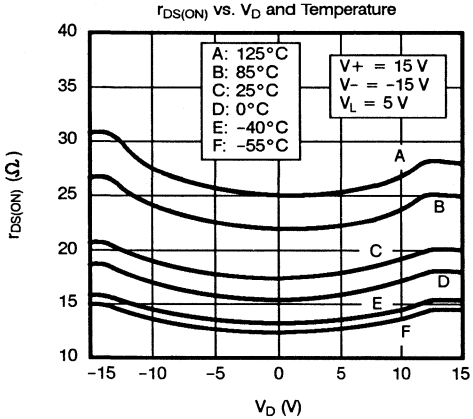
Input Switching Threshold vs. Logic Supply Voltage



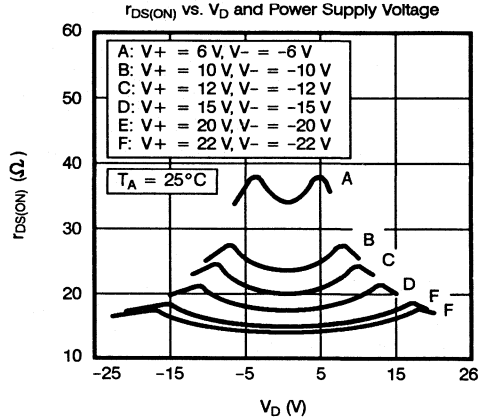
Input Switching Threshold vs. Power Supply Voltage



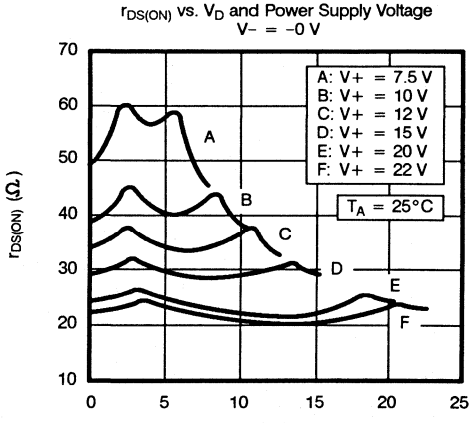
$r_{DS(ON)}$ vs. V_D and Temperature



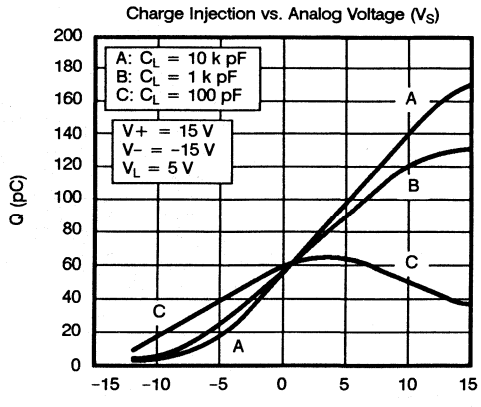
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



$r_{DS(ON)}$ vs. V_D and Power Supply Voltage
V- = -0 V

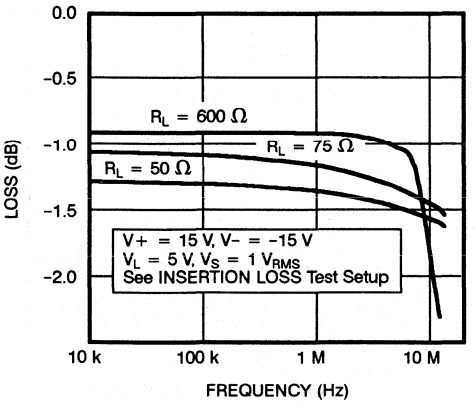


Charge Injection vs. Analog Voltage (V_S)

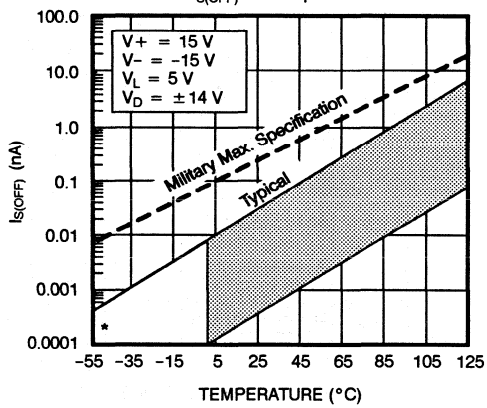


TYPICAL CHARACTERISTICS (Cont'd)

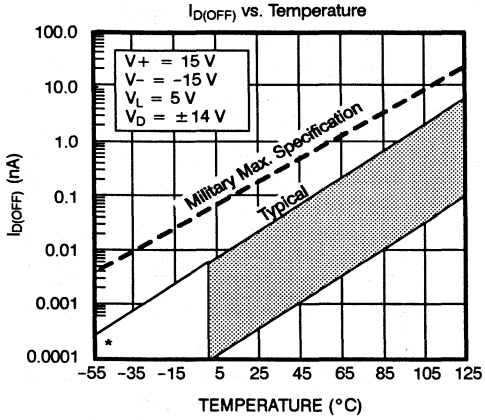
Insertion Loss vs. Frequency



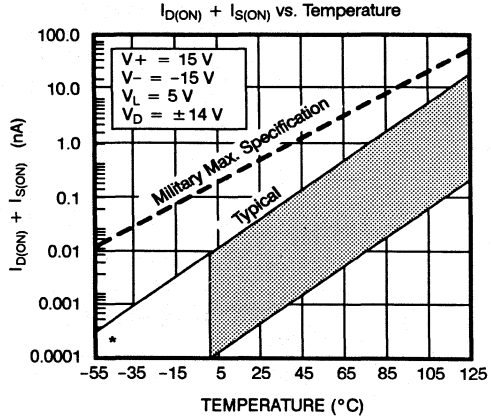
$I_{S(OFF)}$ vs. Temperature



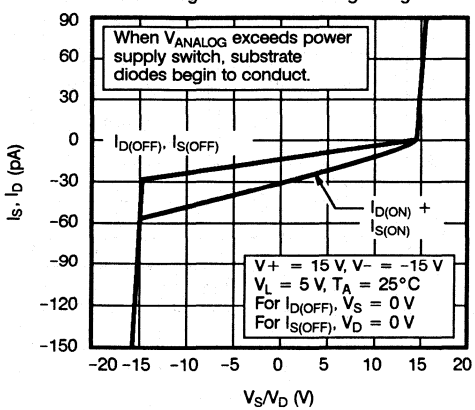
$I_{D(OFF)}$ vs. Temperature



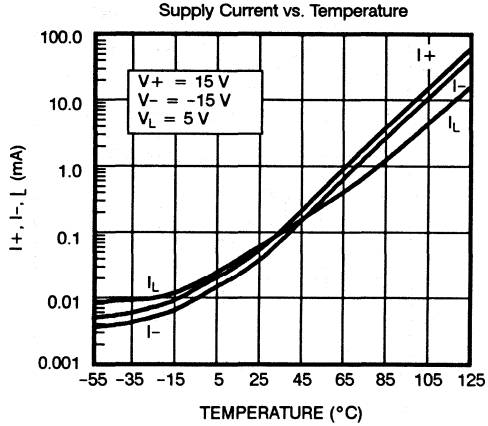
$I_{D(ON)}$ + $I_{S(ON)}$ vs. Temperature



Leakage Current vs. Analog Voltage



Supply Current vs. Temperature

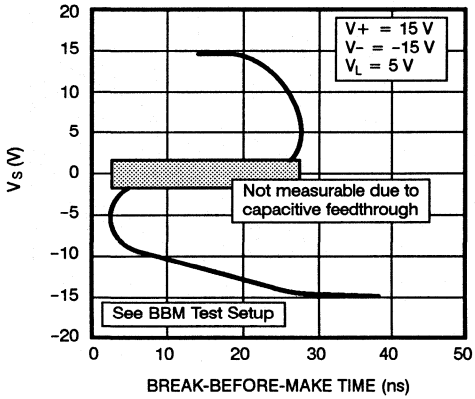


*Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin1-to-pin below the dew point (where water condenses).

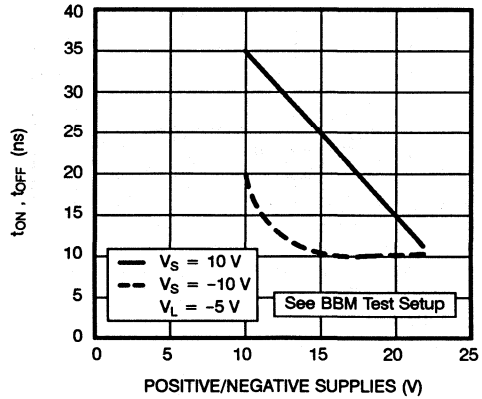
5

TYPICAL CHARACTERISTICS (Cont'd)

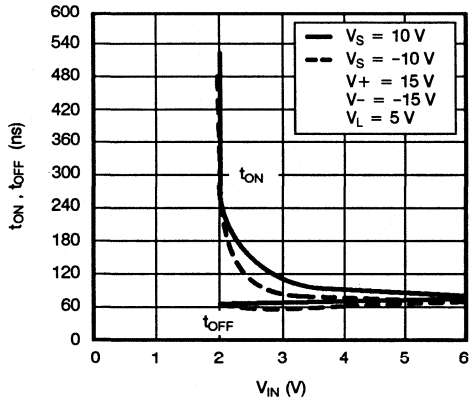
Break-Before-Make vs. Analog Voltage



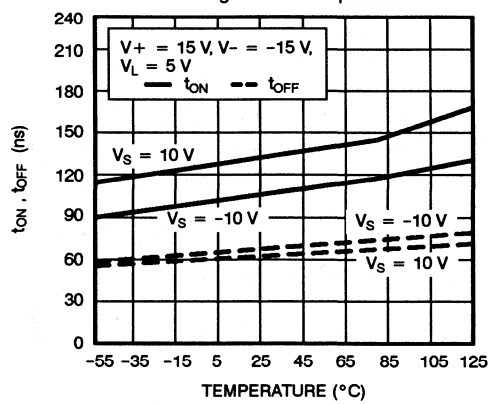
Break-Before-Make vs. Power Supply Voltage



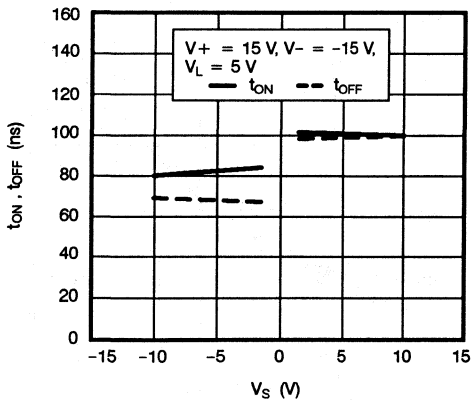
Switching Time vs. Input Logic Voltage (V_{IN})*



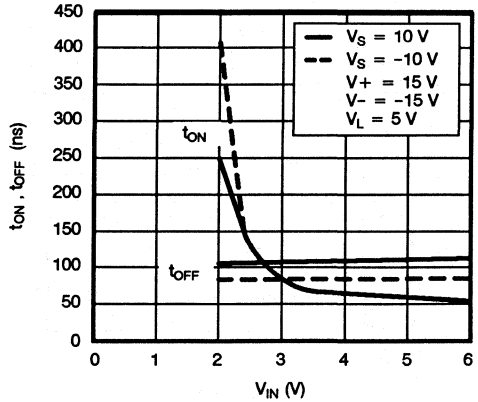
Switching Time vs. Temperature*



Switching Time vs. Analog Voltage*



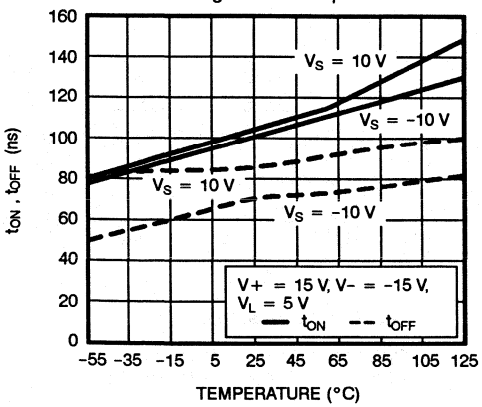
Switching Time vs. Input Logic Voltage (V_{IN})*



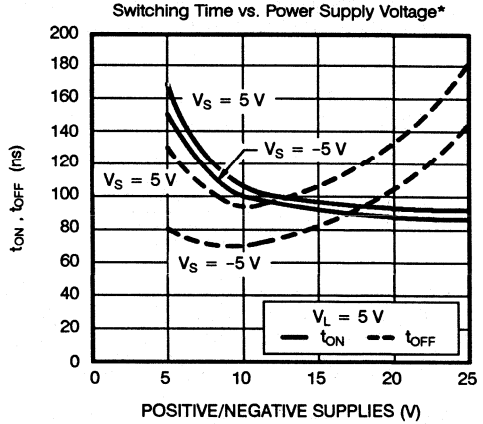
*Refer to Figure 1 for test conditions.

TYPICAL CHARACTERISTICS (Cont'd)

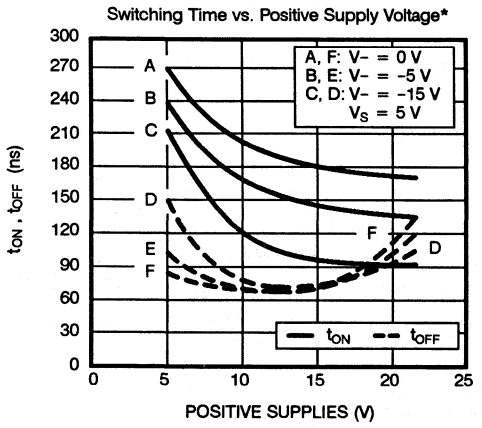
Switching Time vs. Temperature*



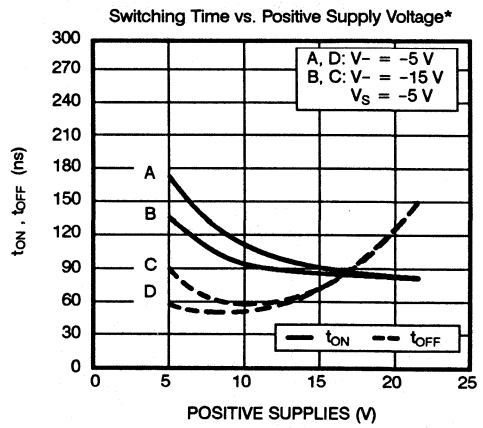
Switching Time vs. Power Supply Voltage*



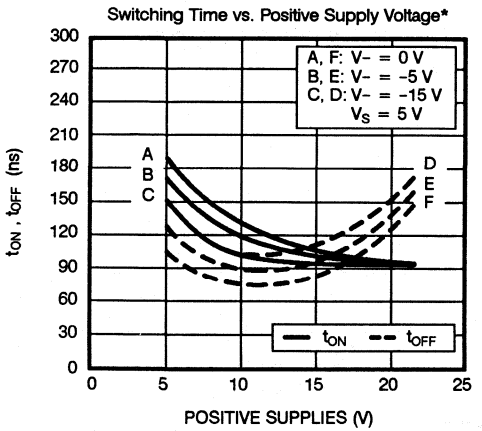
Switching Time vs. Positive Supply Voltage*



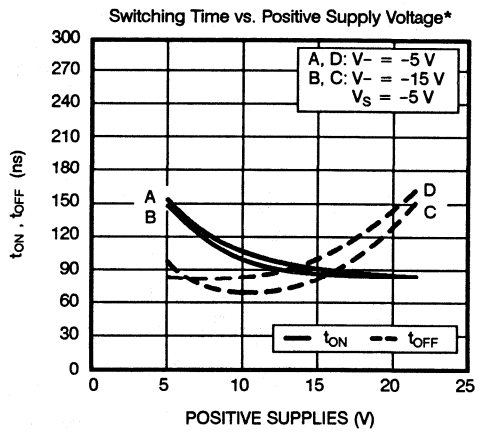
Switching Time vs. Positive Supply Voltage*



Switching Time vs. Positive Supply Voltage*



Switching Time vs. Positive Supply Voltage*

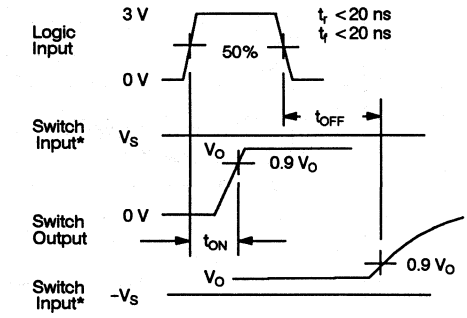


*Refer to Figure 1 for test conditions.

5

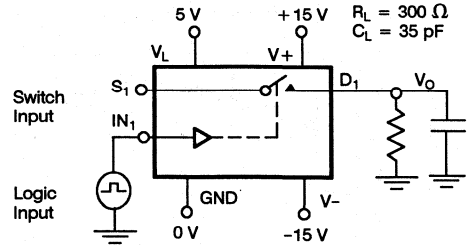
TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



*V_S = 10 V for t_{ON}, V_S = −10 V for t_{OFF}

Note: Logic input waveform is inverted for switches that have the opposite logice sense control

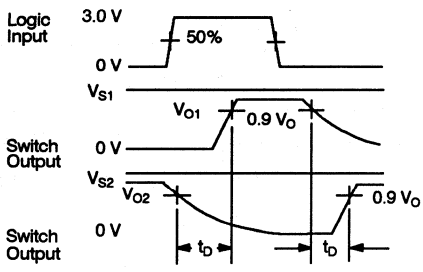


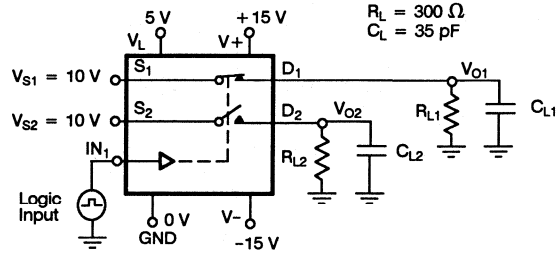
Repeat test for IN_2 and S_2

For load conditions, see Specifications
C_L includes fixture and stray capacitance

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

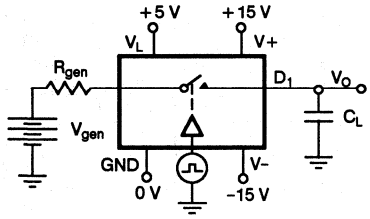
Figure 1. Switching Times





C_L includes fixture and stray capacitance

Figure 2. Break-Before-Make



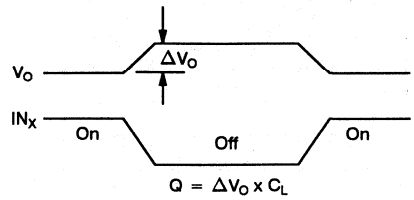
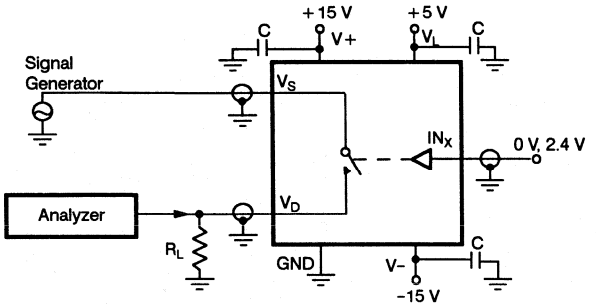


Figure 3. Charge Injection

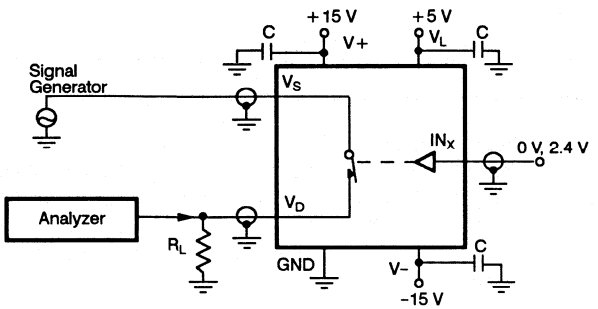
TEST CIRCUITS (Cont'd)



Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

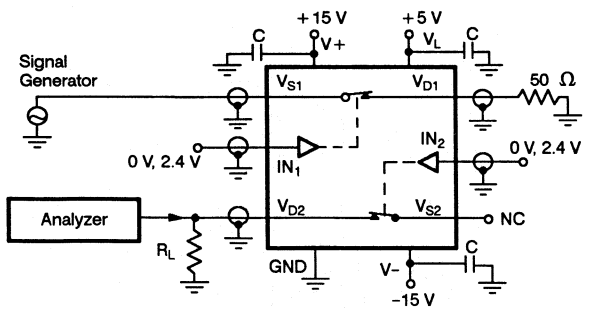
$$\text{Off Isolation} = 20 \log \frac{V_D}{V_S}$$

Figure 4. Off Isolation



Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

Figure 5. Insertion Loss



Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

$$\text{Crosstalk} = 20 \log \frac{V_{D2}}{V_{S1}}$$

Figure 6. Crosstalk

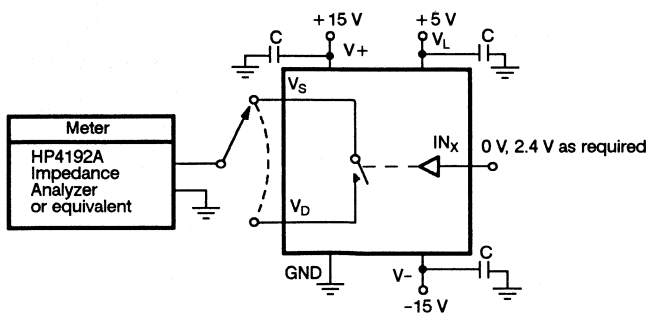


Figure 7. Capacitances

SCHEMATIC DIAGRAM (Typical Channel)

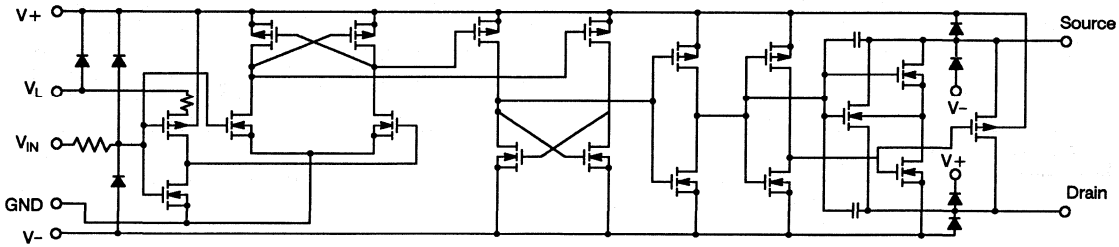


Figure 8.

APPLICATIONS

Stereo Source Selector:
A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low ON-resistance (<35 Ω) minimizes total harmonic distortion.

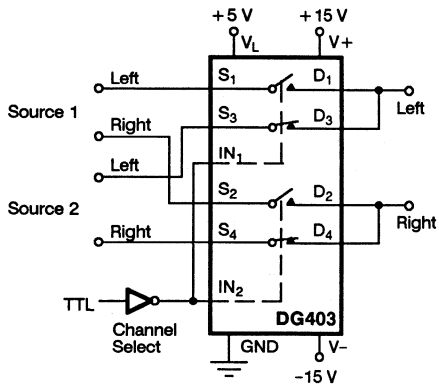


Figure 9. Stereo Source Selector

Dual Slope Integrators:
The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

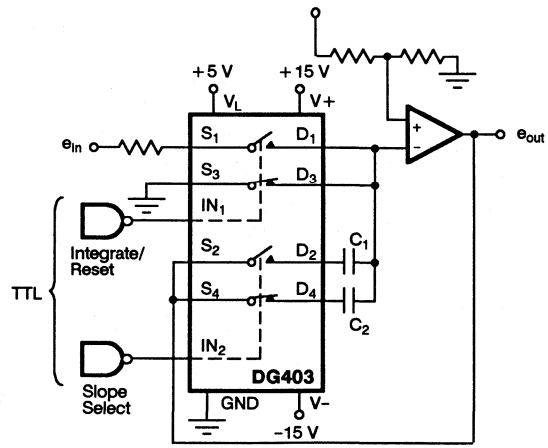


Figure 10. Dual Slope Integrator

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

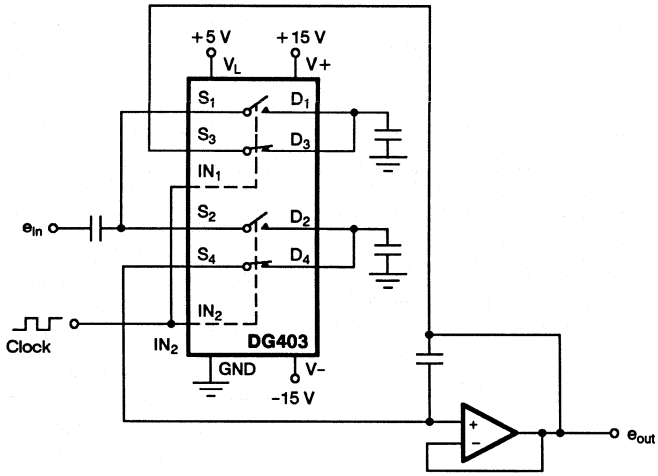


Figure 11. Band-pass Switched Capacitor Filter

Peak Detector:

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input e_{in}. If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{in} goes below e_{out} of A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

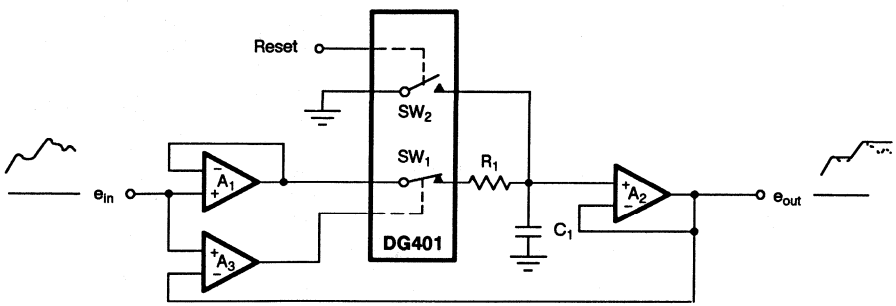


Figure 12. Positive Peak Detector

DG406/407
16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

Siliconix incorporated

FEATURES

- Low $r_{DS(ON)}$ (100 Ω max)
- Low Charge Injection (Q <20 pC typ.)
- Fast Transition Time (250 ns max)
- Low Power (I_{SUPPLY} <75 µA)
- Single Supply Capability
- ESD Protection > ±4000 V

BENEFITS

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness

APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing and Multiplexing/Demultiplexing
- ATE Systems
- Battery Operated Systems
- High Rel Systems
- Single Supply Systems

DESCRIPTION

The DG406 is a 16-channel single-ended analog multiplexer designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address. The DG407 is an 8-channel differential analog multiplexer designed to connect 1 of 8 differential inputs to a common dual output as determined by its 3-bit binary address. Break-before-make switching action protects against momentary shorting of inputs.

An ON channel conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF for stacking several devices. All control inputs, address (A_X) and enable (EN) are TTL compatible over the full specified operating temperature range.

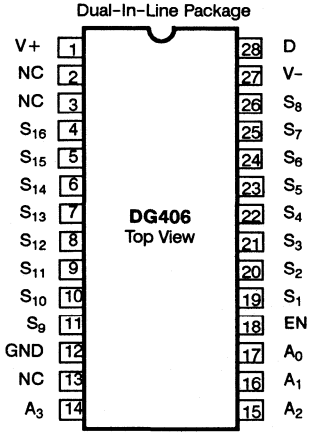
Applications for the DG406/407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with ±20-Volt supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

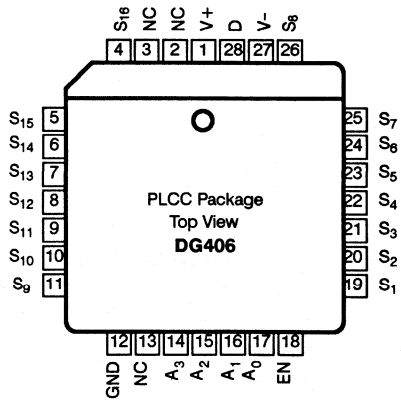
Both DG406 and DG407 are available in dual-in-line ceramic and plastic packages and are specified for operation over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

PIN CONFIGURATION

Dual-In-Line Package

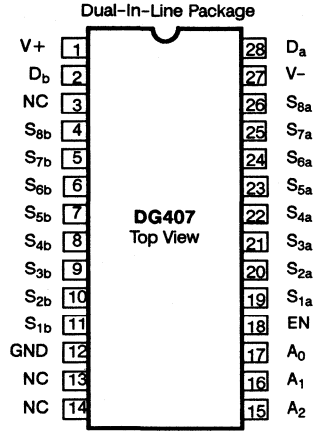


Order Numbers:
CerDIP: DG406AK
Plastic: DG406DJ



Order Number:
DG406DN

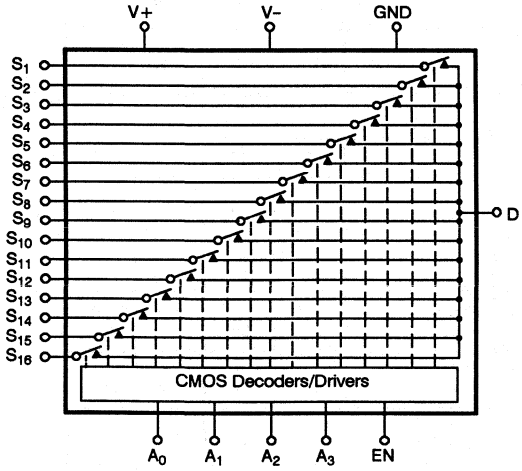
Dual-In-Line Package



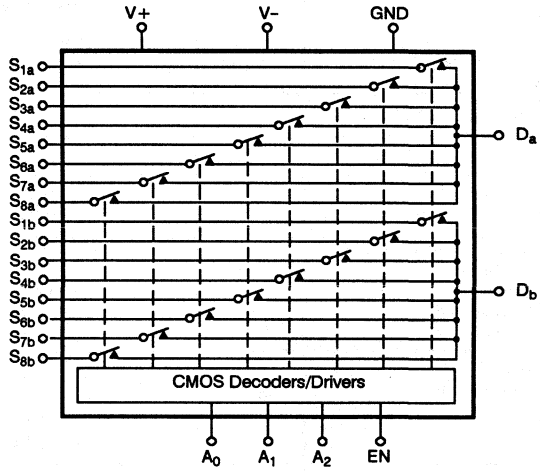
Order Numbers:
CerDIP: DG407AK
Plastic: DG407DJ

Preliminary

FUNCTIONAL BLOCK DIAGRAM



DG406
16-Channel Single Ended Multiplexer



DG407
Differential 8-Channel Multiplexer

A_3	A_2	A_1	A_0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

A_2	A_1	A_0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V, Logic "1" = $V_{AH} \geq 2.4$ V

5

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs [h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.

Current (Any Terminal, Except S or D) ..... 30 mA

Continuous Current, S or D ..... 20 mA

Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Power Dissipation (Package)*

28-Pin Ceramic DIP** ..... 1200 mW

28-Pin Plastic DIP*** ..... 625 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6 mW/°C above 75°C.

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V		TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	V_D = ±10 V I_S = -1 mA		Room Full	50		100 125		100 125	Ω
$r_{DS(ON)}$ Matching Between Channels[f]		$\Delta r_{DS(ON)}$	V_D = 10 V, -10 V		Room			15		15	
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V V_D = ∓10 V	Room Full		-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA
Drain OFF Leakage Current	DG406	$I_{D(OFF)}$		V_D = ±10 V V_S = ∓10 V	Room Full		-2 -200	2 200	-2 -200	2 200	
	DG407			V_D = ±10 V V_S = ∓10 V	Room Full		-2 -100	2 100	-2 -100	2 100	
Drain ON Leakage Current	DG406	$I_{D(ON)}$	V_S = V_D = ±10 V Sequence Each Swtich ON		Room Full		-2 -200	2 200	-2 -200	2 200	
	DG407				Room Full		-2 -100	2 100	-2 -100	2 100	
DIGITAL CONTROL											
Logic High Input Current		I_{AH}	V_A = 2.4 V, 15 V		Full		-10	10	-10	10	µA
Logic Low Input Current		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		-10	10	-10	10	
DYNAMIC CHARACTERISTICS											
Transition Time		t_{TRANS}	See Figure 1		Room			250		250	ns
Break-Before-Make Interval		t_{OPEN}	See Figure 3		Room		10		10		
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 2		Room			200		200	
Enable Turn-OFF Time		$t_{OFF(EN)}$			Room			150		150	
Charge Injection		Qi	C_L = 1 nF, V_S = 0 V, R_s = 0 Ω		Room	20					pC
OFF Isolation[g]			V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz		Room	-65					dB
Logic Input Capacitance		C_{in}	f = 1 MHz		Room	8					pF
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0 V f = 1 MHz	V_S = 0 V	Room	11					
Drain OFF Capacitance	DG406	$C_{D(OFF)}$		V_D = 0 V	Room	70					
	DG407				Room	35					
Drain ON Capacitance	DG406	$C_{D(ON)}$			Room	100					
	DG407				Room	50					

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0 V	Full			75		75	µA
Negative Supply Current	I-		Full		-5		-5		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V	Room Full			0.5 2		0.5 2	mA
Negative Supply Current	I-		Full		-500		-500		µA

SPECIFICATIONS[a] **(Single Supply)**

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Drain-Source ON Resistance[e]	$r_{DS(ON)}$	V_D = 3 V, 10 V I_S = - 1 mA	Room	90					Ω
DYNAMIC CHARACTERISTICS									
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V V_{IN} = 2.4 V	Room	300					ns
Enable Turn ON Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V	Room	250					
Enable Turn OFF Time	$t_{OFF(EN)}$	V_{S1} = 5 V	Room	150					
Charge Injection	Q	C_L = 1 nF, V_S = 6 V, R_S = 0 Ω	Room	5					pC

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = r_{DS(ON)}$ MAX - $r_{DS(ON)}$ MIN
g. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
h. Signals on S_X, D_X, on IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. Room = 25°C, Full = as determined by the operating temperature suffix.

5

DG408/409
8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

Siliconix incorporated

FEATURES

- Low $r_{DS(ON)}$ (100 Ω max)
- low Charge Injection (Q <20 pC typ.)
- Fast Transition Time (250 ns max)
- Low Power (I_{SUPPLY} <75 µA)
- Single Supply Capability

BENEFITS

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness

APPLICATIONS

- Data Acquisition Systems
- Audio Signal Routing and Multiplexing/Demultiplexing
- ATE Systems
- Battery Operated Systems
- High Rel Systems
- Single Supply Systems

DESCRIPTION

The DG408 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a 4-channel differential analog multiplexer designed to connect 1 of 4 differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An ON channel conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF for stacking several devices. All control inputs, address (A_X) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

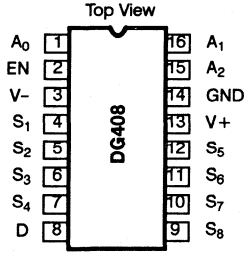
Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

Both DG408 and DG409 are available in dual-in-line ceramic and plastic packages with small outline for surface mount applications, and are specified for operation over the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

For additional information please see App Note AN89-1 and Technical Article TA89-2.

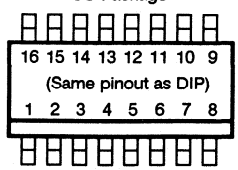
PIN CONFIGURATION

Dual-In-Line Package
Top View



Order Numbers:
CerDIP: DG408AK
DG408AK/883
Plastic: DG408DJ

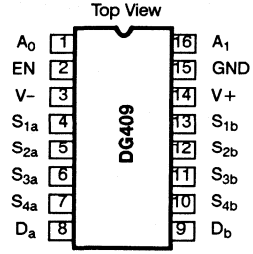
Narrow Body
SO Package



Top View

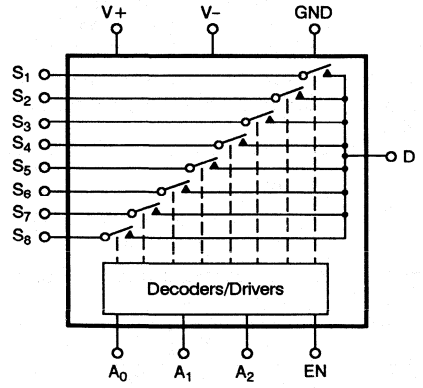
Order Number:
DG408DY
DG409DY

Dual-In-Line Package
Top View

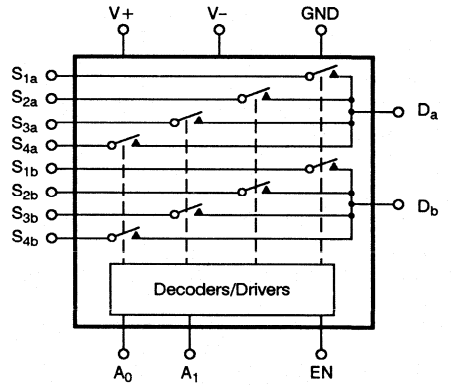


Order Numbers:
CerDIP: DG409AK
DG409AK/883
Plastic: DG409DJ

FUNCTIONAL BLOCK DIAGRAM



DG408
8-Channel Single Ended Multiplexer



DG409
Differential 4-Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs [h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Power Dissipation (Package)*
16-Pin Ceramic DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 450 mW
16-Pin Narrow Body SO**** ..... 600 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6 mW/°C above 75°C.
****Derate 7.6 mW/°C above 75°C.

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SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V		TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	V_D = ±10 V I_S = -10 mA		Room Full	40		100 125		100 125	Ω
$r_{DS(ON)}$ Matching Between Channels[f]		$\Delta r_{DS(ON)}$	V_D = 10 V, -10 V		Room			15		15	
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V V_D = ∓10 V	Room Full		-0.5 -50	0.5 50	-0.5 -50	0.5 50	nA
Drain OFF Leakage Current	DG408	$I_{D(OFF)}$		V_D = ±10 V V_S = ∓10 V	Room Full		-1 -100	1 100	-1 -100	1 100	
	DG409			V_D = ±10 V V_S = ∓10 V	Room Full		-1 -50	1 50	-1 -50	1 50	
Drain ON Leakage Current	DG408	$I_{D(ON)}$	V_S = V_D = ±10 V Sequence Each Swtich ON		Room Full		-1 -100	1 100	-1 -100	1 100	
	DG409				Room Full		-1 -50	1 50	-1 -50	1 50	

Siliconix incorporated

SPECIFICATIONS[a]

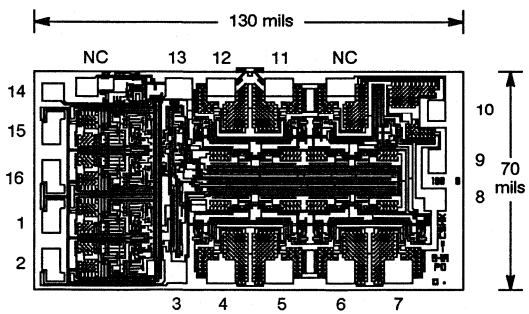
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V		TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DIGITAL CONTROL										
Logic Input Current Input Voltage High	I_{AH}	V_A = 2.4 V, 15 V		Full		-10	10	-10	10	µA
Logic Input Current Input Voltage Low	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		-10	10	-10	10	
DYNAMIC CHARACTERISTICS										
Transition Time	t_{TRANS}	See Figure 1		Full	160		250		250	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 3		Room		10		10		
Enable Turn-ON Time	$t_{ON(EN)}$	See Figure 2		Room Full	115		150 225		150	
Enable Turn-OFF Time	$t_{OFF(EN)}$			Full	105		150		150	
Charge Injection	Qi	C_L = 10 nF, V_S = 0 V		Room	20					pC
OFF Isolation[g]		V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz		Room	-75					dB
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					
Source OFF Capacitance	$C_{S(OFF)}$	V_{EN} = 0 V f = 1 MHz	V_S = 0 V	Room	11					pF
Drain OFF Capacitance DG408	$C_{D(OFF)}$		V_D = 0 V	Room	40					
Drain OFF Capacitance DG409				Room	20					
Drain ON Capacitance DG408	$C_{D(ON)}$			Room	54					
Drain ON Capacitance DG409				Room	34					
POWER SUPPLIES										
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0 V		Full			75		75	µA
Negative Supply Current	I-			Full		-75		-75		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full			0.5 2		0.5 2	mA
Negative Supply Current	I-			Full		-500		-500		µA

SPECIFICATIONS[a] (Single Supply)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Drain-Source ON Resistance[e]	$r_{DS(ON)}$	V_D = 3 V, 10 V I_S = - 1 mA	Room	90					Ω
DYNAMIC CHARACTERISTICS									
Switching Time of Multiplexer	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V V_{IN} = 2.4 V	Room	180					ns
Enable Turn ON Time	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V	Room	180					ns
Enable Turn OFF Time	$t_{ON(EN)}$	V_{S1} = 5 V	Room	120					ns
Charge Injection	Q	C_L = 10 nF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5					pC

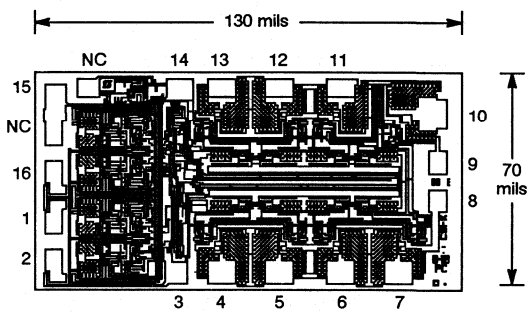
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = r_{DS(ON)}$ MAX - $r_{DS(ON)}$ MIN
g. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
h. Signals on S_X, D_X, on IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHIES



Pad No.	Function DG408	Pad No.	Function DG408
1	A_0	9	S_5
2	EN	10	S_6
3	V-	11	S_7
4	S_1	12	S_8
5	S_2	13	V+ (Substrate)
6	S_3	14	GND
7	S_4	15	A_1
8	D	16	A_2

CSHK-A **DG408**
9 Diodes
5 Resistors
8 p-Channel Enhancement MOSFET's
103 n-Channel Enhancement MOSFET's
2 NPN Bipolar Transistors



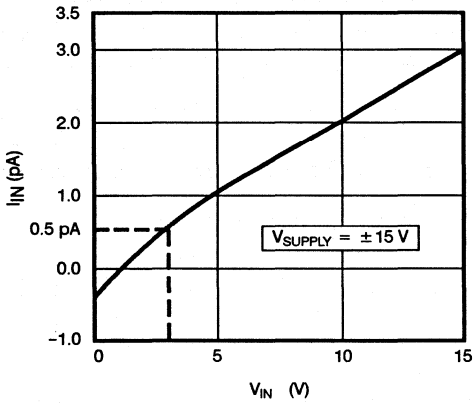
Pad No.	Function DG409	Pad No.	Function DG409
1	A_0	9	D_b
2	EN	10	S_{1b}
3	V-	11	S_{2b}
4	S_{1a}	12	S_{3b}
5	S_{2a}	13	S_{4b}
6	S_{3a}	14	V+ (Substrate)
7	S_{4a}	15	GND
8	D_a	16	A_1

CSHK-B **DG409**
9 Diodes
5 Resistors
8 p-Channel Enhancement MOSFET's
103 n-Channel Enhancement MOSFET's
2 NPN Bipolar Transistors

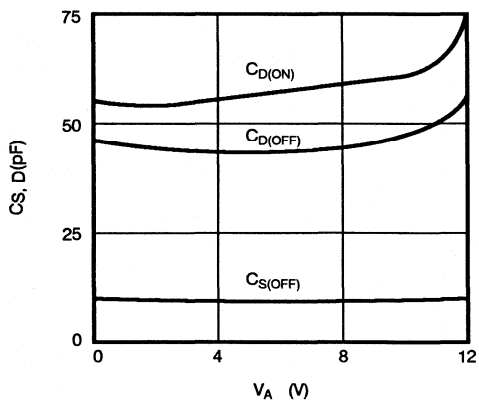
5

TYPICAL CHARACTERISTICS

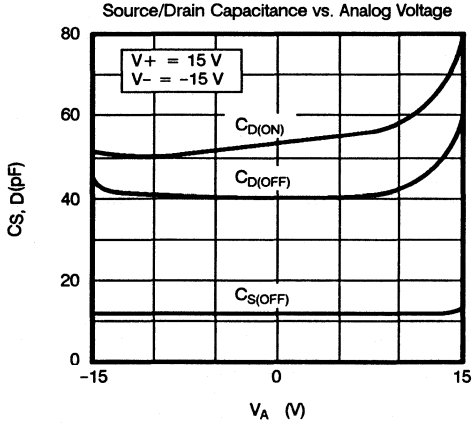
Input Logic Current vs. Logic Input Voltage



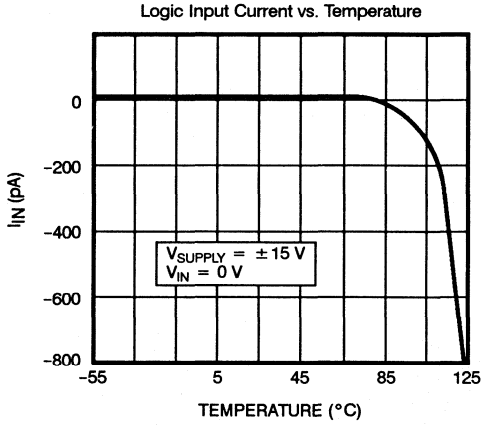
Source/Drain Capacitance vs. Analog Voltage (Single 12 V Supply)



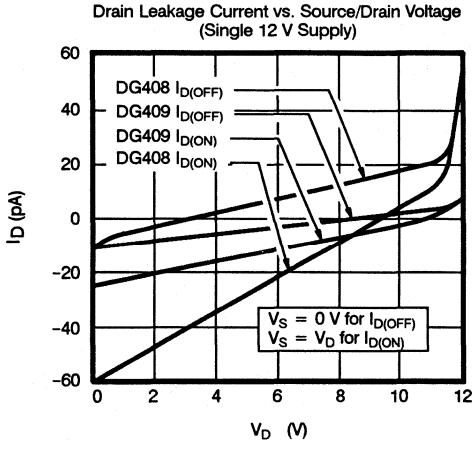
Source/Drain Capacitance vs. Analog Voltage



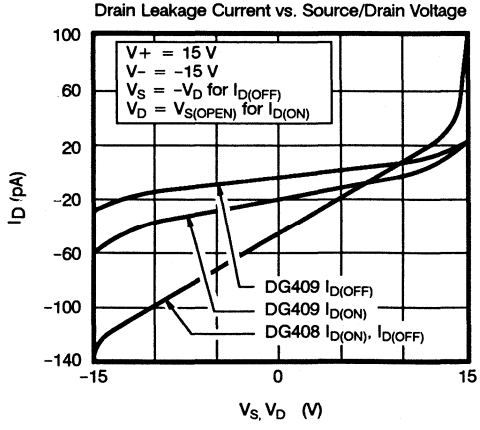
Logic Input Current vs. Temperature



Drain Leakage Current vs. Source/Drain Voltage (Single 12 V Supply)

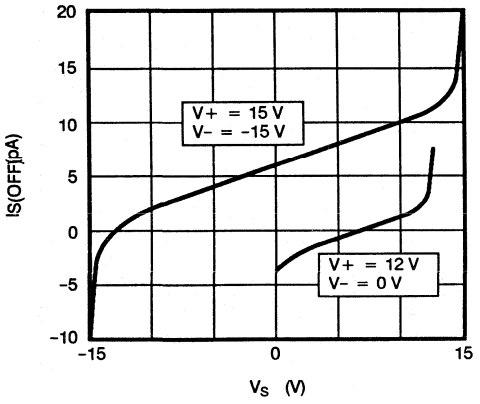


Drain Leakage Current vs. Source/Drain Voltage

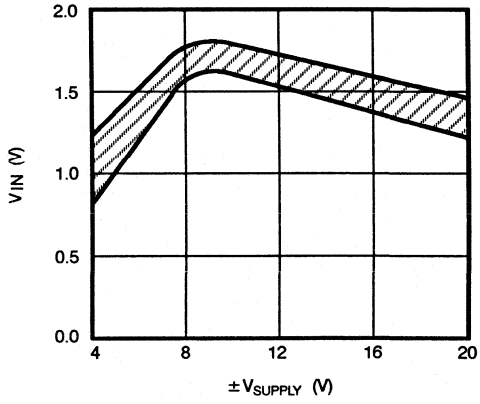


TYPICAL CHARACTERISTICS (Cont'd)

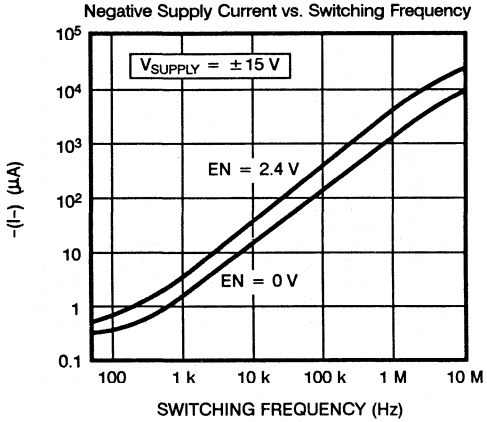
Source Leakage Current vs. Source Voltage



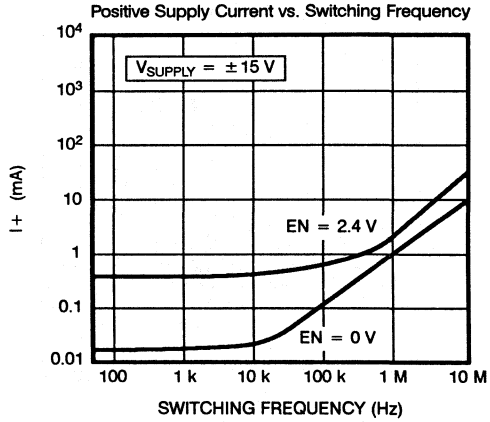
Input Switching Threshold vs. Supply Voltage



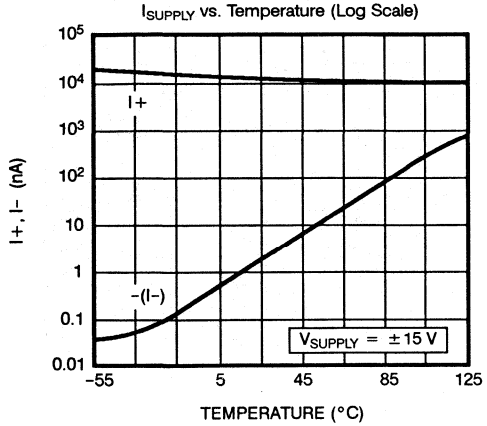
Negative Supply Current vs. Switching Frequency



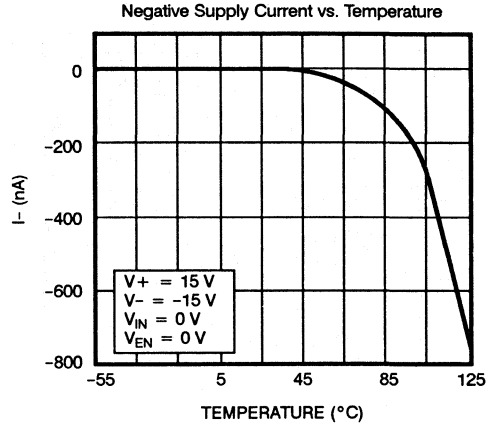
Positive Supply Current vs. Switching Frequency



ISUPPLY vs. Temperature (Log Scale)



Negative Supply Current vs. Temperature



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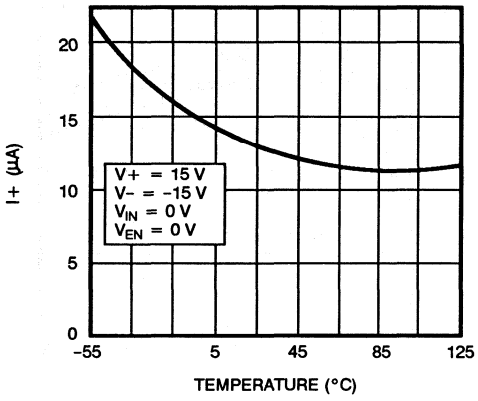
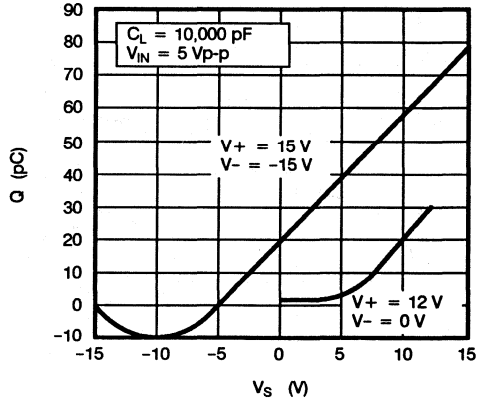
TYPICAL CHARACTERISTICS (Cont'd)

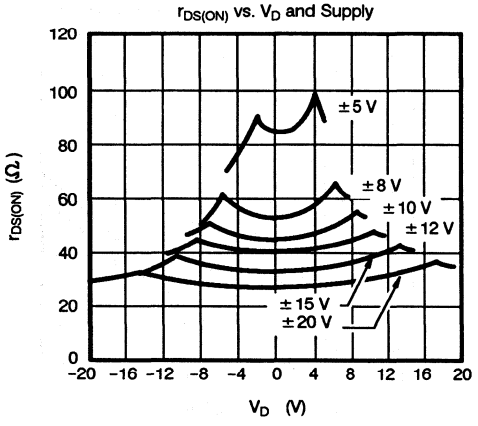
Positive Supply Current vs. Temperature
DG408



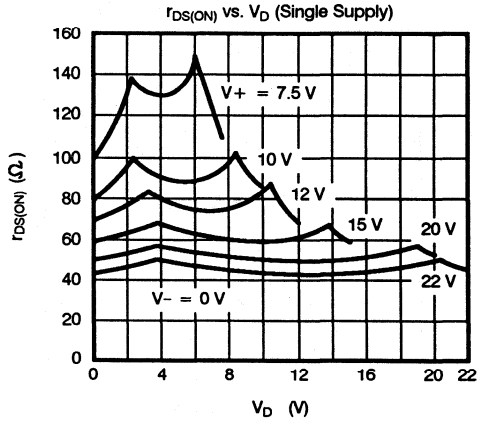
Charge Injection vs. Analog Voltage V_S
DG408/9



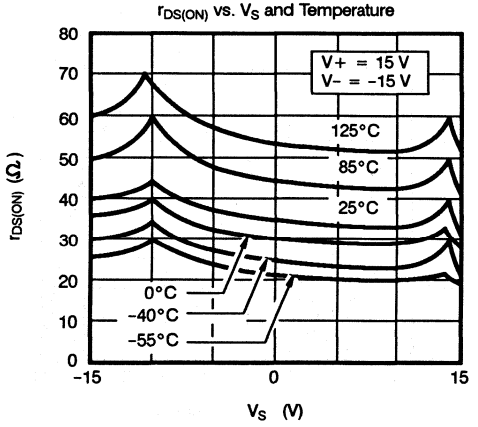
$r_{DS(ON)}$ vs. V_D and Supply



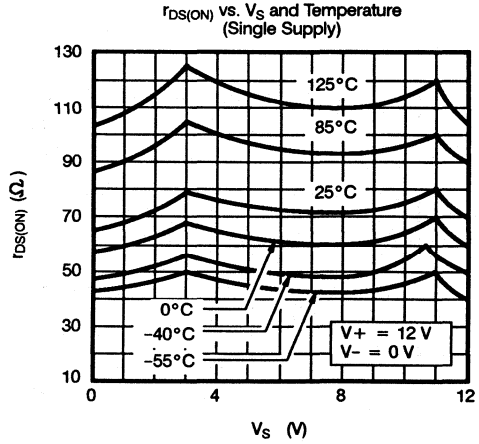
$r_{DS(ON)}$ vs. V_D (Single Supply)



$r_{DS(ON)}$ vs. V_S and Temperature

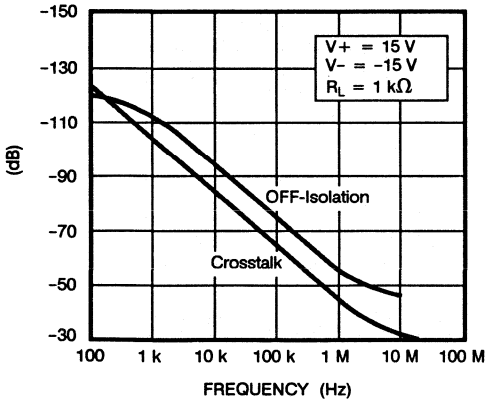


$r_{DS(ON)}$ vs. V_S and Temperature
(Single Supply)

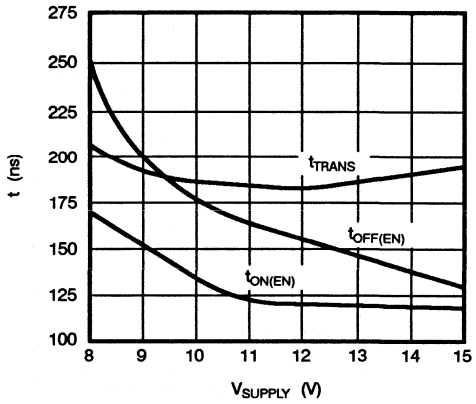


TYPICAL CHARACTERISTICS (Cont'd)

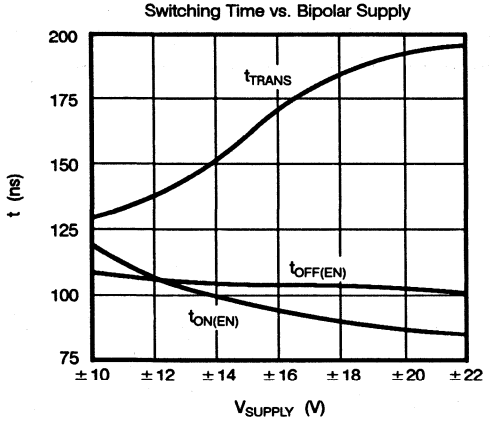
Off Isolation and Crosstalk vs. Frequency



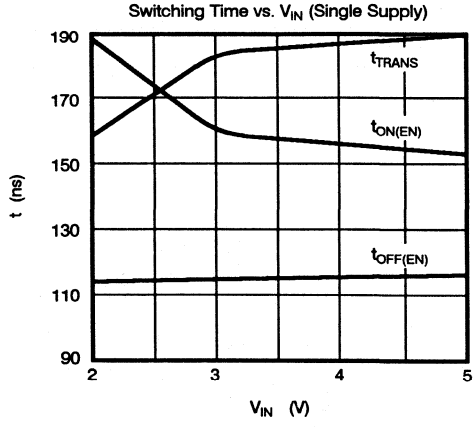
Switching Time vs. Single Supply



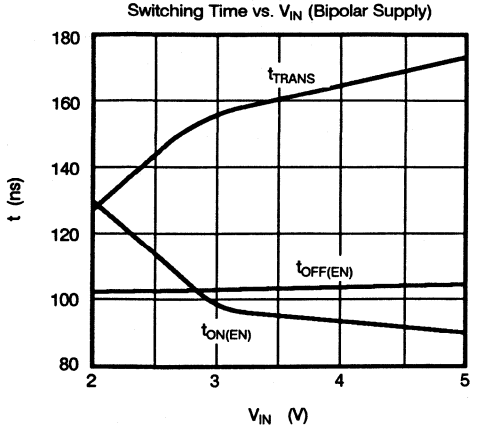
Switching Time vs. Bipolar Supply



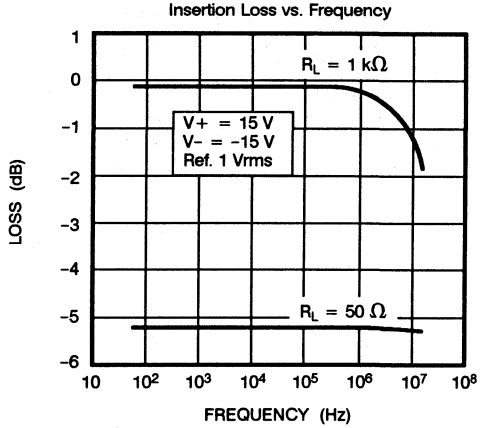
Switching Time vs. V_{IN} (Single Supply)



Switching Time vs. V_{IN} (Bipolar Supply)



Insertion Loss vs. Frequency



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TRUTH TABLES

DG408

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG409

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" $V_{AL} \leq 0.8$ V, Logic "1" $V_{AH} \geq 2.4$ V

TEST CIRCUITS

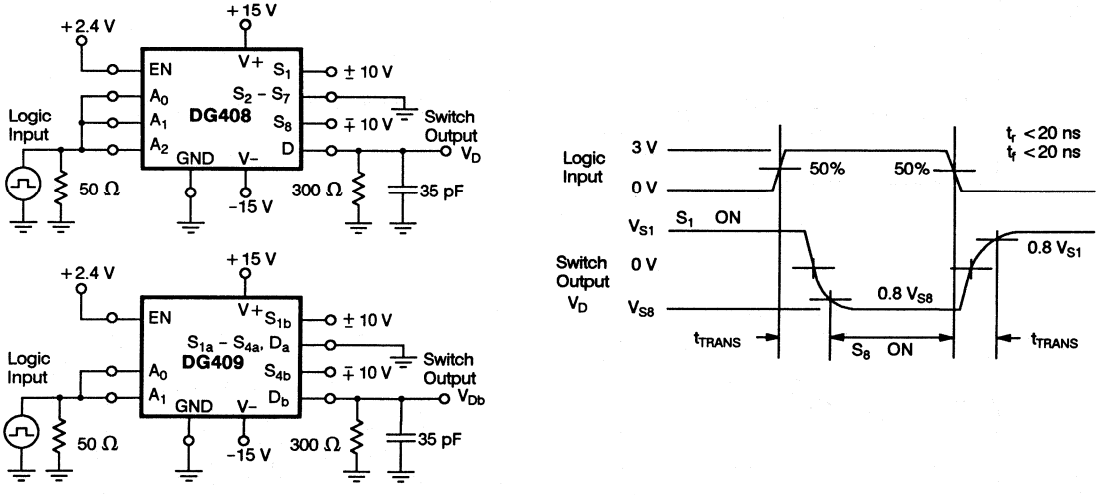


Figure 1. Transition Time

TEST CIRCUITS (Cont'd)

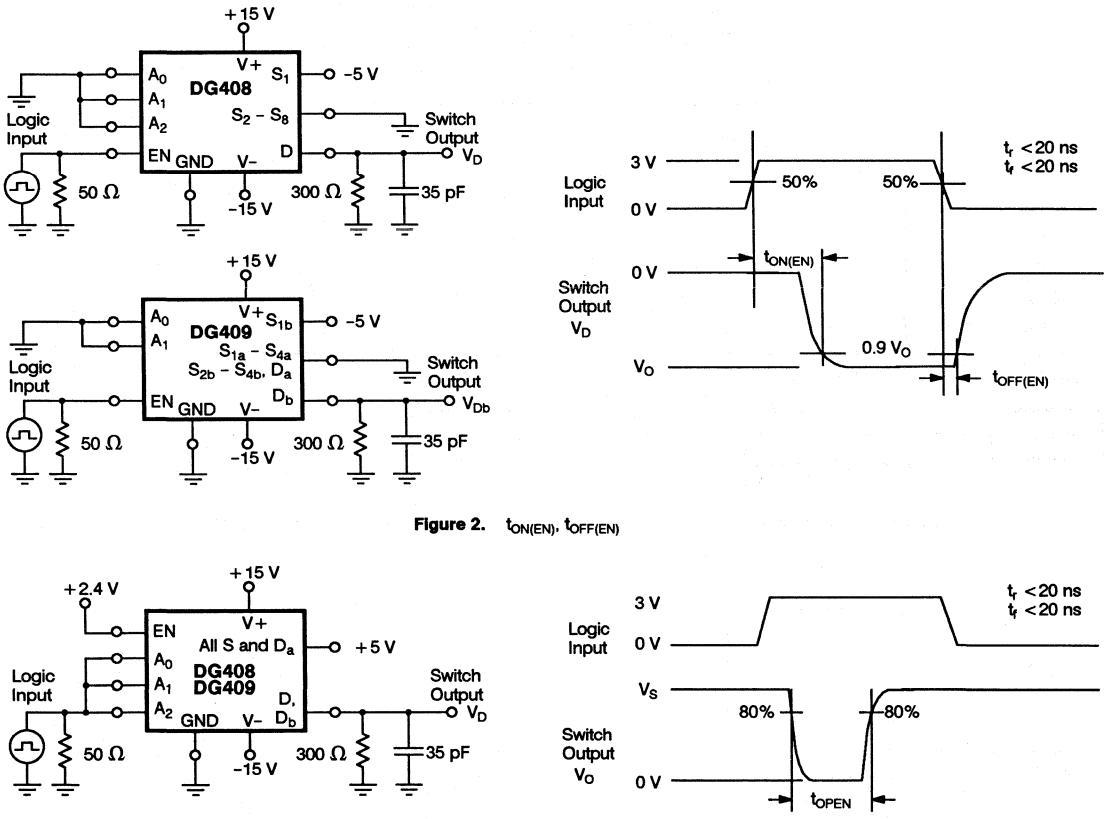


Figure 2. $t_{ON(EN)}$, $t_{OFF(EN)}$

Figure 3. Break-Before-Make Interval

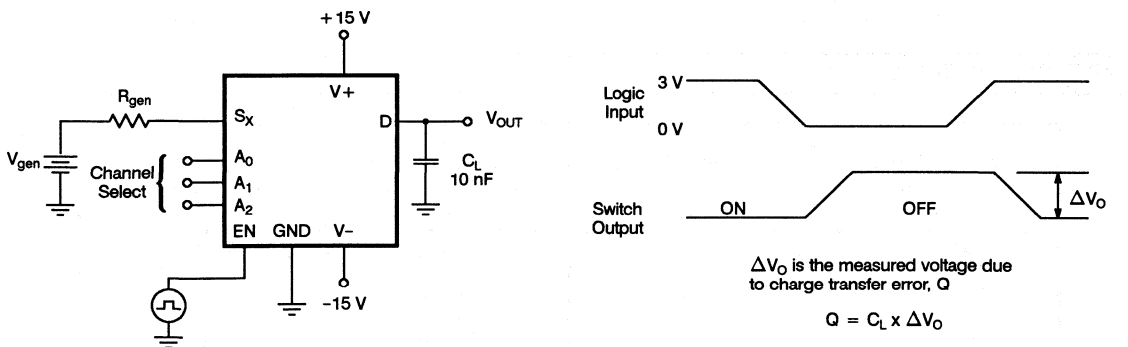


Figure 4. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

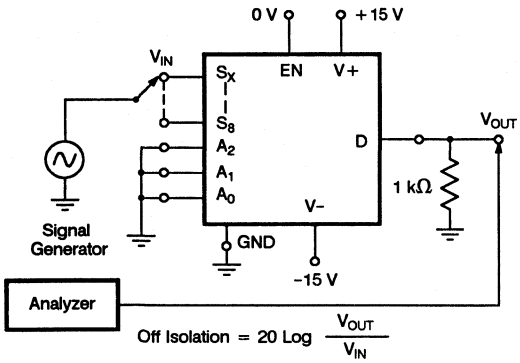


Figure 5. Off Isolation

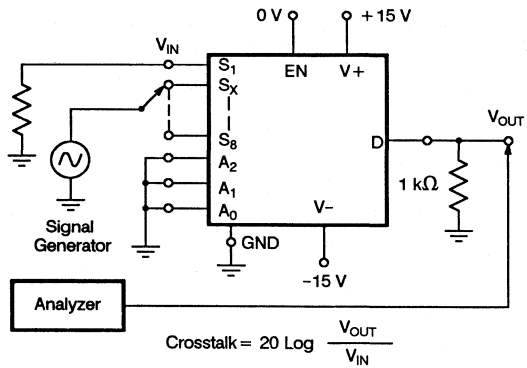


Figure 6. Crosstalk

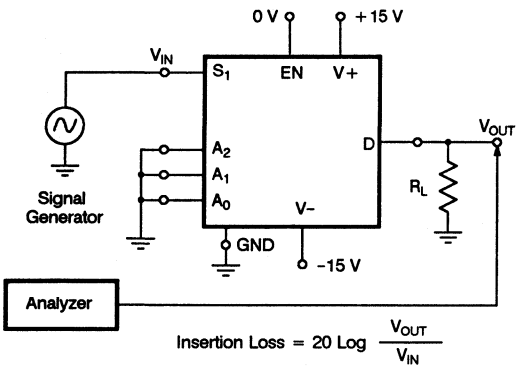


Figure 7. Insertion Loss

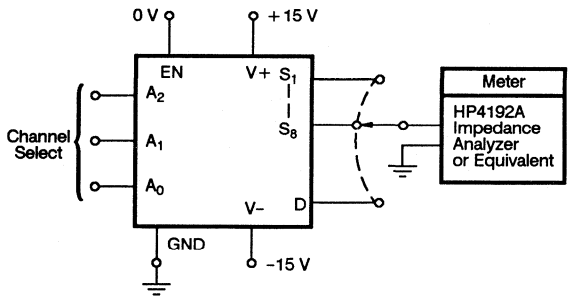


Figure 8. Source/Drain Capacitances

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	V_{IN} Logic Input Voltage V_{INH} Min/V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
12	0	2.4/0.8	0 to 12
8	-8	2.4/0.4	-8 to 8
5	-5	2.0/0.4	-5 to 5

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

** Electrical Characteristics chart based on V+ = 15 V, V- = -15 V.

APPLICATION HINTS (Cont'd)*

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see figure). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

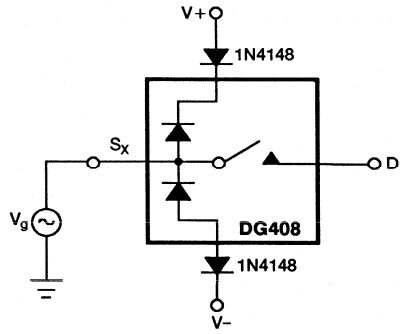
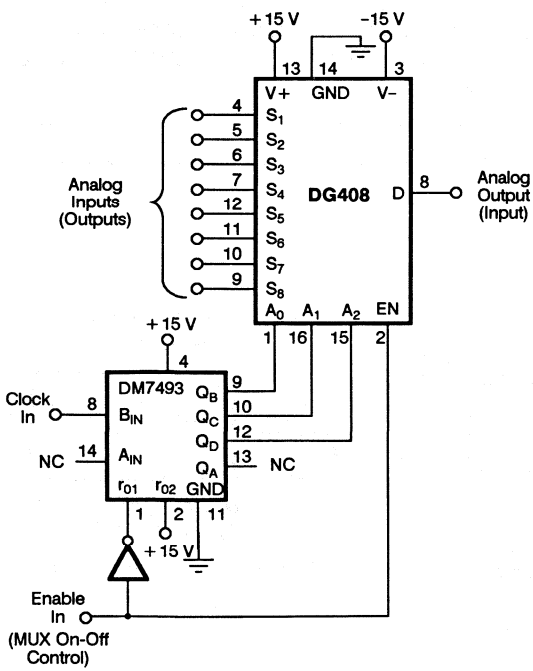


Figure 9. Overvoltage Protection Using Blocking Diodes

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

APPLICATIONS

8-Channel Sequential Mux/Demux



Differential 4-Channel Sequential Mux/Demux

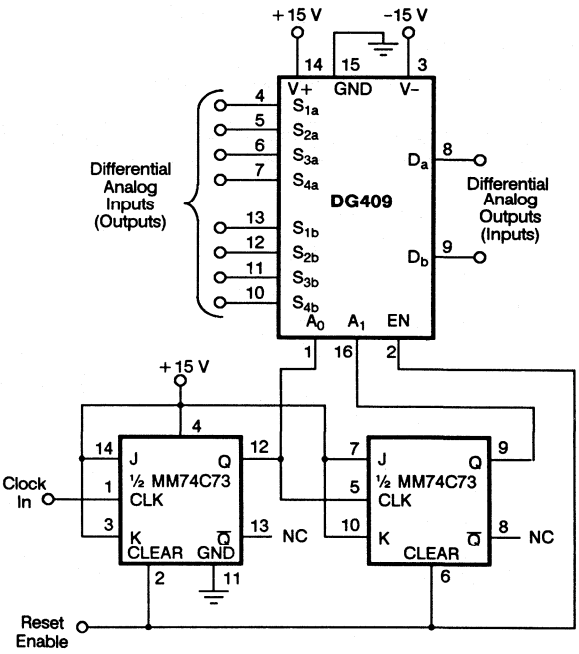


Figure 10.

DG411/412/413
Precision Monolithic Quad SPST CMOS Analog Switches

Siliconix incorporated

FEATURES

- ±15 Volt Input Range
- ON-Resistance <35 Ω
- Fast Switching Action
  t_{ON} <175 ns
- Ultra Low Power (P_D <35 μW)
- TTL, CMOS Compatible
- ESD Protection > ±4000 V
- Single Supply Capability

BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Operated Systems

DESCRIPTION

The DG411 series of monolithic quad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (< 35 μW) with high speed (t_{ON} < 175 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

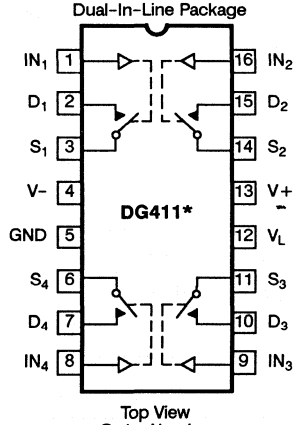
To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to the supplies when OFF. ON-resistance is very flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range limitation.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams. Package options include the 16-pin CerDIP, plastic and small outline (SO) packages. Performance grades include both the industrial, D suffix (-40 to 85°C), and the military, A suffix (-55 to 125°C) temperature ranges.

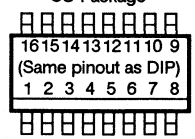
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line Package



Top View
Order Numbers:
CerDIP: DG411AK, DG411AK/883
DG412AK, DG412AK/883
Plastic: DG411DJ, DG412DJ

Narrow Body
SO Package



Top View

Order Numbers:
DG411DY, DG412DY

Four SPST Switches per Package
Truth Table

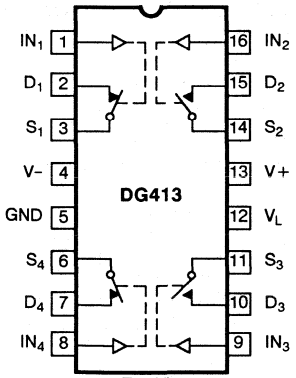
	Switch	
Logic	DG411	DG412
0	ON	ON
1	OFF	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches shown for logic "1" input.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION (Cont'd)

Dual-In-Line Package



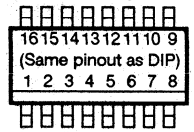
Top View

Order Numbers:

CerDIP: DG413AK
DG413AK/883

Plastic: DG413DJ

SO Package



Top View

Order Number:
DG413DY

DG413

Four SPST Switches per Package

Truth Table*

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

* Switches shown for logic "1" input.

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
GND to V- ..... 25 V
V_L ..... (GND -0.3 V) (V+) +0.3 V
Digital Inputs, V_S, V_D[1] ..... (V-) -2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% Duty Cycle) ..... 100 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 470 mW
16-Pin CerDIP*** ..... 900 mW
16-Pin SO**** ..... 600 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 25°C.
***Derate 12 mW/°C above 75°C.
****Derate 7.6 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

5

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]	V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V I_S = -10 mA, V_D = ±8.5 V		Room Full	25		35 45	35 45		Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V V- = -16.5 V	V_D = -15.5 V V_S = 15.5 V	Room Full	-0.1	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
	$I_{D(OFF)}$		V_D = 15.5 V V_S = -15.5 V	Room Full	-0.1	-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Channel On Leakage Current	$I_{D+S(ON)}$		V_D = 15.5 V V_S = -15.5 V	Room Full	-0.1	-0.4 -40	0.4 40	-0.4 -40	0.4 40	

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
DIGITAL CONTROL									
Input Current, V_{IN} LOW	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.005	-0.5	0.5	-0.5	0.5	µA
Input Current, V_{IN} HIGH	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.005	-0.5	0.5	-0.5	0.5	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, V_S = ±10 V	Room	110		175		175	ns
			Hot			220		220	
Turn-OFF Time	t_{OFF}	See Switching Time Test Circuit	Room	100		145		145	
			Hot			160		160	
Break-Before-Make Time Delay	t_D	DG413 Only R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
OFF Isolation[c]		R_L = 50 Ω, C_L = 5 pF	Room	68					dB
Ch-to-Ch Crosstalk[c]		f = 1 MHz	Room	85					
Source OFF Capacitance[c]	$C_{S(OFF)}$	f = 1 MHz	Room	9					pF
Drain OFF Capacitance[c]	$C_{D(OFF)}$		Room	9					
Channel ON Capacitance[c]	$C_{D(ON)}$ + $C_{S(ON)}$		Room	35					

SPECIFICATIONS (UNIPOLAR SUPPLIES)[a]

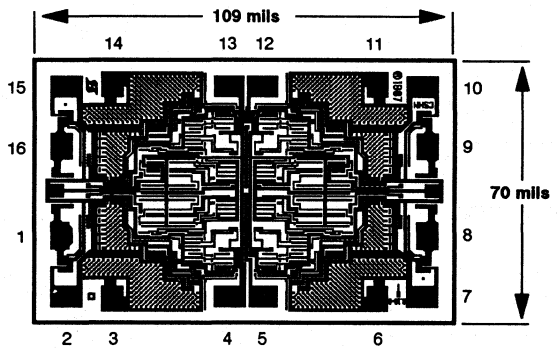
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source ON Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = 3.8 V V+ = 10.8 V	Room	40		80		80	Ω
			Full			100		100	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ±8 V	Room	175		250		250	ns
			Hot			315		315	
Turn-OFF Time	t_{OFF}	See Switching Time Test Circuit	Room	95		125		125	
			Hot			140		140	
Break-Before-Make Time Delay	t_D	DG413 Only R_L = 300 Ω, C_L = 35 pF	Room	25					
Charge Injection	Q	V_g = 6.0 V, R_g = 0 Ω, C_L = 10 nF	Room	25					pC

SPECIFICATIONS (UNIPOLAR SUPPLIES)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V	Room Hot	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Hot	-0.0001	-1 -5		-1 -5		
Logic Supply Current	I_L		Room Hot	-0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Hot	-0.0001	-1 -5		-1 -5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



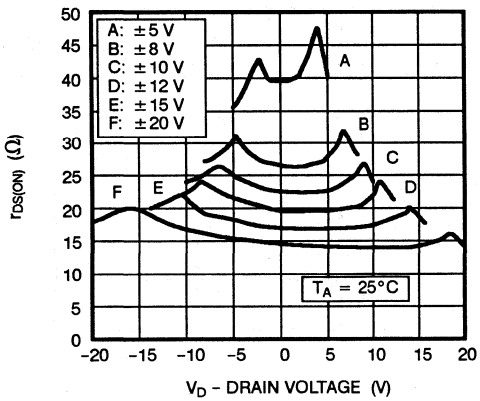
Pad No.	Function
1	IN_1
2	D_1
3	S_1
4	V-
5	GND
6	S_4
7	D_4
8	IN_4
9	IN_3
10	D_3
11	S_3
12	V_L
13	V+ (Substrate)
14	S_2
15	D_2
16	IN_2

CSHN-A, B, C

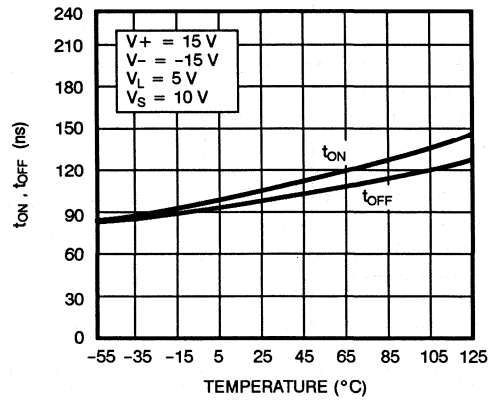
8 Capacitors
5 Resistors
36 p-Channel Enhancement MOSFETs
44 n-Channel Enhancement MOSFETs
8 Diodes

TYPICAL CHARACTERISTICS

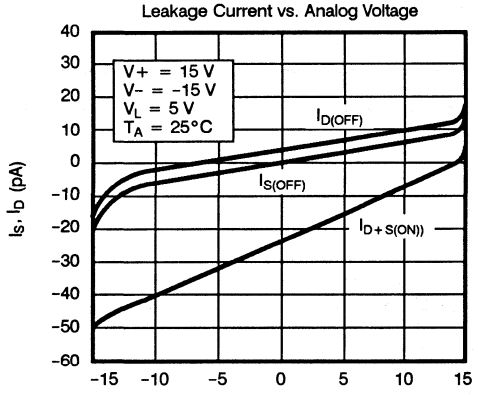
ON-resistance vs. V_D and Power Supply Voltage



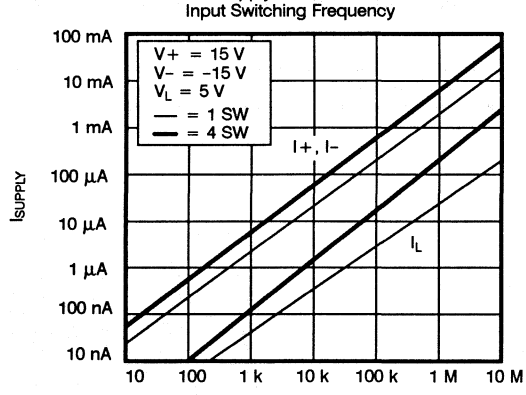
Switching Time vs. Temperature



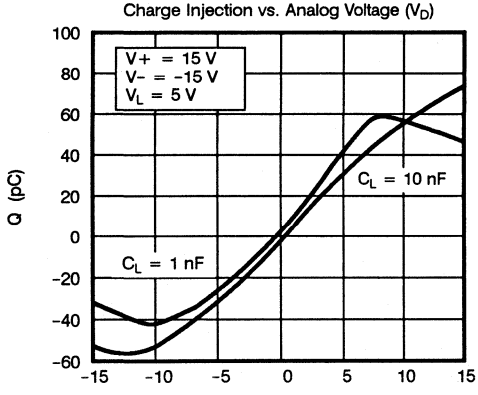
Leakage Current vs. Analog Voltage



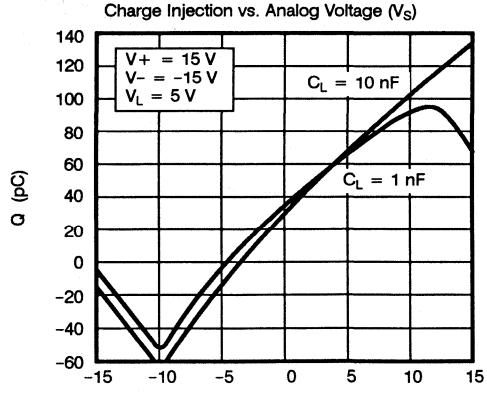
Supply Current vs. Input Switching Frequency



Charge Injection vs. Analog Voltage (V_D)

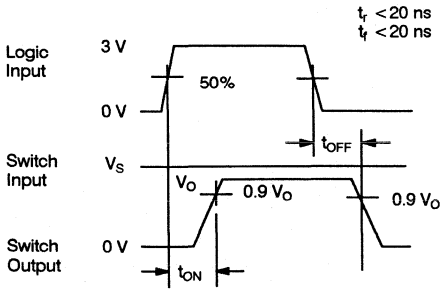


Charge Injection vs. Analog Voltage (V_S)

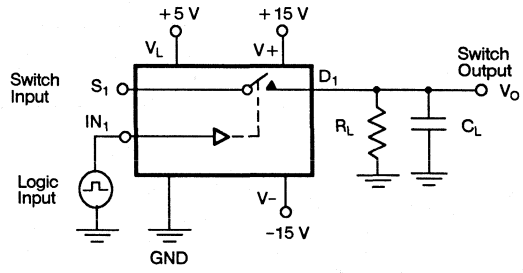


TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.



Repeat test for all IN and S.

For load conditions, See Specifications
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Time

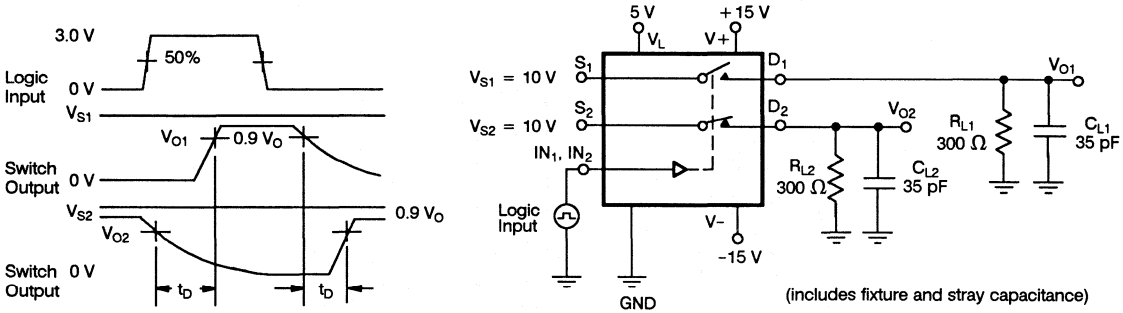
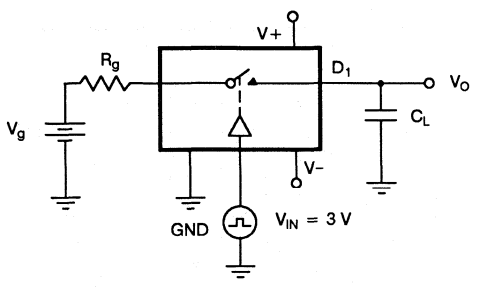
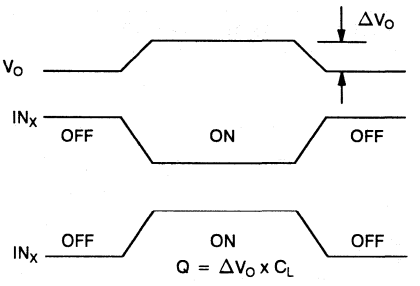


Figure 2. Break-Before-Make





IN_X dependent on switch configuration Input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

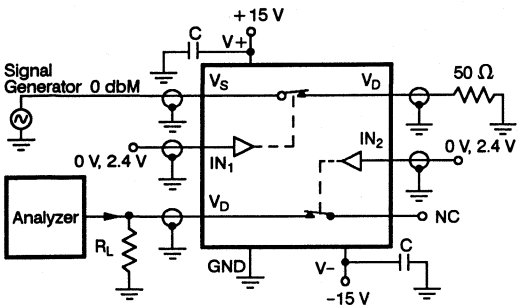


Figure 4. Crosstalk

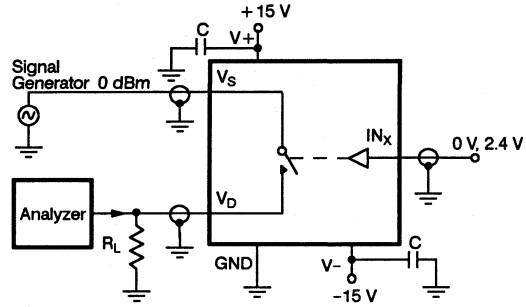


Figure 5. Off Isolation

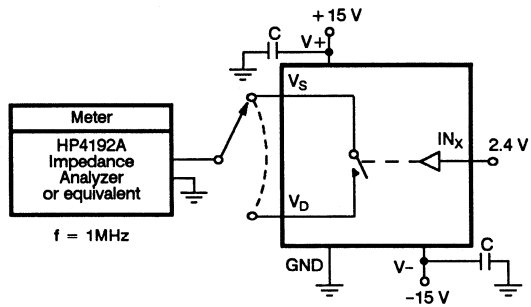


Figure 6. Source/Drain Capacitances

SCHEMATIC DIAGRAM (Typical Channel)

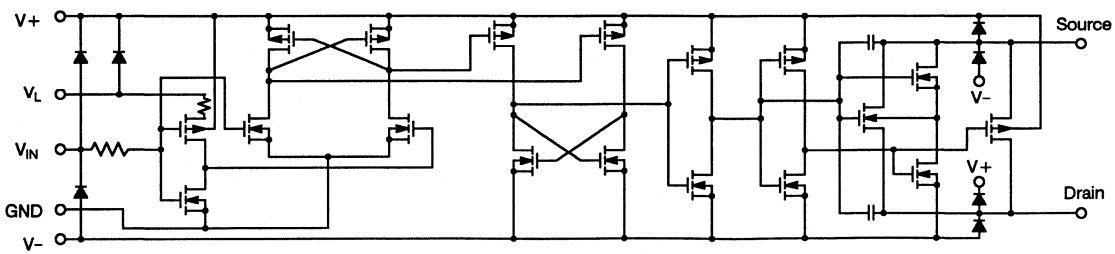
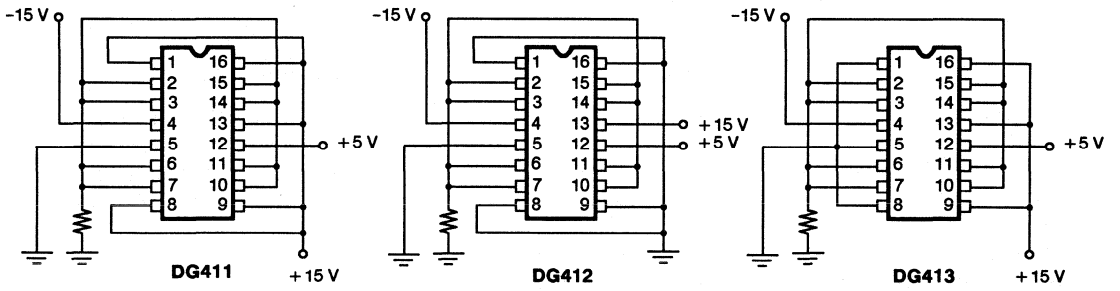


Figure 7.

BURN-IN CIRCUITS



Note: All resistors are 10 kΩ unless otherwise specified.

Figure 8.

APPLICATIONS

Single Supply Operation:

The DG411/412/413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. To function properly 12 volts are tied to Pin 13 and 0 volts are tied to Pin 4. Note: Pin 12 still requires 5 volts for TTL compatible switching.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 9, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

5

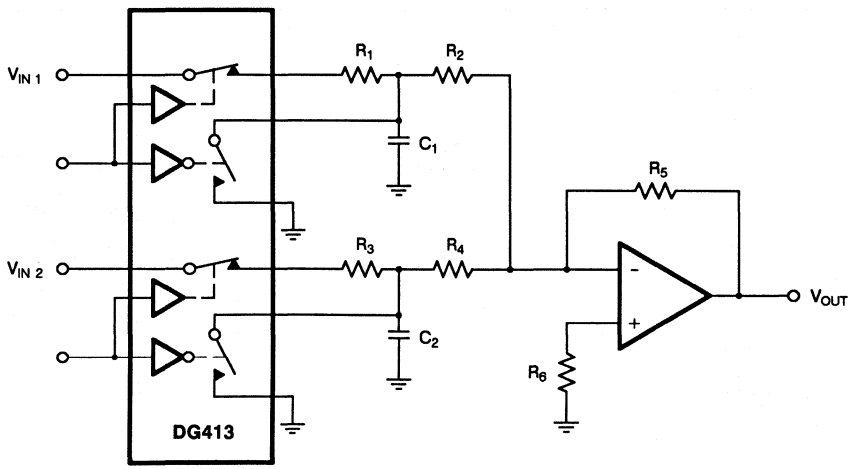


Figure 9. Summing Amplifier

DG417/418/419
Precision MiniDIP CMOS Analog Switches

Siliconix incorporated

FEATURES

- ± 15 Volt Input Range
- ON-Resistance < 35 Ω
- Fast Switching Action t_{ON} < 175 ns
- Ultra Low Power Requirements ($P_D \leq 35$ µW)
- TTL and CMOS Compatible
- MiniDIP and SO Packaging
- ESDS Protection > ± 4000 V

BENEFITS

- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

APPLICATIONS

- Precision Test Equipment
- Precision Instrumentation
- Battery Operated Systems
- Sample and Hold Circuits

DESCRIPTION

The DG417, DG418 and DG419 monolithic CMOS analog switches were designed to provide high performance switching of analog signals. Combining low power, low leakages, high speed, low ON-resistance and small physical size, the DG417 series is ideally suited for portable and battery powered industrial and military applications requiring high performance and efficient use of board space.

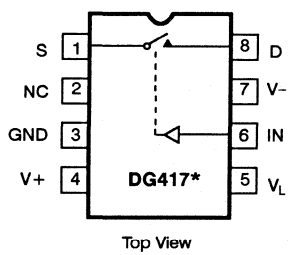
To achieve high voltage ratings and superior switching performance, the DG417 series is built on Siliconix's high voltage silicon gate (HVSG) process. Break-before-make is guaranteed for the DG419, which is an SPDT configuration. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is very flat over the full ± 15 V analog range, rivaling JFET performance without the inherent dynamic range and supply voltage limitations.

The three devices are differentiated by their switch action as shown in the functional block diagrams. Package options include the 8-pin plastic and ceramic DIP, and the small outline. Performance grades include both the industrial, D suffix (-40 to 85°C) and the military, A suffix (-55 to 125°C) temperature ranges.

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE

Dual-In-Line Package

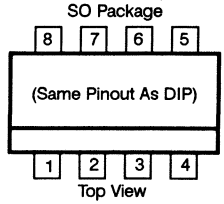


Top View

Order Numbers:

CerDIP: DG417AK, DG417AK/883
DG418AK, DG418AK/883
Plastic: DG417DJ
DG418DJ

Narrow Body
SO Package



Top View

Order Number:
DG417DY
DG418DY

One SPST Switch per Package
Truth Table*

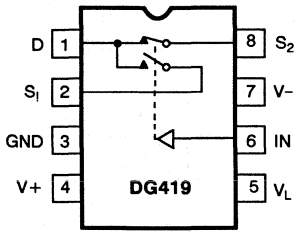
Logic	Switch	
	DG417	DG418
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switch Shown for Logic "1" Input

PIN CONFIGURATION, FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE (Cont'd)

Dual-In-Line Package



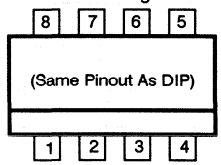
Top View

Order Numbers:

CerDIP: DG419AK, DG419AK/883

Plastic: DG419DJ

SO Package



Top View

Order Number:
DG419DY

One SPDT Switch per Package

Truth Table*

Logic	Switch 1	Switch 2
0	ON	OFF
1	OFF	ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

* Switches Shown for Logic "1" Input

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V
GND ..... 25 V
V_L ..... (GND -0.3 V) to (V+) + 0.3 V
Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+) + 2 V
or 30 mA, whichever occurs first
Current, (Any Terminal) Continuous ..... 30 mA
Current (S or D) Pulsed 1 ms, 10% duty cycle ..... 100 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
8-Pin Plastic DIP** ..... 400 mW
8-Pin CerDIP*** ..... 600 mW
8-Pin SO**** ..... 400 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C.
***Derate 12 mW/°C above 75°C.
****Derate 6.5 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

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SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[c]		V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	I_S = -200 mA, V_D = ±12.5 V	Room	20		35		35	Ω
			V+ = 13.5 V, V- = -13.5 V	Full			45		45	
Switch OFF Leakage Current		$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = -15.5 V, V_S = 15.5 V	Room	-0.1	-0.25	0.25	-0.25	0.25	nA
				Full		-20	20	-20	20	
	DG417 DG418	$I_{D(OFF)}$	V+ = 16.5 V, V- = -16.5 V, V_D = 15.5 V, V_S = -15.5 V	Room	-0.1	-0.25	0.25	-0.25	0.25	
				Full		-20	20	-20	20	
	DG419			Room	-0.1	-0.75	0.75	-0.75	0.75	
				Full		-60	60	-60	60	
Channel ON Leakage Current	DG417 DG418	$I_{D(ON)}$	V+ = 16.5 V, V- = -16.5 V, V_S = V_D = ±15.5 V	Room	-0.4	-0.4	0.4	-0.4	0.4	
				Full		-40	40	-40	40	
	DG419			Room	-0.4	-0.75	0.75	-0.75	0.75	
				Full		-60	60	-60	60	

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DIGITAL CONTROL										
Input Current, V_{IN} Low		I_{IL}	V_{IN} = 0.8 V	Full	0.005	-0.5	0.5	-0.5	0.5	µA
Input Current, V_{IN} High		I_{IH}	V_{IN} = 2.4 V	Full	0.005	-0.5	0.5	-0.5	0.5	
DYNAMIC CHARACTERISTICS										
Turn-ON Time		t_{ON}	DG417, DG418 ONLY R_L = 300 Ω, C_L = 35 pF V_S = ±10 V See Switching Time Test Circuit	Room Full	100		175 250		175 250	ns
Turn-OFF Time		t_{OFF}		Room Full	60		145 210		145 210	
Transition Time		t_{TRANS}	DG419 ONLY R_L = 300 Ω, C_L = 35 pF V_{S1} = ±10 V, V_{S2} = ∓10 V	Room Full			175 250		175 250	
Break-Before-Make Time Delay		t_D	DG419 ONLY R_L = 300 Ω, C_L = 35 pF V_{S1} = V_{S2} = ±10 V	Room	13	5		5		
Charge Injection		Q	C_L = 10 nF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
Source OFF Capacitance[d]		$C_{S(OFF)}$	f = 1 MHz, V_S = 0 V	Room	8					pF
Drain OFF Capacitance[d]	DG417 DG418	$C_{D(OFF)}$		Room	8					
Channel ON Capacitance[d]	DG417 DG418	$C_{D + S(ON)}$		Room	30					
	DG419			Room	35					
POWER SUPPLIES										
Positive Supply Current		I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0.0 or 5.0 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current		I-		Room Full	-0.0001	-1 -5		-1 -5		
Logic Supply Current		I_L		Room Full	0.0001		1 5		1 5	
Ground Current		I_{GND}		Room Full	-0.0001	-1 -5		-1 -5		

SPECIFICATIONS (UNIPOLAR SUPPLIES)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V, V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source ON-Resistance[e]	$r_{DS(ON)}$	I_S = -10 mA, V_D = 3.8 V, V+ = 10.8 V	Room	40					Ω
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF	Room	110					ns
Turn-OFF Time	t_{OFF}	V_S = 8 V, See Switching Time Test Circuit	Room	40					ns
Break-Before-Make Time Delay	t_D	DG419 ONLY, R_L = 300 Ω, C_L = 35 pF	Room	60					ns
Charge Injection	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room	5					pC
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 13.2 V	Room	0.0001					µA
Negative Supply Current	I-	V_L = 5.25 V	Room	-0.0001					µA
Logic Supply Current	I_L	V_{IN} = 0 or 5 V	Room	0.0001					µA
Ground Current	I_{GND}		Room	-0.0001					µA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

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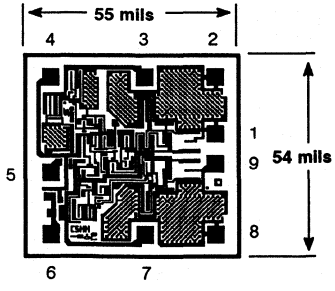
DIE TOPOGRAPHY



DG417 Pad No.	DG417 Function	DG418 Pad No.	DG418 Function	DG419 Pad No.	DG419 Function
1	D	1	NC	1	D_A
2	S	2	NC	2	S_1
3	GND	3	GND	3	GND
4	V+ (substrate)	4	V+ (substrate)	4	V+ (substrate)
5	V_L	5	V_L	5	V_L
6	IN	6	IN	6	IN
7	V-	7	V-	7	V-
8	NC	8	S	8	S_2
9	NC	9	D	9	D_B

CSHH-A (DG417, DG418)

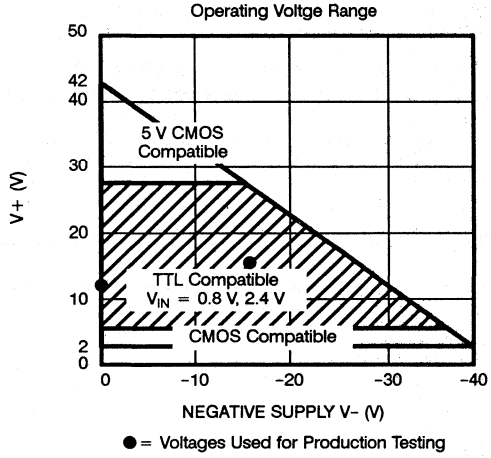
8 p-Channel MOSFETs
10 n-Channel MOSFETs
2 Diodes
1 Resistor
2 Capacitors

CSHH-A (DG419)

11 p-Channel MOSFETs
15 n-Channel MOSFETs
2 Diodes
1 Resistor
4 Capacitors

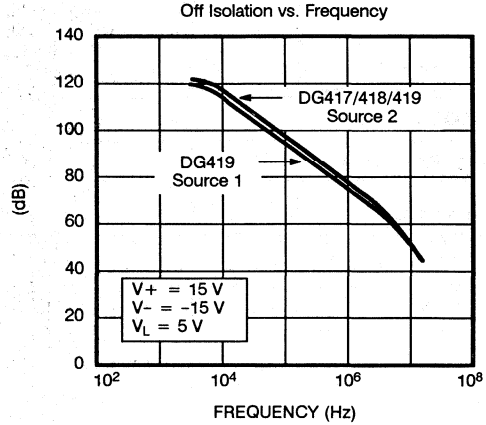
TYPICAL CHARACTERISTICS

Operating Voltge Range

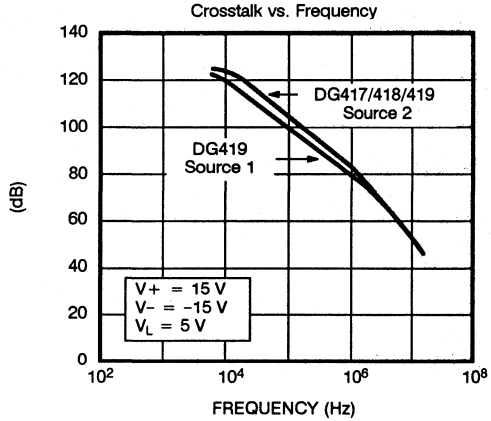


● = Voltages Used for Production Testing

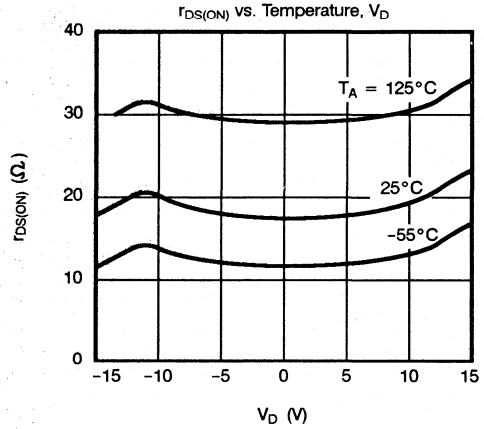
Off Isolation vs. Frequency



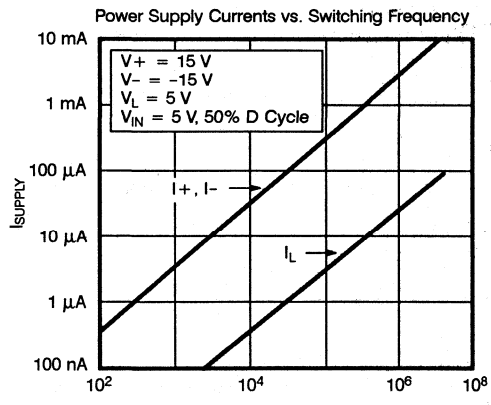
Crosstalk vs. Frequency



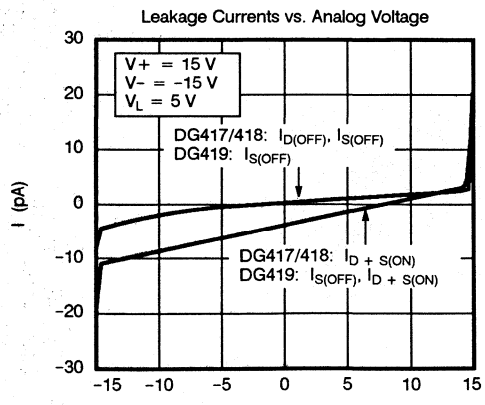
$r_{DS(ON)}$ vs. Temperature, V_D



Power Supply Currents vs. Switching Frequency

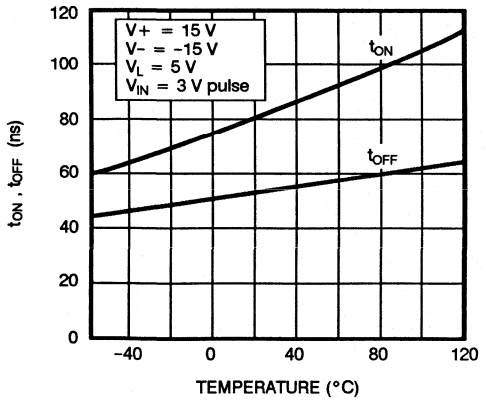


Leakage Currents vs. Analog Voltage

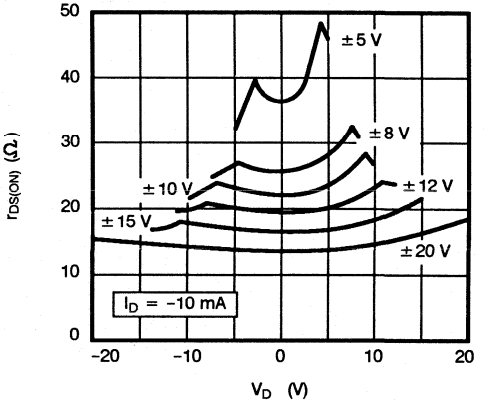


TYPICAL CHARACTERISTICS (Cont'd)

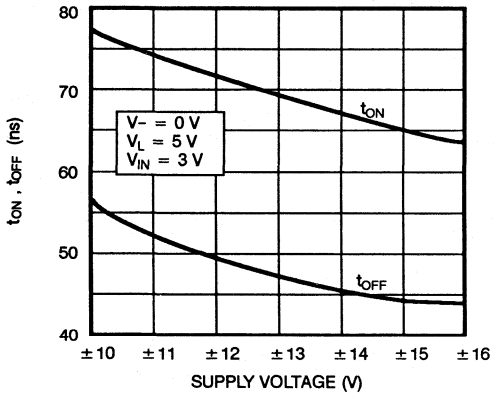
Switching Time vs. Temperature



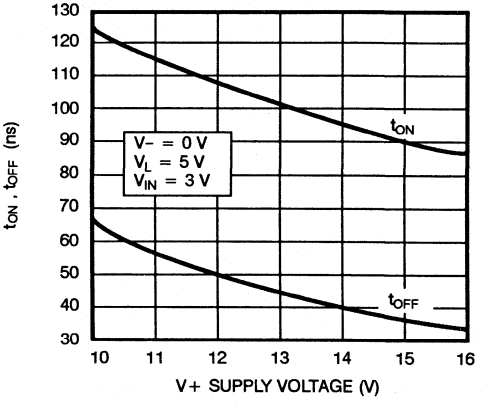
$r_{DS(ON)}$ vs. V_D and Supply Voltage



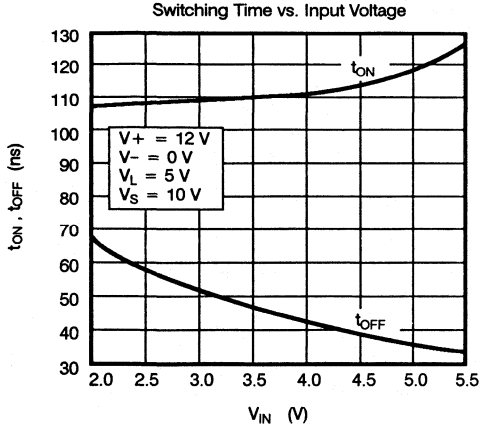
Switching Time vs. Supply Voltages



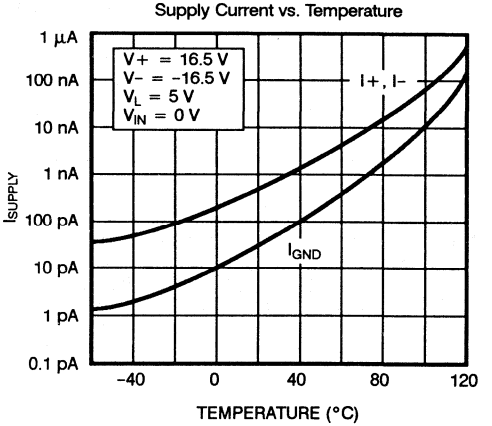
Switching Time vs. V+



Switching Time vs. Input Voltage



Supply Current vs. Temperature



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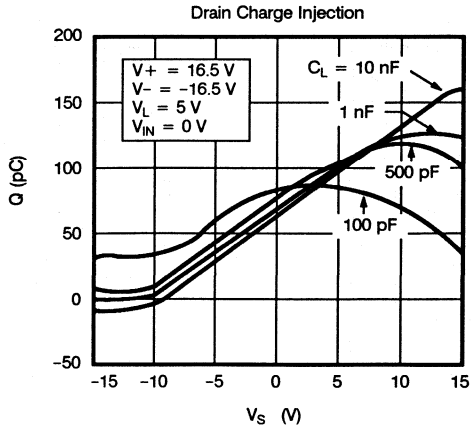
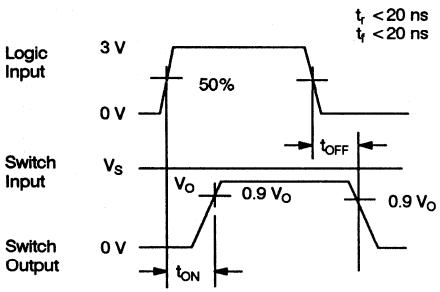
TYPICAL CHARACTERISTICS (Cont'd)

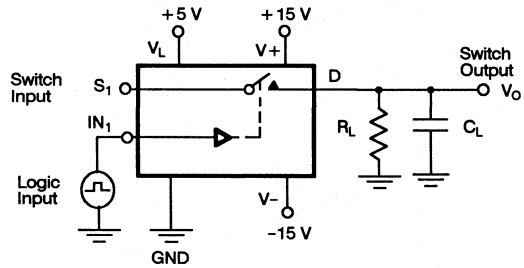


TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



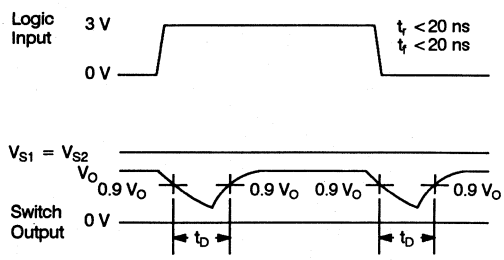
NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

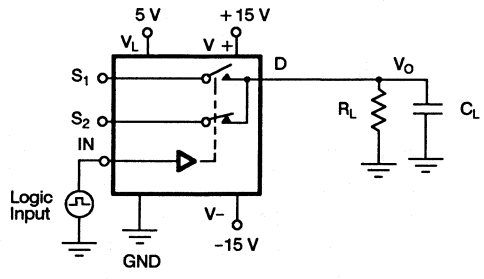


For load conditions, See Specifications
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Times (DG417 and DG481 Only)





For load conditions, See Specifications
C_L (includes fixture and stray capacitance)

Figure 2. Break- Before-Make (DG419 Only)

TEST CIRCUITS (Cont'd)

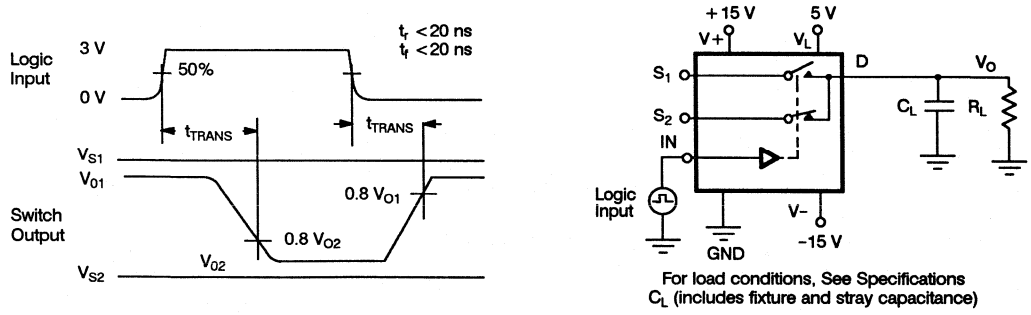


Figure 3. Transition Time (DG419 Only)

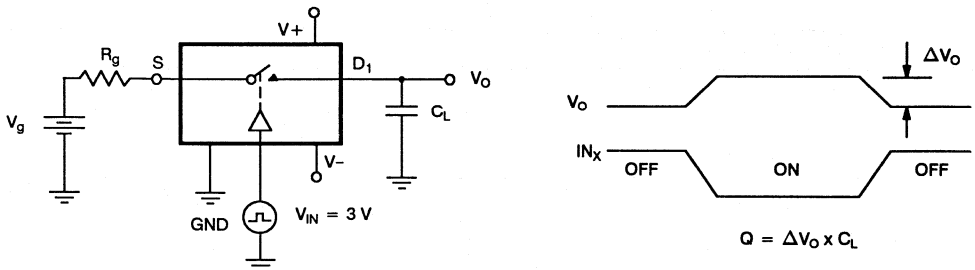
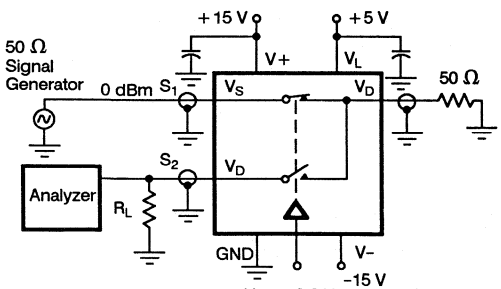


Figure 4. Charge Injection



Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

Figure 5. Crosstalk (DG419 Only)

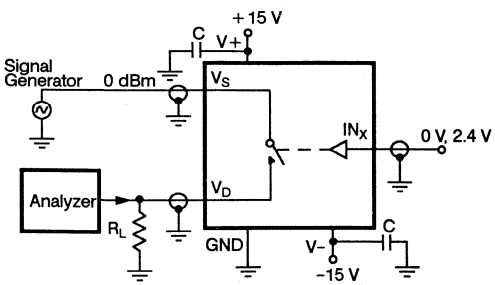


Figure 6. Off Isolation

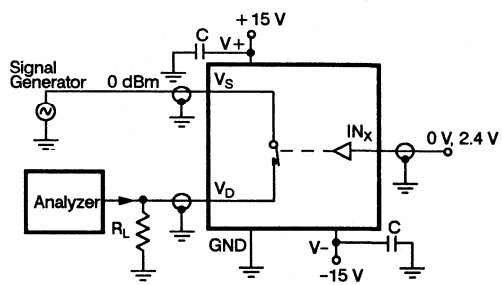


Figure 7. Insertion Loss

TEST CIRCUITS (Cont'd)

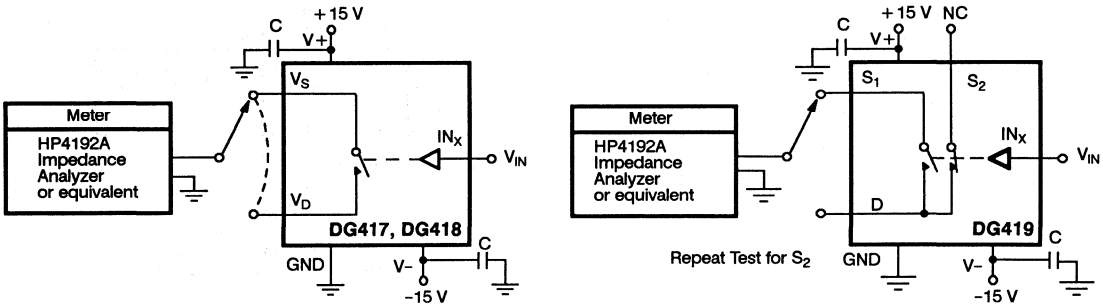


Figure 8. Source/Drain Capacitances

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

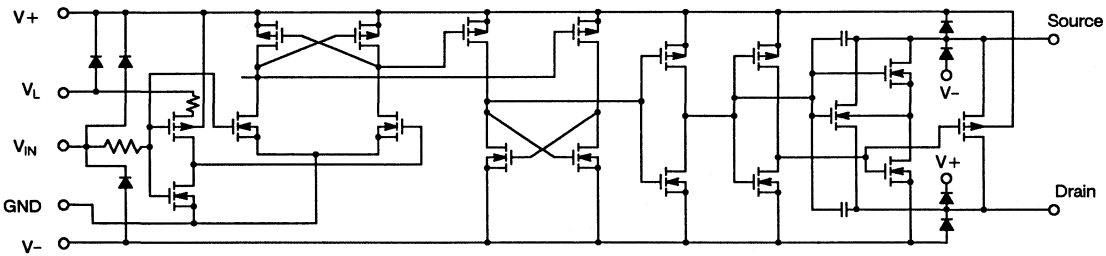
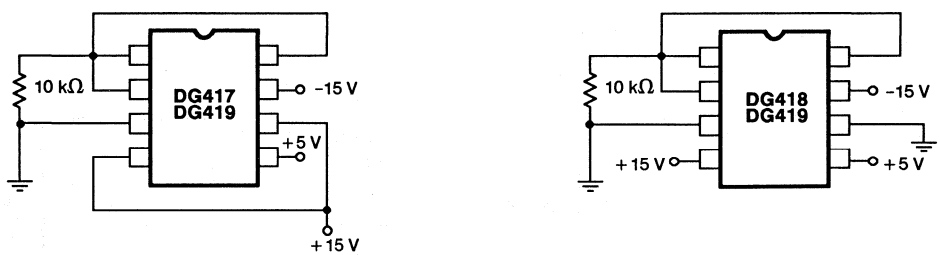


Figure 9.

BURN-IN CIRCUIT



DG419 is burned-in once in each configuration.

Figure 10.

Switched Signal Powers Analog Switch

The analog switch in Figure 11 derives power from its input signal, provided the input signal amplitude exceeds 4 volts and its frequency exceeds 1 kHz.

This circuit is useful when signals have to be routed to either of two remote loads. Only three conductors are required: one for the signal to be switched, one for the control signal and a common return.

A positive input pulse turns on the clamping diode D_1 and charges C_1. The charge stored on C_1 is used to power the chip; operation is satisfactory because the switch requires less than 1 μA of stand-by supply current. Loading of the signal source is imperceptible. The DG419's ON-resistance is a low 100 Ω for a 5 V input signal.

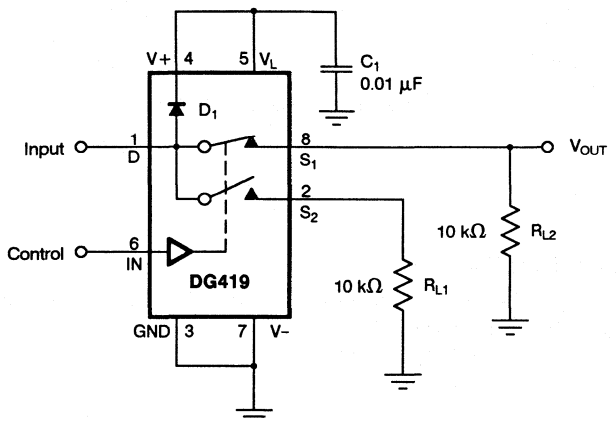


Figure 11. Switched Signal Powers Remote SPDT Analog Switch

Micropower UPS Transfer Switch

When V_{CC} drops to 3.3 V, the DG417 changes states, closing SW_1 and connecting the backup cell, as shown in Figure 12. D_1 prevents current from leaking back towards the rest of the circuit. Current consumption by the CMOS analog switch is around 100 pA; this ensures that most of the power available is applied to the memory, where it is really needed. In the stand-by mode, hundreds of μA are sufficient to retain data.

When the 5 V supply comes back up, the resistor divider senses the presence of at least 3.5 V, and causes a new change of state in the analog switch, restoring normal operation.

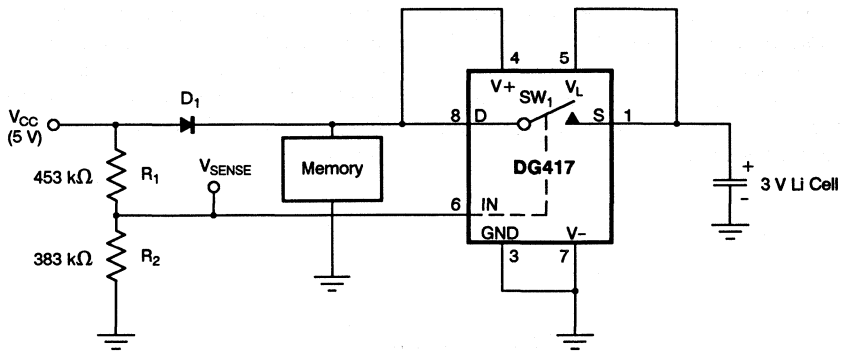


Figure 12. Micropower UPS Circuit

Programmable Gain Amplifier

The DG419, as shown in Figure 13, allows accurate gain selection in a small package. Switching into virtual ground reduces distortion caused by $r_{DS(ON)}$ variation as a function of analog signal amplitude.

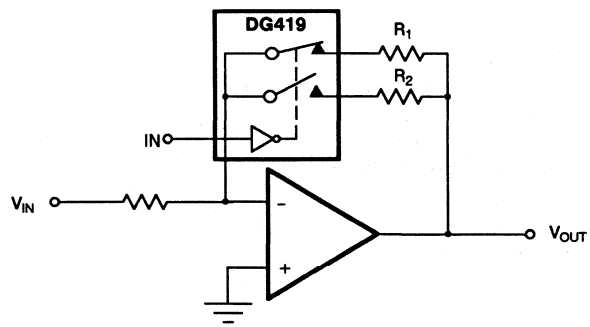


Figure 13. Programmable Gain Amplifier

Level Shifter

The DG419 may be used as a GaAs FET driver. It translates a TTL control signal into −8 V, 0 V level outputs to drive the gate.

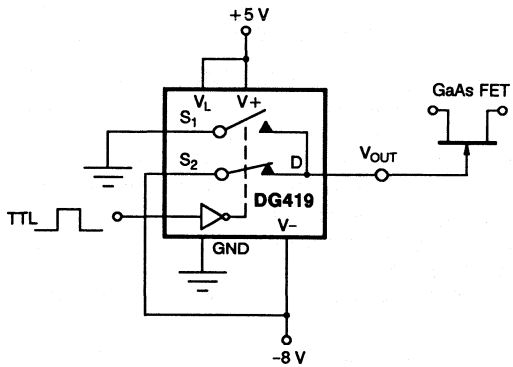


Figure 14. Level Shifter

5

DG421/423/425
Low-Power – High-Speed Latchable CMOS Analog Switches

Siliconix incorporated

FEATURES

- Latched Inputs
- ±15 Volt Input Range
- On-Resistance <35 Ω
- Fast Switching Action t_{ON} <250 ns
- Micropower Requirements (P_D <35 μW)
- TTL, CMOS Compatible

BENEFITS

- Wide Dynamic Range
- μP Compatible
- Reduced Component Count
- low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Battery Operation

APPLICATIONS

- High Performance Data Bus Switching
- Precision Sample and Hold Circuits
- Digital Filters
- μP Controlled Analog Systems
- Portable Instruments

DESCRIPTION

The DG421 series of dual monolithic analog switches features latchable logic inputs which simplify interfacing with microprocessors. This series combines fast switching speed (t_{ON} <250 ns), and low ON-resistance ($r_{DS(ON)}$ <35 Ω) making it ideally suited for battery powered industrial and military applications that require μP compatible analog switches.

To achieve high-voltage ratings and superior switching performance, the DG421 series is built on Siliconix's high voltage silicon gate CMOS process. Break-before-make is guaranteed for the DG423. An epitaxial layer prevents latchup.

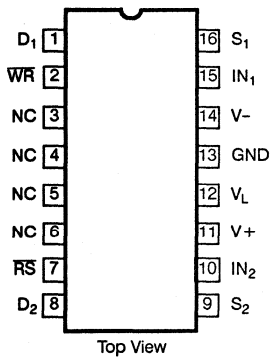
Each switch conducts equally well in both directions when ON and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is nearly flat over the full ±15 V analog range, rivaling JFET performance without the inherent dynamic range and supply voltage limitations.

When $\overline{WR}$ is set LOW the input data latches become transparent. When $\overline{WR}$ goes HIGH the latches store the logic control data. The $\overline{RS}$ pin is used to reset all the switches in the circuit to the default value (all inputs LOW) when it is set LOW.

This family offers three devices, which are differentiated by switch action as shown in the functional block diagrams. Packaging includes 16-pin plastic DIP and CerDIP. Performance grades include both the industrial, D suffix (-40 to 85°C) and the military, A suffix (-55 to 125°C) temperature ranges. Additionally, a 20-pin PLCC is available for the DG423.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

Dual-In-Line Package

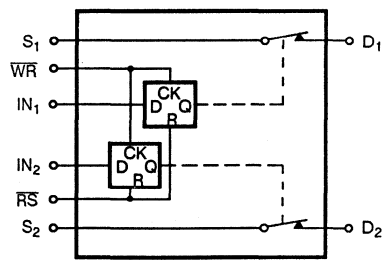


Top View

Order Numbers:

CerDIP: DG421AK, DG421AK/883
Plastic: DG421DJ

DG421



Two SPST Switches per Package

Truth Table*

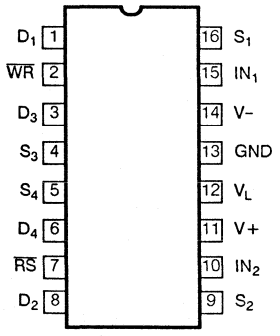
$\overline{WR}$	$\overline{RS}$	IN_X	Switch
0	1	0	OFF
		1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

*Switches Shown for Logic "1" Input

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

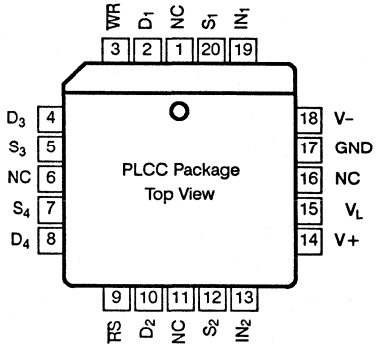
Dual-In-Line Package



Top View

Order Numbers:

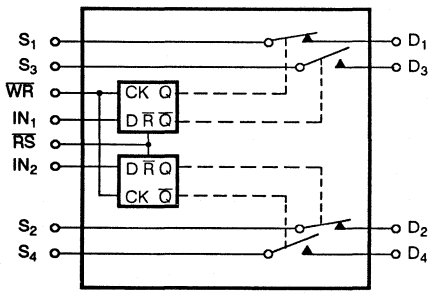
CerDIP: DG423AK, DG425AK
DG423AK/883, DG425AK/883
Plastic: DG423DJ, DG425DJ



Order Number:

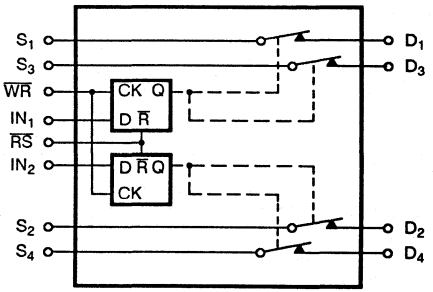
DG423DN

DG423



Two SPDT Switches per Package

DG425



Two DPST Switches per Package

Truth Table

$\overline{WR}$	$\overline{RS}$	IN_X	SW 1, 2	SW 3, 4
0	1	0 1	OFF ON	ON OFF

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

Truth Table

$\overline{WR}$	$\overline{RS}$	IN_X	Switch
0	1	0 1	OFF ON

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.4 V

Latch Operation Truth Table

IN_X	$\overline{RS}$	$\overline{WR}$	Latch/Switch X
X	1	0	Transparent Latch Operation
X	1	⌟	Control Data Latched-in, Switches On or Off as Selected by Last IN_X
X	0	X	All Latches Reset, Switches On or OFF as When IN_X = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 1
X	⌞	X	

5

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

V_L ..... (GND -0.3 V) to (V+) +0.3 V

Digital Inputs[1] V_S, V_D ..... V- minus 2 V to (V+ plus 2 V) or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 40 mA

Current, S or D (Pulsed 1 ms, 10% duty) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C

(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C

(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*

16-Pin Plastic DIP** ..... 470 mW

16-Pin CerDIP*** ..... 900 mW

20-Pin PLCC**** ..... 800 mW

*All leads welded or soldered to PC Board.

**Derate 6 mW/°C above 75°C.

***Derate 12 mW/°C above 75°C.

****Derate 10 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS[a]

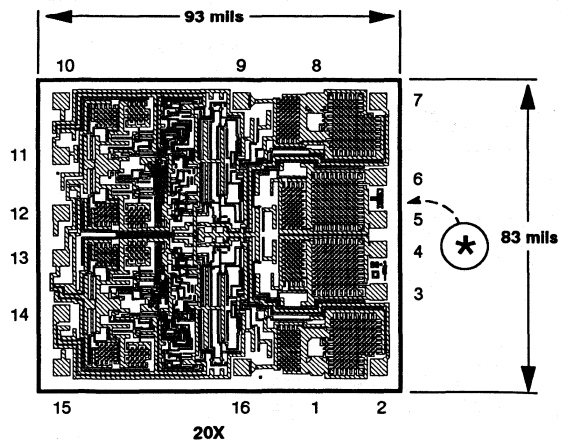
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]	$r_{DS(ON)}$	I_S = -200 mA, V_D = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full	25		35 45		35 45	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V	Room Full	-0.01	-0.25 -20	0.25 20	-0.25 -20	0.25 20	nA
	$I_{D(OFF)}$	V_D = -15.5 V, V_S = 15.5 V V_D = 15.5 V, V_S = -15.5 V	Room Full	-0.01	-0.25 -20	0.25 20	-0.25 -20	0.25 20	
Channel ON Leakage Current	$I_{D(ON)}$	V+ = 16.5 V, V- = -16.5 V	Room Full	-0.04	-0.4 -40	0.4 40	-0.4 -40	0.4 40	
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V all other = 2.4 V	Full	0.005	-0.5	0.5	-0.5	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V all other = 0.8 V	Full	0.005	-0.5	0.5	-0.5	0.5	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF	Room Full	170		250 300		250	ns
Turn-OFF Time	t_{OFF}	See Switching Time Test Circuit	Room Full	140		200 200		200	
Latch Timing	t_{WW}	R_L = 300 Ω, C_L = 35 pF V_S = ±10 V	Room Full		200 200		200		
	t_{DW}		Room Full		100 100		100		
	t_{WD}		Room Full		60 100		60		
Break-Before-Make Time Delay	t_D	DG423 ONLY R_L = 300 Ω, C_L = 35 pF	Room	25	5		5		
Charge Injection[c]	Q	C_L = 10 nF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	60					pC
OFF Isolation Reject Ratio		R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	65					dB

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)									
Crosstalk (Channel-to-Channel)		Between Any Two Channels R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	76					dB
Source Off	$C_{S(OFF)}$	f = 1 MHz	Full	9					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Full	9					
Channel ON Capacitance	$C_{D+S(ON)}$		Full	18					
POWER SUPPLY									
Positive Supply Current	I+	V+ = 16.5 V, C- = -16.5 V V_{IN} = 0 or 5 V	Room Full	0.0001		1 5		1 5	µA
Negative Supply Current	I-		Room Full	-0.0001	-1 -5		-1 -5		
Logic Supply Current	I_L		Room Full	0.0001		1 5		1 5	
Ground Current	I_{GND}		Room Full	-0.0001	-1 -5		-1 -5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function DG423/5	Function DG421
1	D_1	D_1
2	$\overline{WR}$	$\overline{WR}$
3	D_3	NC
4	S_3	NC
5	S_4	NC
6	D_4	NC
7	$\overline{RS}$	$\overline{RS}$
8	D_2	D_2
9	S_2	S_2
10	IN_2	IN_2
11	V+ (substrate)	V+ (substrate)
12	V_L	V_L
13	GND	GND
14	V-	V-
15	IN_1	IN_1
16	S_1	S_1

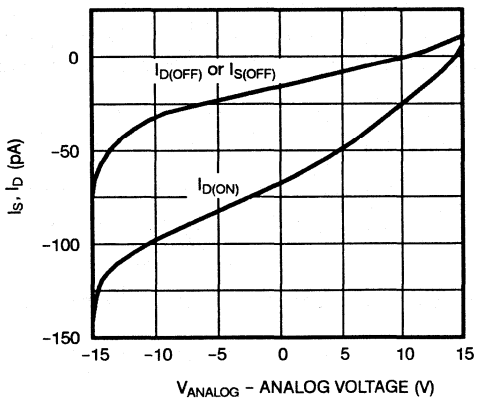
CSHD-I*

126 NMOS
114 PMOS
16 Capacitors
12 Diodes
12 Resistors

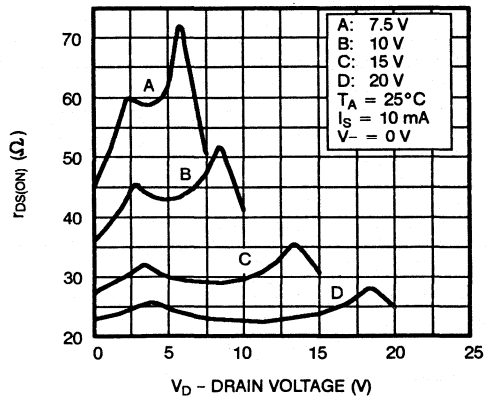
***A = DG421 or DG423**
B = DG421 or DG425

TYPICAL CHARACTERISTICS

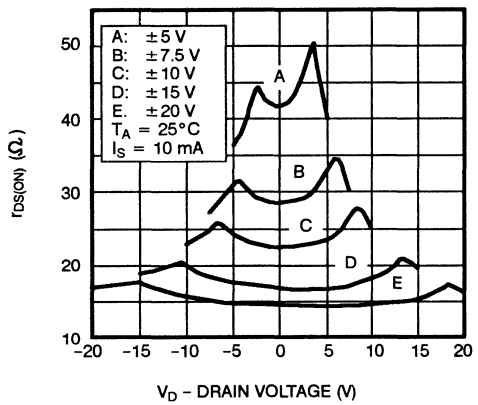
Leakage Currents vs. Analog Voltage



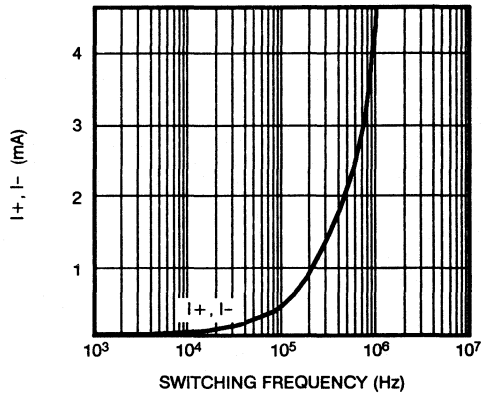
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



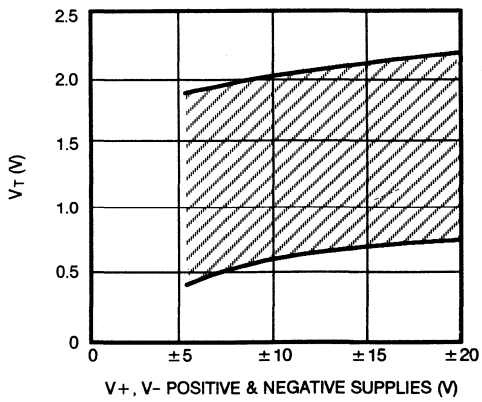
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



Supply Currents vs. Switching Frequency

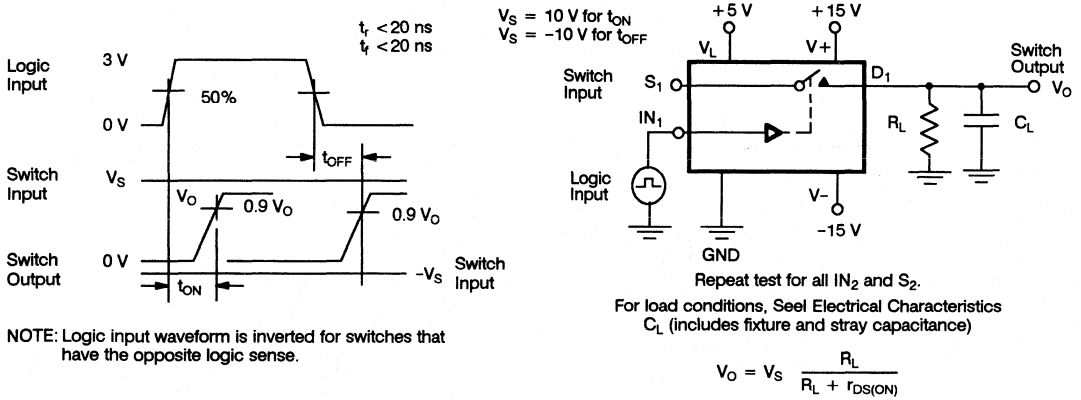


Input Switching Threshold vs. V+ and V- Supply Voltages



TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

Repeat test for all IN_2 and S_2.

For load conditions, Seel Electrical Characteristics
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Time

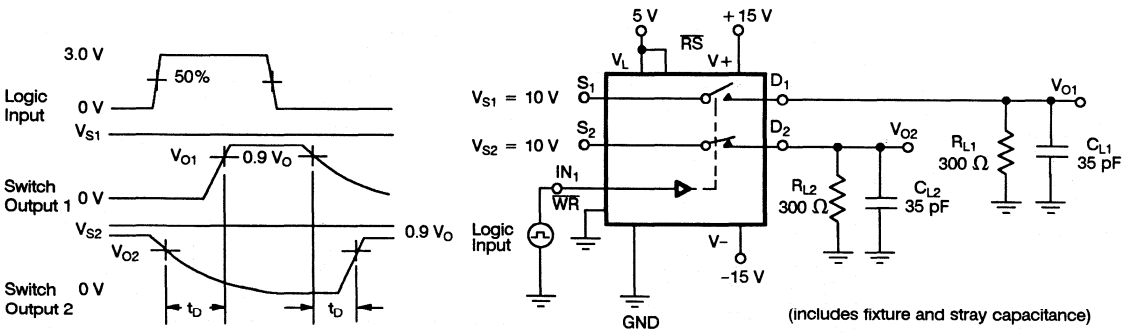
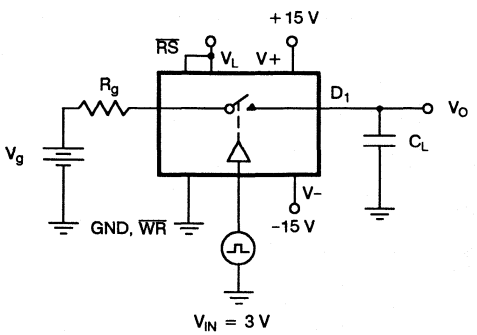
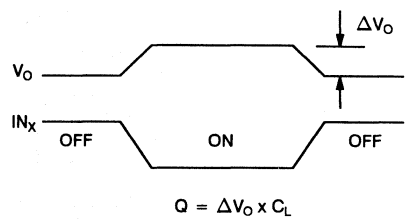


Figure 2. Break-Before-Make





$$Q = \Delta V_O \times C_L$$

IN_X dependent on switch configuration Input polarity determined by sense of switch.

Figure 3. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

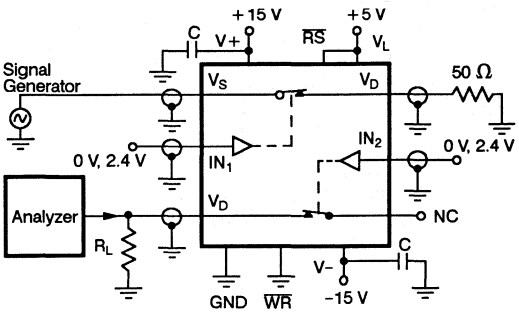


Figure 4. Crosstalk

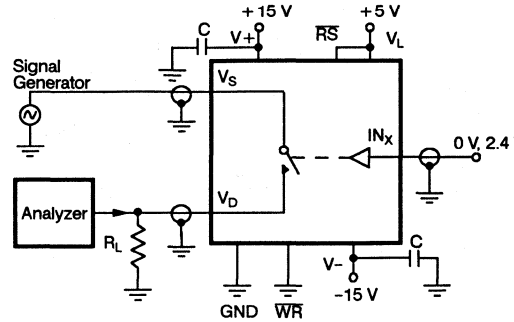


Figure 5. Off Isolation

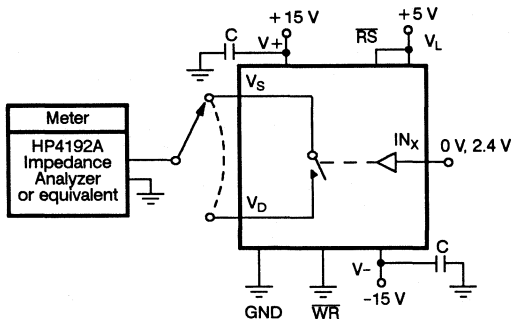


Figure 6. Source/Drain Capacitances

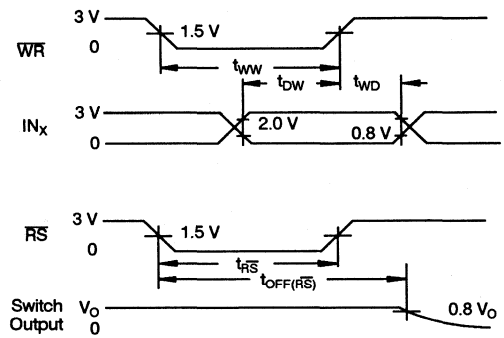


Figure 7. Latch Timing

BURN-IN CIRCUIT

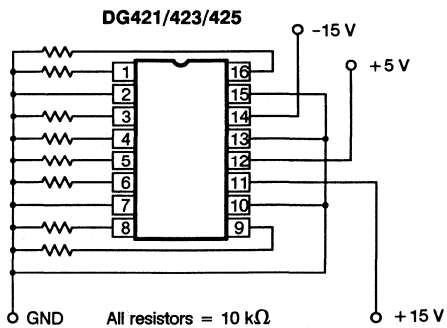
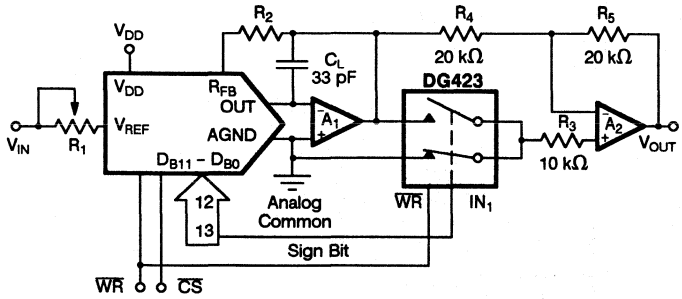


Figure 8.

APPLICATIONS

Figure 9 shows a circuit configured to increase the effective resolution of the 12-bit DAC to 13 bits. The circuit operates with a sign plus magnitude code. A sign bit of "0" connects R_3 to GND, giving 12-bit resolution per quadrant.



12-Bit Plus Sign Magitude Code Table

Sign Bit	Digital Input MSB LSB	Analog Output (V_{OUT})
0	1111 1111 1111	+(4095/4096)V_{IN}
0	0000 0000 0000	0 Volts
1	0000 0000 0000	0 Volts
1	1111 1111 1111	+(4095/4096)V_{IN}

Figure 9. 12-Bit Plus Sign Magnitude D/A Converter

When switch S_1 of Figure 10 is closed, the op amp is placed in the familiar unity-gain non-inverting configuration. When switch S_2 is closed and S_1 is open the gain is given by:

$$A_V = 1 + \frac{R_1}{R_2}$$

The microprocessor system $\overline{WR}$ must gate the decoder output to ensure proper timing.

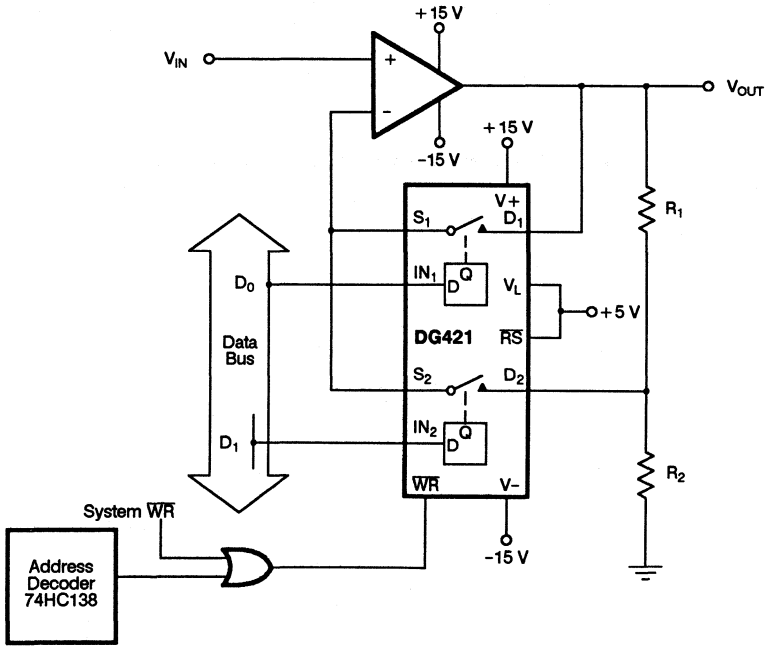
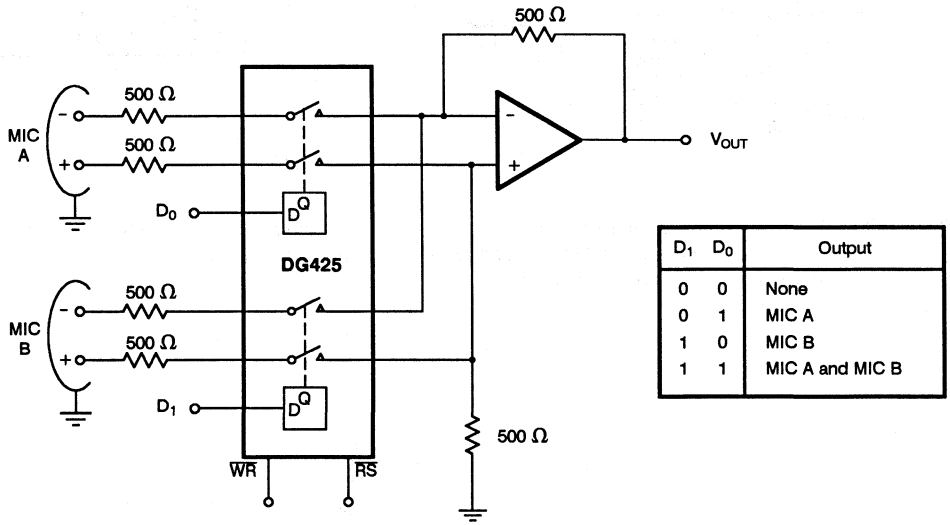


Figure 10. Bus-Controlled Precision Gain-Ranging Circuit

5

Figure 11 shows a balanced-line microphone input stage that provides selection or summing between two balanced-line microphones and also performs differential-to-single-ended conversion. Either MIC A or MIC B can be selected, and neither and/or both may be summed at the output. This configuration uses "virtual ground" switching, a method which minimizes distortion resulting from the analog switch on-resistance modulation. The actual voltage swings experienced by the analog switch barely exceed 1 V for a 15-V full-scale range input.



D_1	D_0	Output
0	0	None
0	1	MIC A
1	0	MIC B
1	1	MIC A and MIC B

Figure 11. Bus-Controlled Selector for Balanced-Line Microphones

Siliconix incorporated

DG441/442
Monolithic Quad SPST CMOS Analog Switches

FEATURES

- ON-Resistance $<85\ \Omega$
- Low Power Consumption (P_D <1.6 mW)
- Fast Switching Action
  t_{ON} <250 ns
  t_{OFF} <120 ns (DG441)
- ESD Protection > ±4000 V
- Low Charge Injection
- DG201A/DG202 Upgrades
- TTL, CMOS Compatible
- Single Supply Capability

BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Error
- Simplifies Retrofit
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment

DESCRIPTION

The DG441 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog and audio signals. Combining low ON-resistance (<85 Ω) with high speed (t_{ON} <250 ns), the DG441 series is ideally suited for upgrading DG201A/DG202 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high voltage ratings and superior switching performance, the DG441 series is built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is very flat over the full ±5 V analog range.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. The DG441/442 are available in 16-pin plastic, CerDIP and SO packages. Performance grades include both the military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature range.

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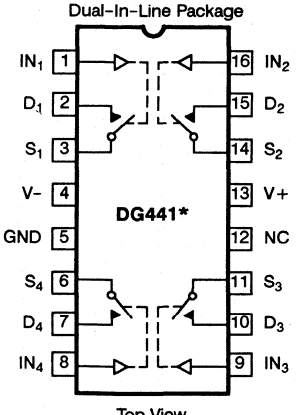
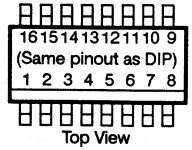
FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package



Top View
Order Numbers:
CerDIP: DG441AK, DG441AK/883
DG442AK, DG442AK/883
Plastic: DG441DJ, DG442DJ

Narrow Body
SO Package



Top View

Order Numbers:
DG441DY, DG442DY

Four SPST Switches per Package
Truth Table

Logic	Switch DG441*	Switch DG442
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches shown for logic "1" input.

Siliconix incorporated

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V

GND to V- ..... 25 V

Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+) +2 V
or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin CerDIP*** ..... 900 mW
16-Pin Narrow Body SO**** ..... 600 mW

*All leads welded or soldered to PC Board.
**Derate 6 mW/°C above 75°C.
***Derate 12 mW/°C above 75°C.
****Derate 7.6 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS (DUAL SUPPLY)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]	$r_{DS(ON)}$	I_S = -10 mA, V_D = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full	50		85 100		85 100	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Hot	0.01	-0.5 -20	0.5 20	-0.5 -20	0.5 20	nA
	$I_{D(OFF)}$		Room Hot	0.01	-0.5 -20	0.5 20	-0.5 -20	0.5 20	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V- = -16.5 V V_S = V_D = ±15.5 V	Room Hot	0.08	-0.5 -40	0.5 40	-0.5 -40	0.5 40	
DIGITAL CONTROL									
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	-0.00001	-0.5	0.5	-0.5	0.5	µA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.00001	-0.5	0.5	-0.5	0.5	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF	Room	150		250		250	ns
Turn-OFF Time DG441	t_{OFF}	V_S = ±10 V	Room	90		120		120	
Turn-OFF Time DG442	t_{OFF}	See Figure 1	Room	110		170		170	
Charge Injection	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-1					pC
OFF Isloation[c]		R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	60					dB
Crosstalk[c] (Channel-to-Channel)		Any Other Channel Switches R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	-100					
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz	Room	4					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	4					
Channel ON Capacitance[d]	$C_{D + S(ON)}$	V_{ANALOG} = 0 V	Room	16					

SPECIFICATIONS (DUAL SUPPLY)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V	Full	15		100		100	µA
Negative Supply Current	I-		Room Full	-0.0001	-1 -5		-1 -5		
Ground Current	I_{GND}		Full	-15	-100		-100		

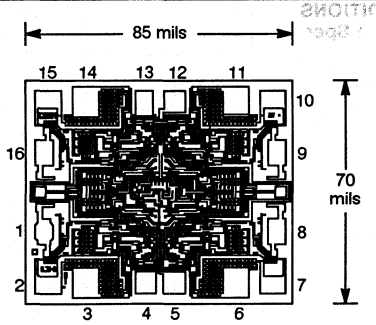
SPECIFICATIONS (SINGLE SUPPLY)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source ON-Resistance[e]	$r_{DS(ON)}$	I_S = -10 mA, V_D = 3V, 8 V V+ = 10.8 V	Room Full	100		160 200		160 200	Ω
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF	Room	300		400		400	ns
Turn-OFF Time	t_{OFF}	See Test Circuit, V_S = 8 V	Room	60		200		200	
Charge Injection	Q	C_L = 1 nF, V_{gen} = 6 V, R_{gen} = 0 Ω	Room	2					pC
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V	Full	15		100		100	µA
Negative Supply Current	I-		Room Full	-0.0001	-1 -100		-1 -100		
Ground Current	I_{GND}		Full	-15	-100		-100		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

5

DIE TOPOGRAPHY



Pad No.	Function
1	N_1
2	D_1
3	S_1
4	V-
5	GND
6	S_4
7	D_4
8	N_4
9	N_3
10	D_3
11	S_3
12	NC
13	V+ (Substrate)
14	S_2
15	D_2
16	N_2

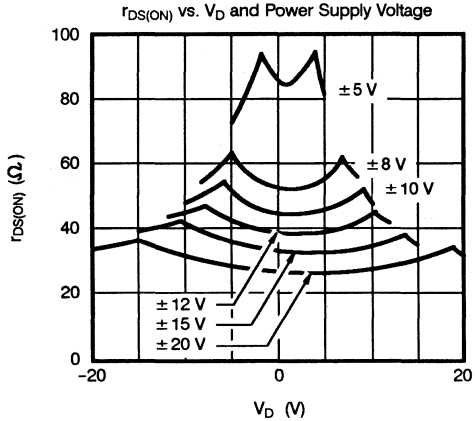
CSHM-E, F
4 Capacitors
2 Resistors
1 Zener Diode

32 p-channel Enhancement MOSFET's
36 n-channel Enhancement MOSFET's
2 NPN Bipolar FETs

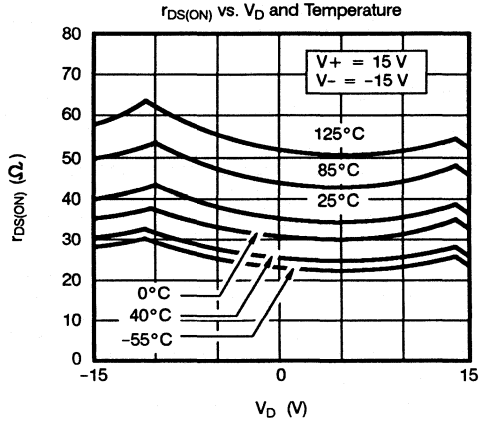
8 Diodes

TYPICAL CHARACTERISTICS

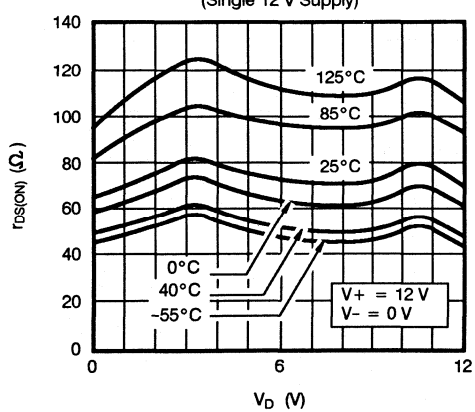
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



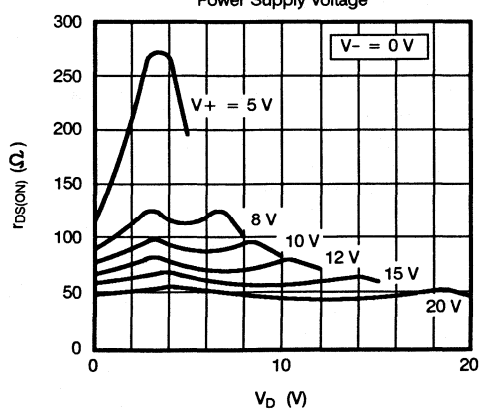
$r_{DS(ON)}$ vs. V_D and Temperature



$r_{DS(ON)}$ vs. V_D and Temperature (Single 12 V Supply)

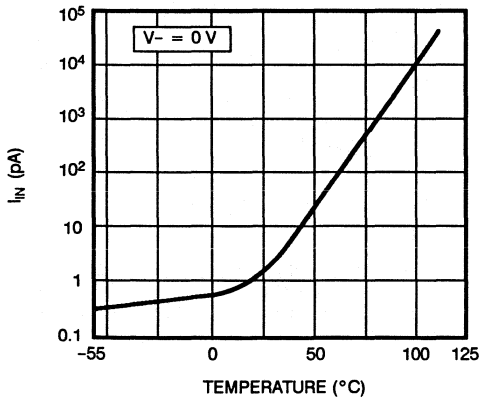


$r_{DS(ON)}$ vs. V_D and Unipolar Power Supply Voltage

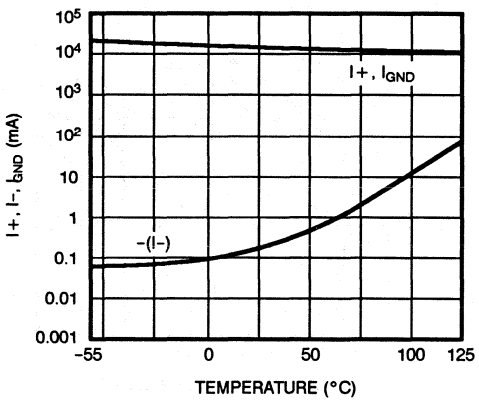


TYPICAL CHARACTERISTICS (Cont'd)

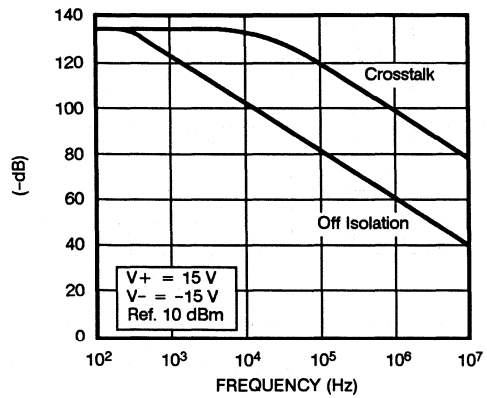
Input Current vs. Temperature



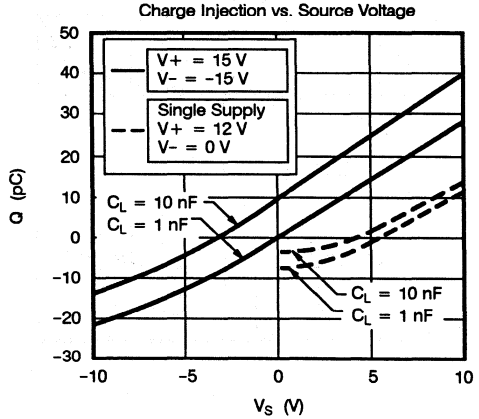
Supply Current vs. Temperature



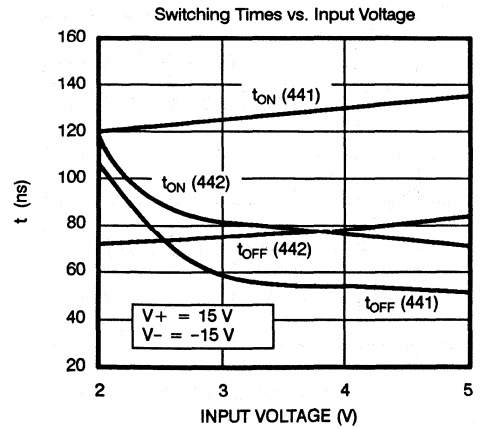
Crosstalk and Off Isolation vs. Frequency



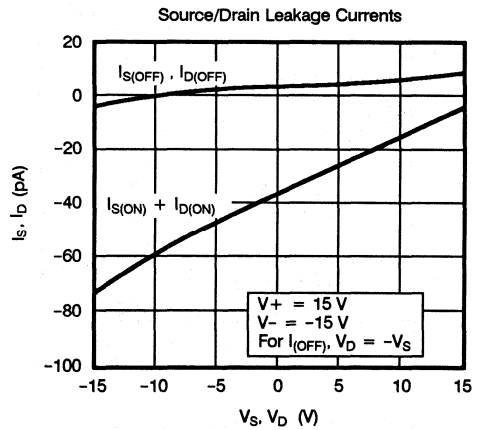
Charge Injection vs. Source Voltage



Switching Times vs. Input Voltage



Source/Drain Leakage Currents



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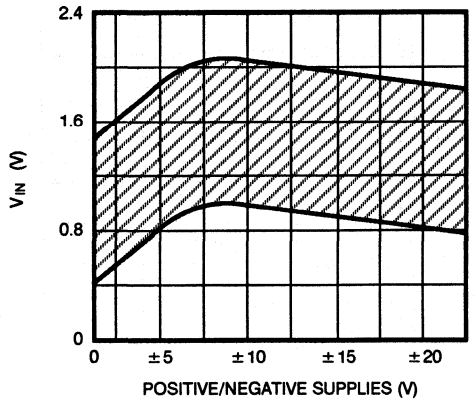
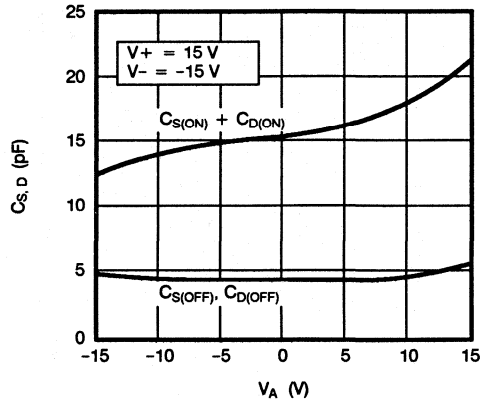
TYPICAL CHARACTERISTICS (Cont'd)

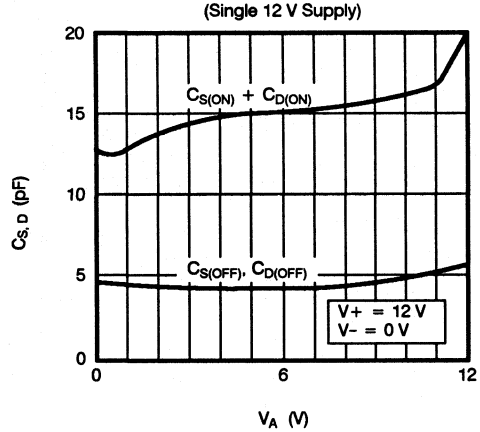
Switching Threshold vs. Supply Voltage



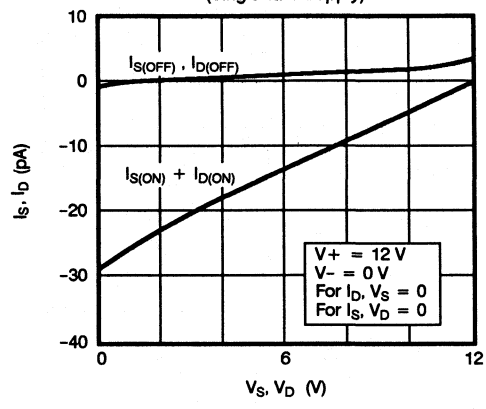
Source/Drain Capacitance vs. Analog Voltage



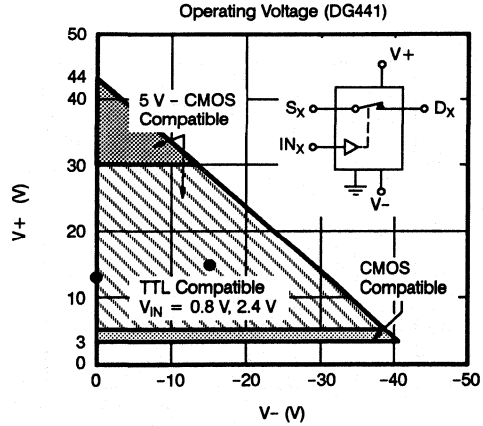
Source/Drain Capacitance vs. Analog Voltage (Single 12 V Supply)



Source/Drain Leakage Currents (Single 12 V Supply)

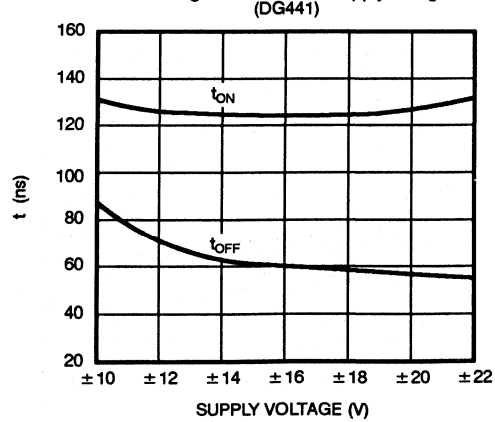


Operating Voltage (DG441)

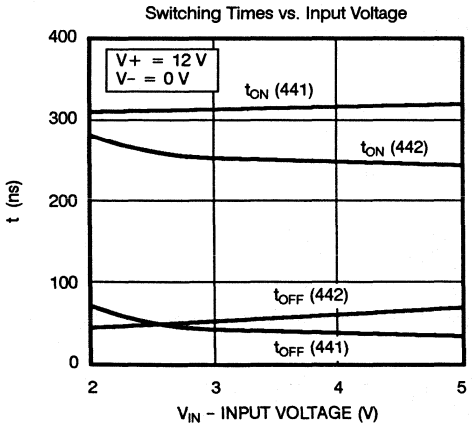


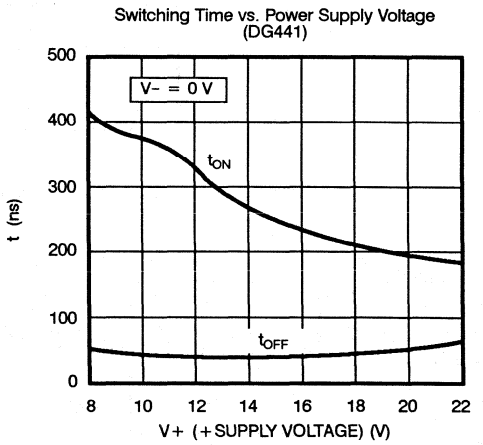
● = Voltages Used for Production Testing

Switching Time vs. Power Supply Voltage (DG441)



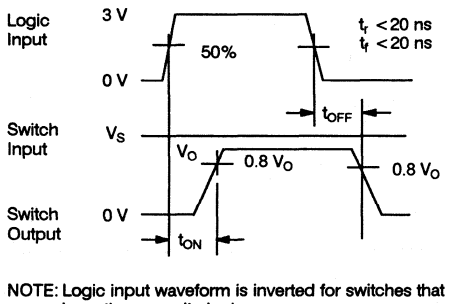
TYPICAL CHARACTERISTICS (Cont'd)



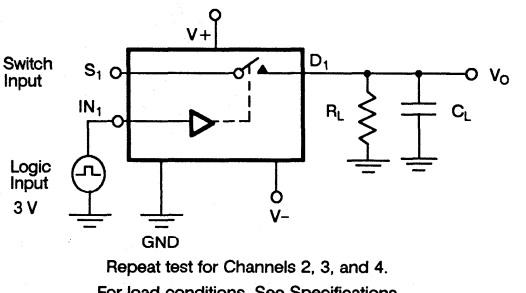


TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.



Repeat test for Channels 2, 3, and 4.

For load conditions, See Specifications
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Time

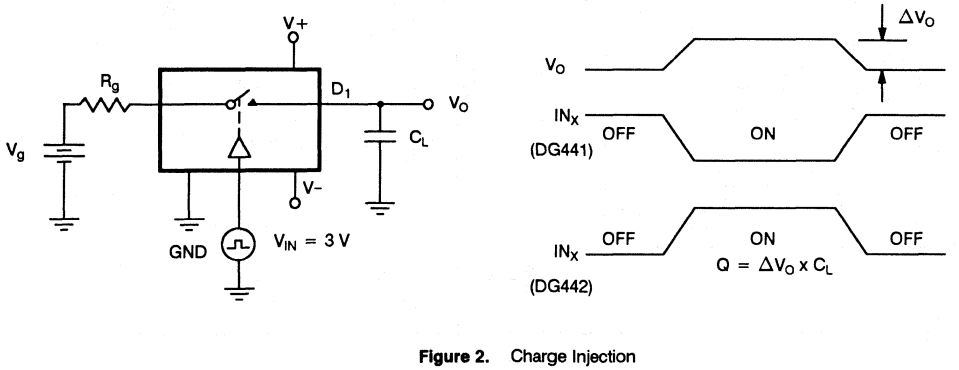


Figure 2. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

$$\text{Off Isolation} = 20 \log \frac{V_S}{V_D}$$

C = 1 µF tantalum in parallel with 0.01 µF ceramic

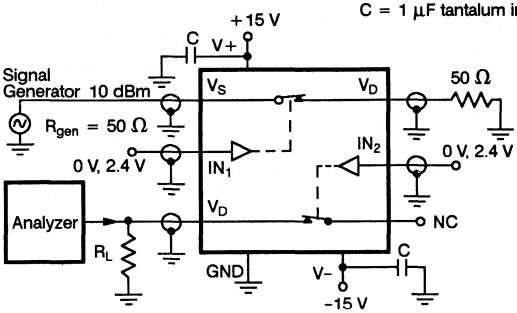


Figure 3. Crosstalk

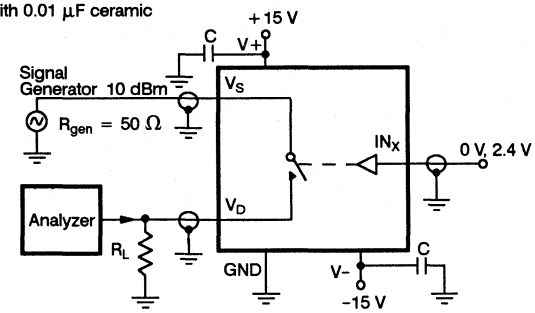


Figure 4. Off Isolation

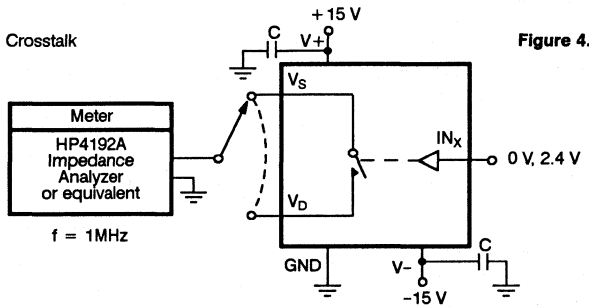


Figure 5. Source/Drain Capacitances

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

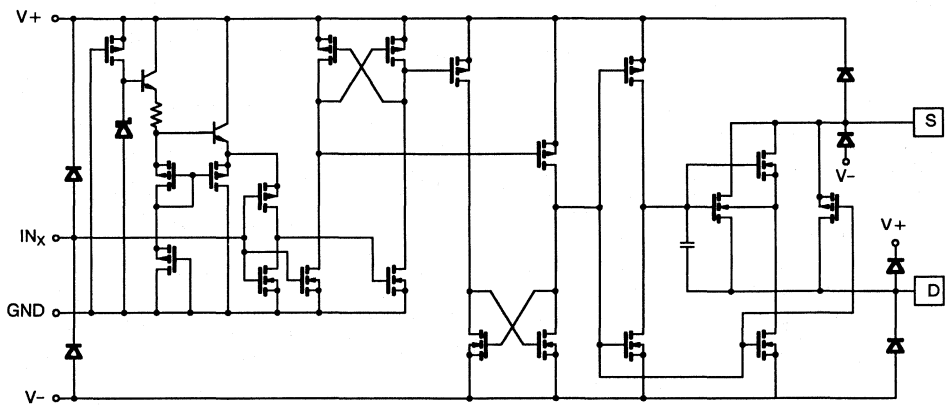
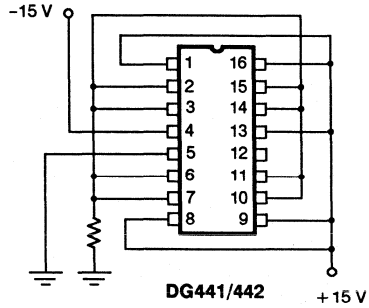


Figure 6.

BURN-IN CIRCUIT



Note: All resistors are 10 kΩ unless otherwise specified

Figure 7.

APPLICATIONS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	$V_{INH(MIN)}$ HIGH Logic Input Voltage (V)	$V_{INL(MAX)}$ LOW Logic Input Voltage (V)	V_S or V_D Analog Signal Range (V)
20	-20	2.4	0.8	-20 to 20
15	-15	2.4	0.8	-15 to 15
10	-10	2.4	0.8	-10 to 10
5	-5	2.0	0.5	-5 to 5
12	0	2.4	0.8	0 to 12
5	0	2.0	0.5	0 to 5

Figure 8.

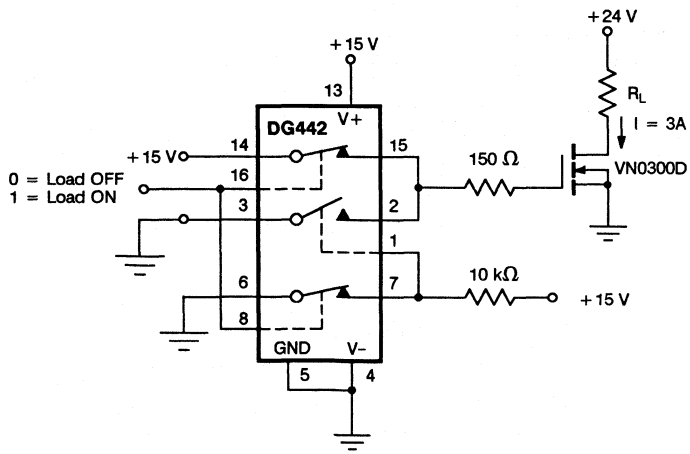


Figure 9. Power MOSFET Driver

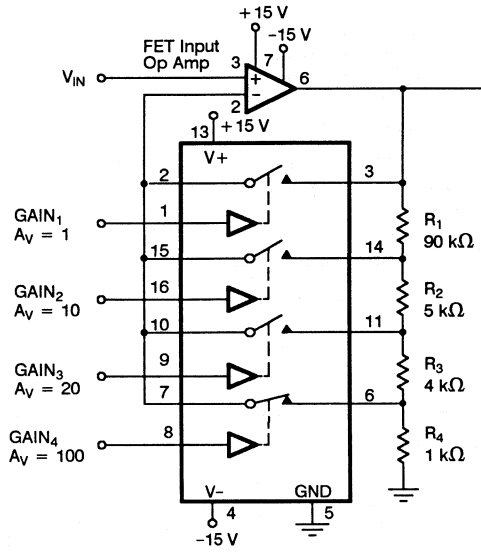


Figure 10. Precision-Weighted Resistor Programmable-Gain Amplifier

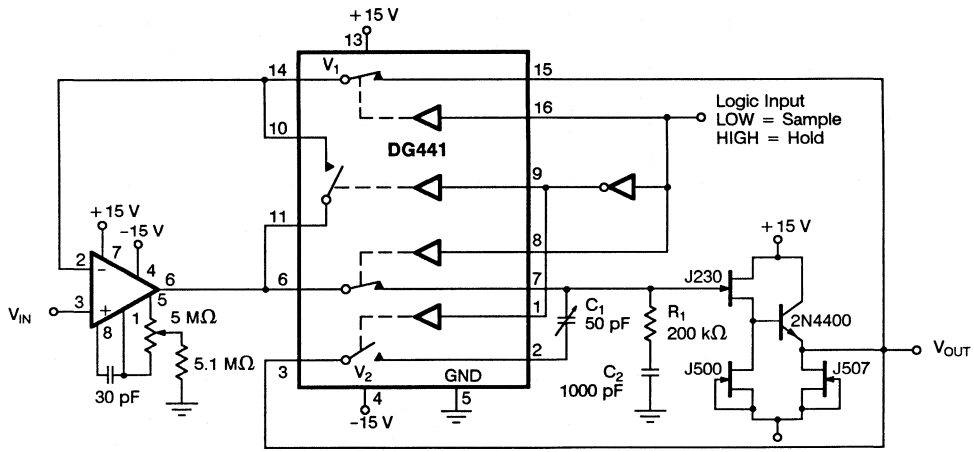


Figure 11. Precision Sample-and-Hold

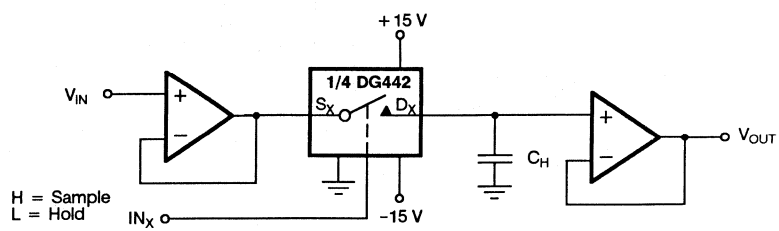


Figure 12. Open Loop Sample-and-Hold

Siliconix incorporated

DG444/445
Low Cost Quad SPST CMOS Analog Switches

FEATURES

- ON-Resistance $<85\ \Omega$
- Low Power Consumption (P_D <35 mW)
- Fast Switching Action
  t_{ON} <250 ns
  t_{OFF} <120 ns (DG444)
- Low Cost
- ESD Protection > ±4000 V
- Low Charge Injection
- DG211/DG212 Upgrades
- TTL, CMOS Compatible

BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply
- Faster Throughput
- Improved Reliability
- Reduced Pedestal Error
- Simple Interfacing

APPLICATIONS

- Audio and Video Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Single Supply Circuits

DESCRIPTION

The DG444 series of monolithic quad analog switches was designed to provide high speed, low error switching of analog signals. Combining low power (<35 µW) with high speed (t_{ON} < 250 ns), the DG444 series is ideally suited for upgrading DG211/212 sockets. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

To achieve high-voltage ratings and superior switching performance, the DG444 series is built on Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents latchup.

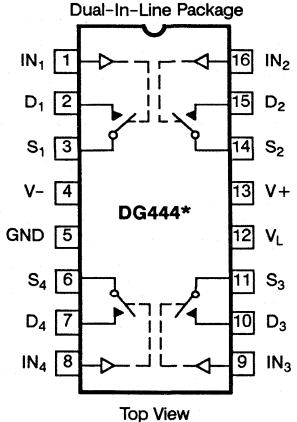
Each switch conducts equally well in both directions when ON, and blocks up to 30 volts peak-to-peak when OFF. ON-resistance is very flat over the full ± 15 V analog range.

The two devices in this series are differentiated by the type of switch action as shown in the functional block diagrams for each. Packaging options include the 16-pin plastic and small outline. The performance grade for this series is the industrial, D suffix (-40 to 85°C) temperature range.

5

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

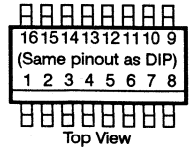
Dual-In-Line Package



Top View
Order Numbers:

Plastic: DG444DJ, DG445DJ

Narrow Body
SO Package



Top View

Order Numbers:
DG444DY, DG445DY

Four SPST Switches per Package
Truth Table

Logic	Switch DG444*	Switch DG445
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches shown for logic "1" input.

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
GND to V- ..... 25 V
V_L ..... (GND -0.3 V) to (V+) + 0.3 V
Digital Inputs[1], V_S, V_D ..... (V-) -2 V to (V+) +2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA
Storage Temperature (D Suffix) ..... -65 to 125°C
Operating Temperature (D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW
16-Pin Narrow Body SO**** ..... 600 mW

*All leads welded or soldered to PC Board.
**Derate 6 mW/°C above 75°C.
***Derate 12 mW/°C above 75°C.

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH							
Analog Signal Range[c]	V_{ANALOG}		Full		-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = ±8.5 V V+ = 13.5 V, V- = -13.5 V	Room Full	50		85 100	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V V_D = ±15.5 V, V_S = ∓15.5 V	Room Hot	0.01	-0.5 -20	0.5 20	nA
	$I_{D(OFF)}$		Room Hot	0.01	-0.5 -20	0.5 20	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5 V, V- = -16.5 V V_S = V_D = ±15.5 V	Room Hot	0.08	-0.5 -40	0.5 40	
DIGITAL CONTROL							
Input Current with V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V All Other = 2.4 V	Full	-0.00001	-0.5	0.5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V All Other = 0.8 V	Full	0.00001	-0.5	0.5	
DYNAMIC CHARACTERISTICS							
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF	Room	150		250	ns
Turn-OFF Time DG444	t_{OFF}	V_S = ±10 V	Room	90		120	
Turn-OFF Time DG445		See Figure 1	Room	110		170	
Charge Injection[c]	Q	C_L = 1 nF, V_S = 0 V V_{gen} = 0 V, R_{gen} = 0 Ω	Room	-1			pC
OFF Isloation[c]		R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room	60			dB
Crosstalk (Channel-to-Channel)[c]		Any Other Channel Switches R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	100			
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz	Room	4			pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	4			
Channel ON Capacitance[d]	$C_{D + S(ON)}$	V_{ANALOG} = 0 V	Room	16			

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES							
Positive Supply Current	I+	V+ = 16.5 V, V- = -16.5 V_{IN} = 0 or 5 V	Room Hot	0.001		1 5	µA
Negative Supply Current	I-		Room Hot	-0.0001	-1 -5		
Logic Supply Current	I_L		Room Hot	0.001		1 5	
Ground Current	I_{GND}		Room Hot	-0.001	-1 -5		

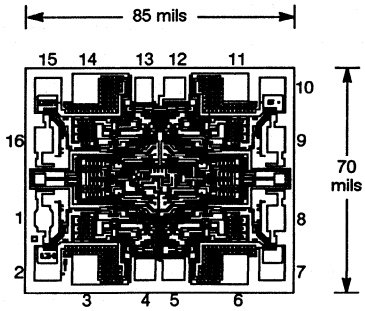
SPECIFICATIONS (UNIPOLAR SUPPLIES)[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH							
Analog Signal Range[c]	V_{ANALOG}		Full		0	12	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = 3V, 8 V V+ = 10.8 V, V_L = 5.25 V	Room Full	100		160 200	Ω
DYNAMIC CHARACTERISTICS							
Turn-ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, V_S = 8 V	Room	300		400	ns
Turn-OFF Time	t_{OFF}	See Switching Time Test Circuit	Room	60		200	
Charge Injection[c]	Q	C_L = 1 nF, V+ = 12 V V_{gen} = 6 V, R_{gen} = 0 Ω	Room	2			pC
POWER SUPPLIES							
Positive Supply Current	I+	V+ = 13.2 V V_{IN} 0 or 5 V	Room Full	0.001		1 5	µA
Negative Supply Current	I-	V_{IN} 0 or 5 V	Room Full	-0.0001	-1 -5		
Logic Supply Current	I_L	V_L = 5.25 V V_{IN} 0 or 5 V	Room Full	0.001		1 5	
Ground Current	I_{GND}	V_{IN} = 0 or 5 V	Room Full	-0.001	-1 -5		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

Siliconix incorporated

DIE TOPOGRAPHY



Pad No.	Function
1	IN_1
2	D_1
3	S_1
4	V-
5	GND
6	S_4
7	D_4
8	IN_4
9	IN_3
10	D_3
11	S_3
12	NC
13	V+ (Substrate)
14	S_2
15	D_2
16	IN_2

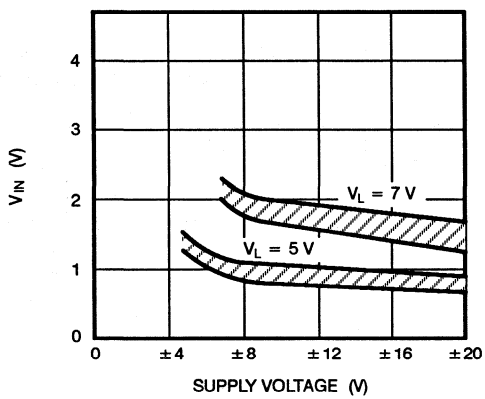
CSHM-C, D
4 Capacitors
1 Resistor

28 p-channel Enhancement MOSFET's
36 n-channel Enhancement MOSFET's

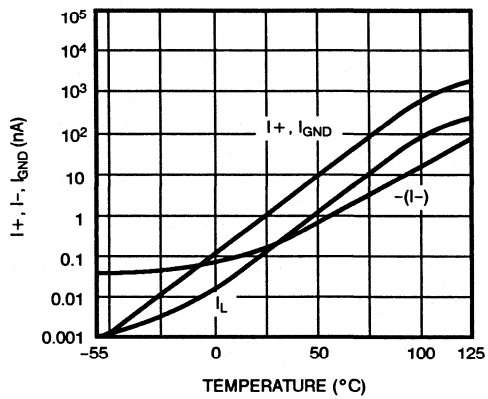
8 Diodes

TYPICAL CHARACTERISTICS

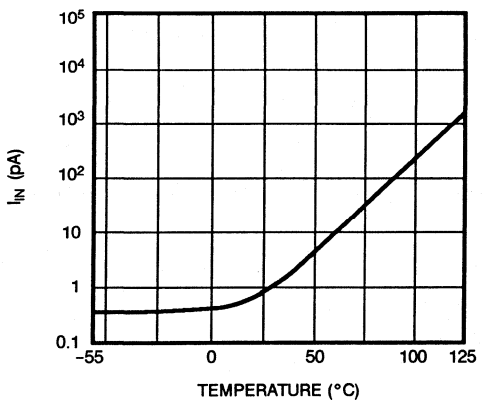
Switching Threshold vs. Supply Voltage



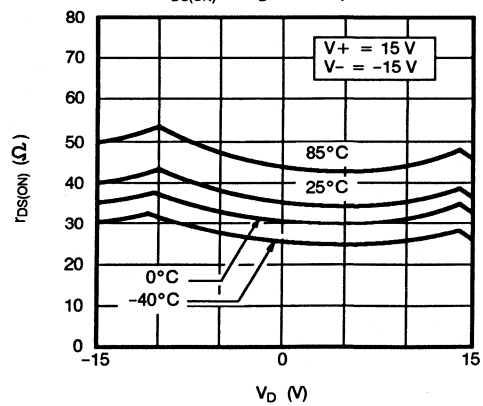
Supply Current vs. Temperature



Input Current vs. Temperature

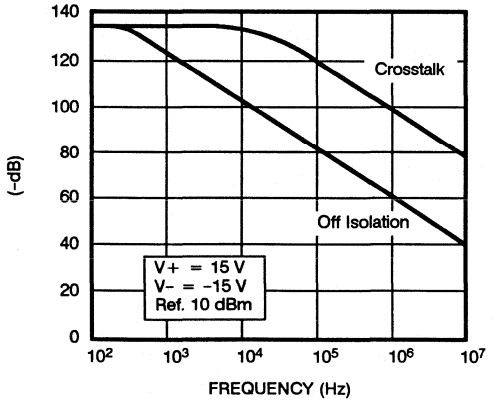


$r_{DS(ON)}$ vs. V_D and Temperature

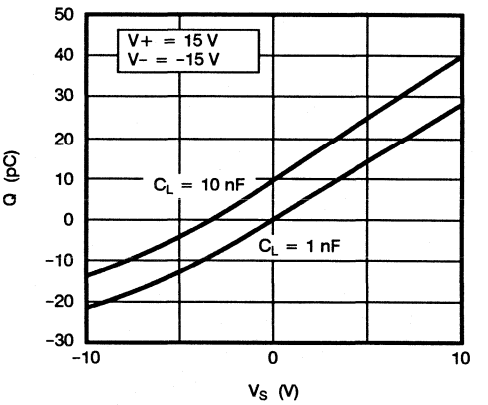


TYPICAL CHARACTERISTICS (Cont'd)

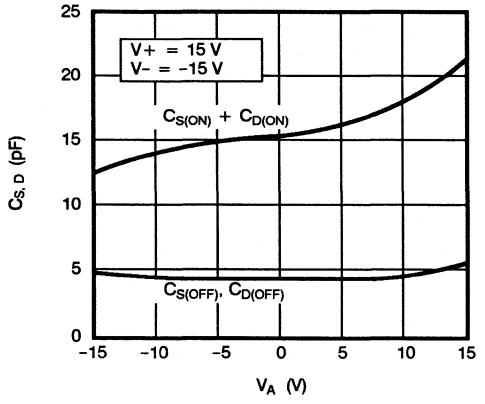
Crosstalk and Off Isolation vs. Frequency



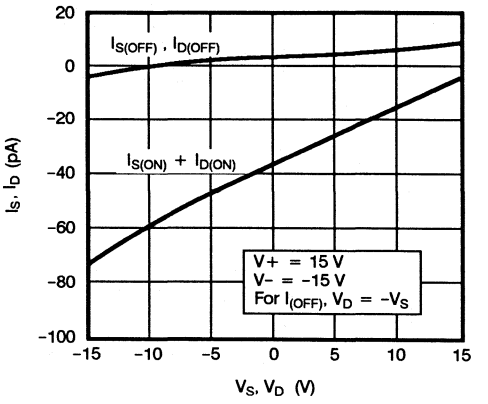
Charge Injection vs. Source Voltage



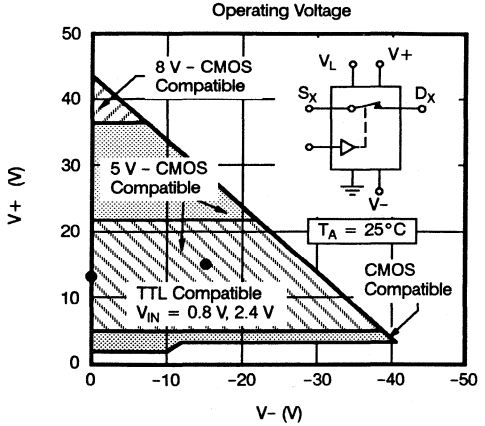
Source/Drain Capacitance vs. Analog Voltage



Source/Drain Leakage Currents

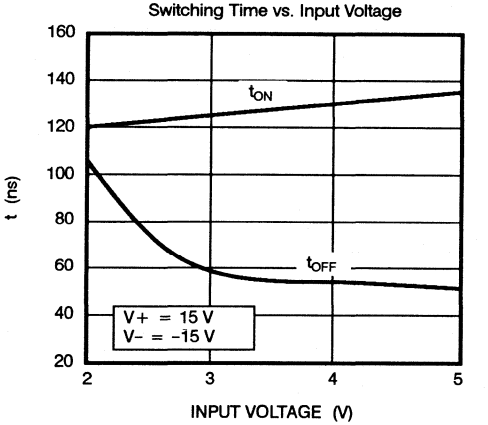


Operating Voltage



● = Voltages Used for Production Testing

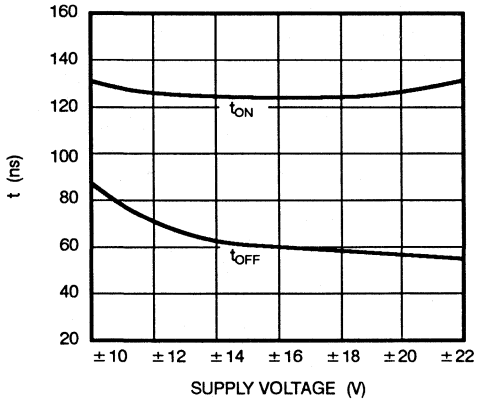
Switching Time vs. Input Voltage



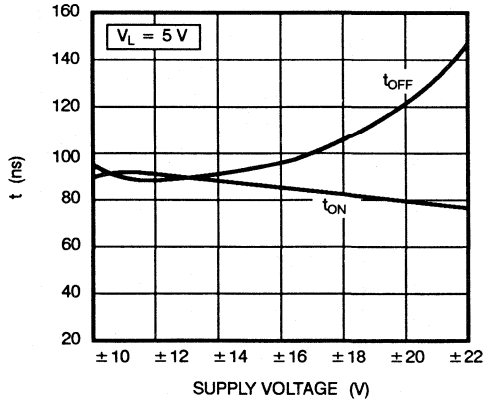
5

TYPICAL CHARACTERISTICS (Cont'd)

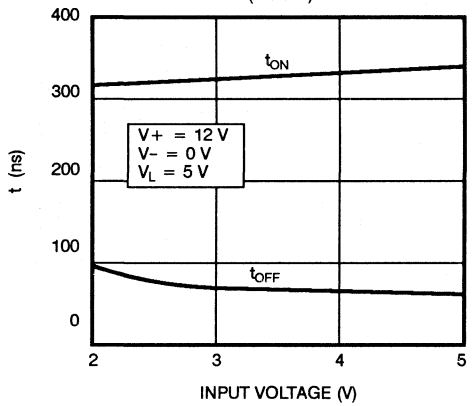
Switching Time vs. Power Supply Voltage (DG444)



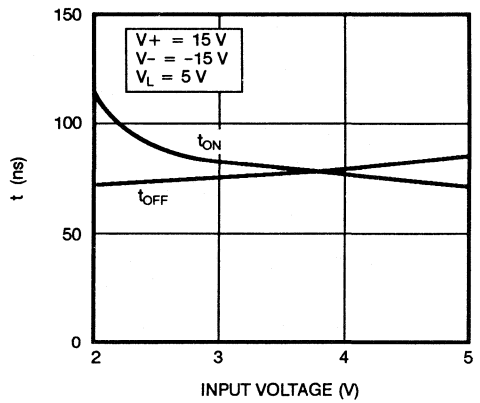
Switching Time vs. Power Supply Voltage (DG445)



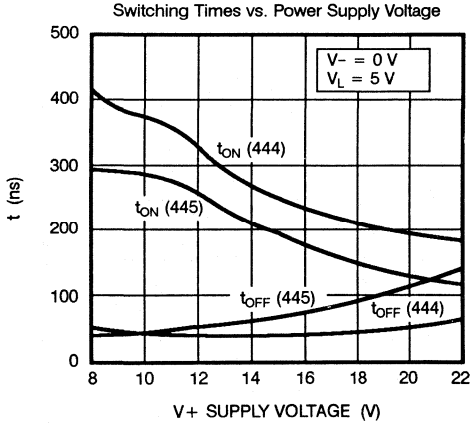
Switching Time vs. Input Voltage (DG444)



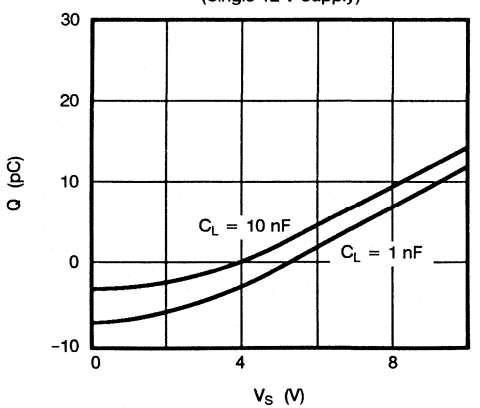
Switching Time vs. Input Voltage (DG445)



Switching Times vs. Power Supply Voltage

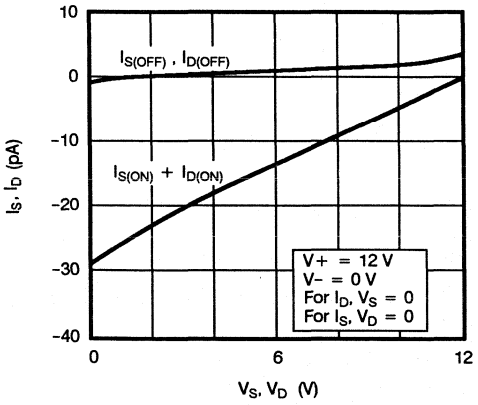


Charge Injection vs. Source Voltage (Single 12 V Supply)

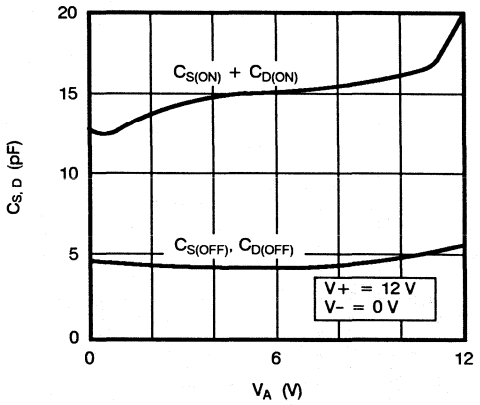


TYPICAL CHARACTERISTICS (Cont'd)

Source/Drain Leakage Currents
(Single 12 V Supply)

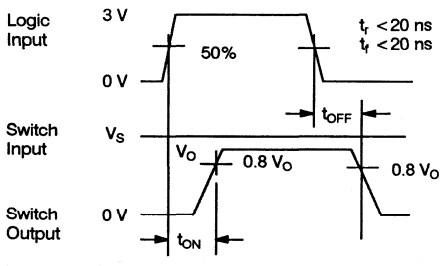


Source/Drain Capacitance vs. Analog Voltage
(Single 12 V Supply)

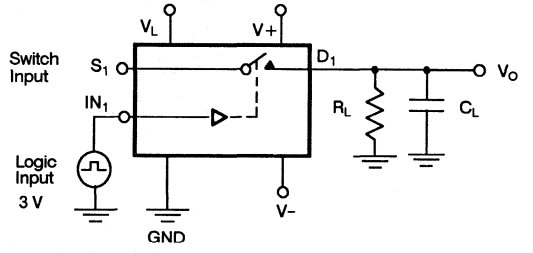


TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

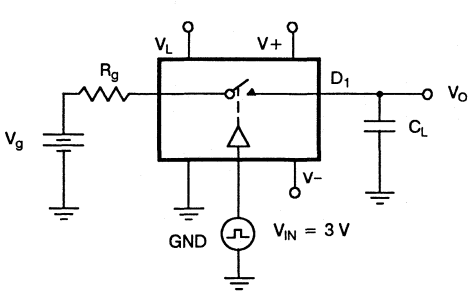


Repeat test for Channels 2, 3, and 4.

For load conditions, See Specifications
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Time



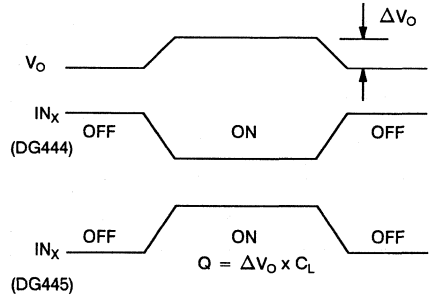


Figure 2. Charge Injection

TEST CIRCUITS (Cont'd)

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

C = 1 µF tantalum in parallel with 0.01 µF ceramic

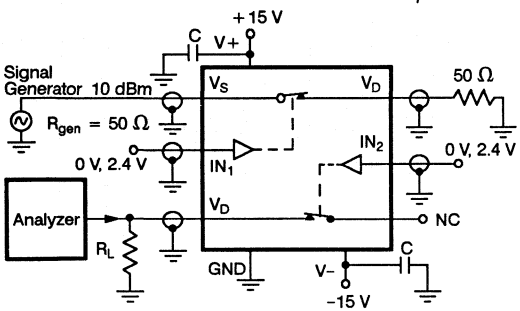


Figure 3. Crosstalk

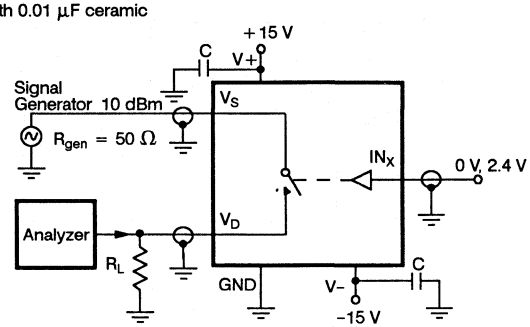


Figure 4. Off Isolation

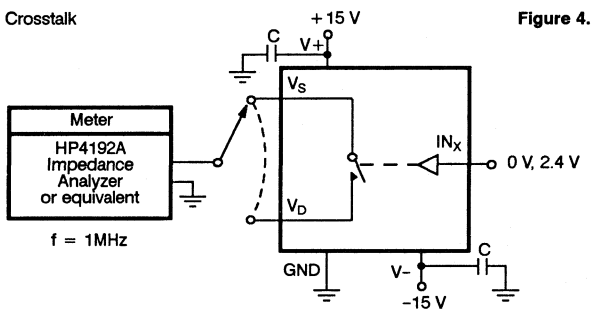


Figure 5. Source/Drain Capacitances

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

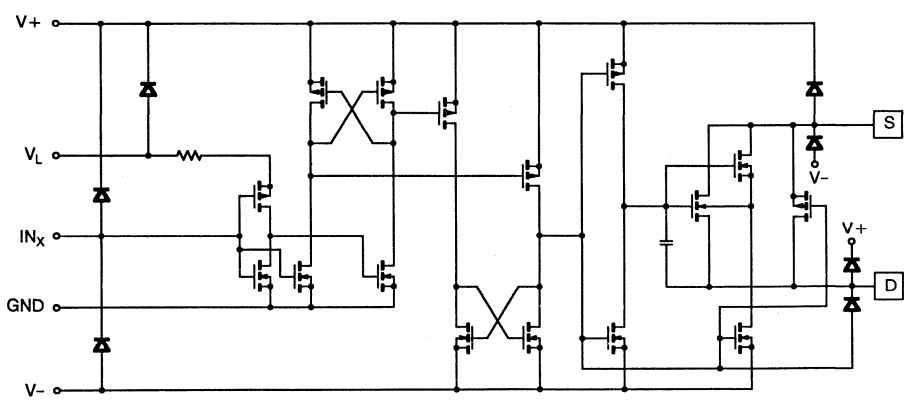
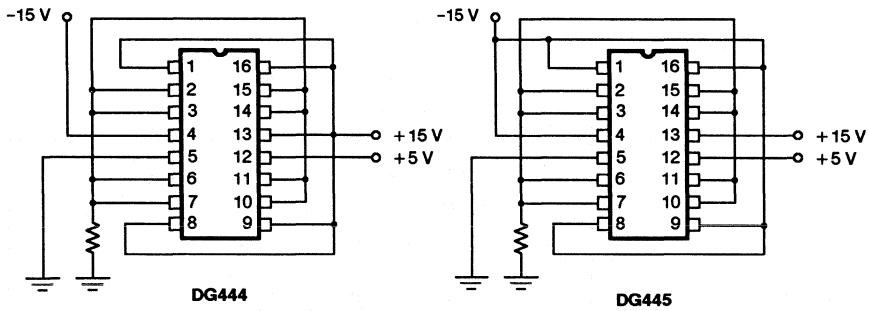


Figure 6.

BURN-IN CIRCUIT



Note: All resistors are 10 kΩ unless otherwise specified

Figure 7.

APPLICATIONS

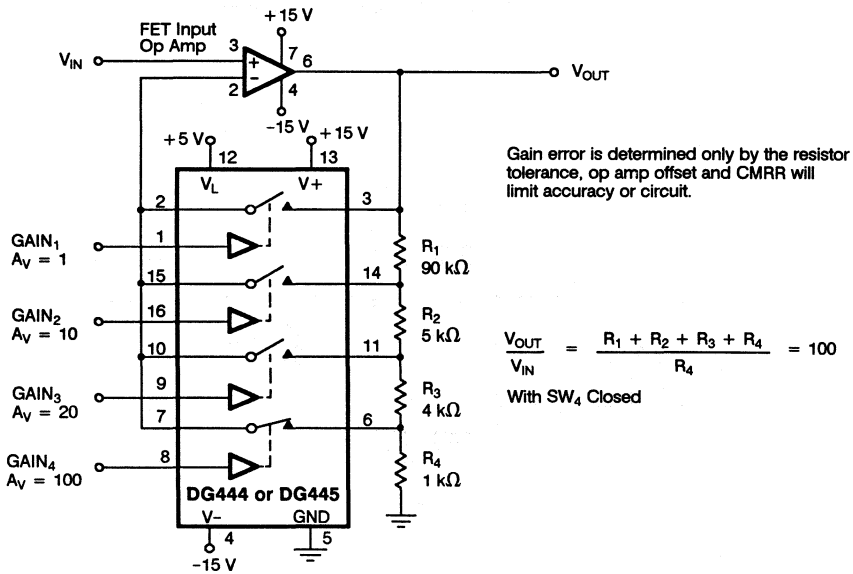


Figure 8. Precision-Weighted Resistor Programmable-Gain Amplifier

5

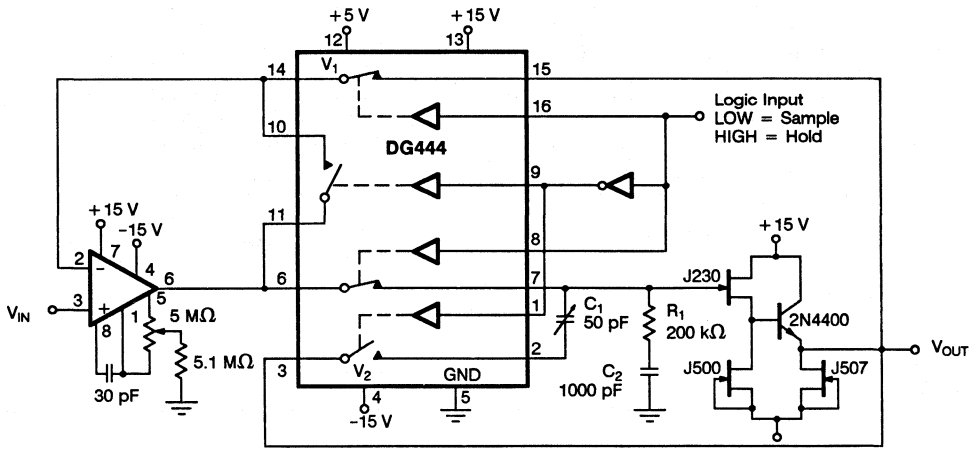


Figure 9. Precision Sample-and-Hold

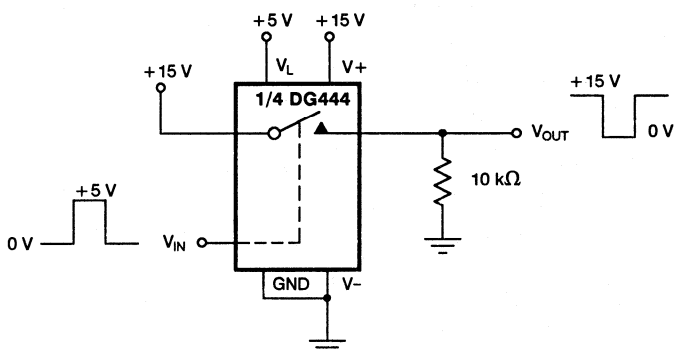


Figure 10. Level Shifter

Siliconix incorporated

DG458/459

8-Channel and Dual 4-Channel Fault Protected CMOS Analog Multiplexers

FEATURES

- Fault and Overvoltage Protection
- Fail Safe with Power Loss (No Latchup)
- Break-Before-Make Switching
- TTL and CMOS Compatible Inputs
- All Channels OFF When Power OFF for Signals Up to ±35 V

BENEFITS

- Improved Ruggedness
- Power Loss Protected
- Prevents Adjacent Channel Crosstalk
- Standard Logic Interface

APPLICATIONS

- Data Acquisition Systems
- Industrial Process Control
- Avionics Test Equipment
- High Rel Control Systems

DESCRIPTION

The DG458 and DG459 are 8- and 4-channel multiplexers, respectively, incorporating fault protection. A series n-channel/p-channel/n-channel MOSFET structure provides device and signal-source protection in the event of power loss or overvoltages. Under fault conditions the multiplexer input (or output) appears as an open circuit and only a few nanoamperes of leakage current will flow. This protects not only the multiplexer and the circuitry following it, but also protects the sensors or signal sources which drive the multiplexer.

The DG458 and DG459 multiplexers can withstand continuous overvoltage inputs up to ±35 V. All digital inputs have TTL compatible logic thresholds. Break-before-make operation prevents channel-to-channel interference.

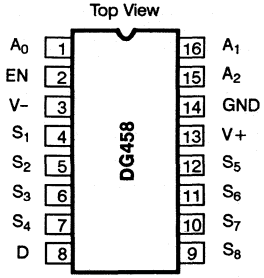
The DG458 and DG459 are pin compatible with the industry-standard DG508A and DG509A multiplexers.

The DG458/459 are offered in 16-pin plastic and CerDIP packages for operation over the extended industrial, D suffix (–40 to 85°C) and military, A suffix (–55 to 125°C) temperature ranges.

5

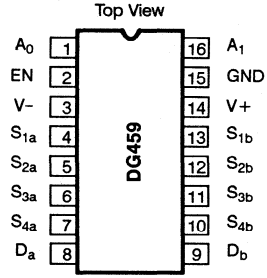
PIN CONFIGURATION

Dual-In-Line Package
Top View



Order Numbers:
CerDIP: DG458AK
Plastic: DG458DJ

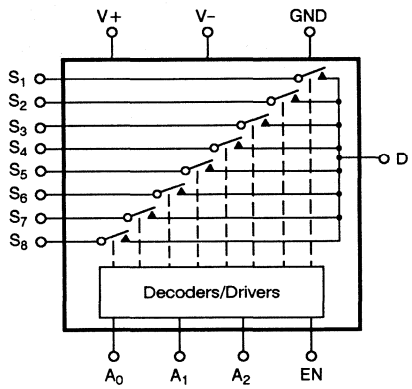
Dual-In-Line Package
Top View



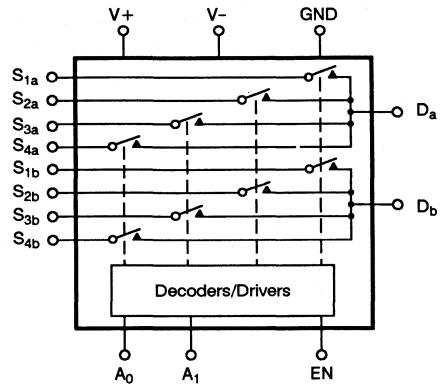
Order Numbers:
CerDIP: DG459AK
Plastic: DG459DJ

Siliconix incorporated

FUNCTIONAL BLOCK DIAGRAM



DG458
8-Channel Single Ended Multiplexer



DG459
Differential 4-Channel Multiplexer

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... 44 V
V+ to GND ..... 22 V
V- to GND ..... -25 V
V_{EN}, V_A Digital Input ..... (V-) -4 V to (V+) +4 V
V_S, Analog Input Overvoltage with Power ON
(V-) -20 V to (V+) +20 V
V_S, Analog Input Overvoltage with Power OFF ... -35 V to +35 V
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Power Dissipation (Package)*
16-Pin Ceramic DIP** ..... 1000 mW
16-Pin Plastic DIP*** ..... 600 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.3 mW/°C above 25°C.

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V		TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[f]		V_{ANALOG}			Full		-10	10	-10	10	V
Drain-Source ON-Resistance[g]		$r_{DS(ON)}$	V_D = ±9.5 V, I_D = -0.1 mA		Room Full	1.2		1.5 1.8		1.8 2.0	kΩ
			V_D = ±5 V, I_D = -0.1 mA		Room	200		500		500	Ω
$r_{DS(ON)}$ Matching Between Channels[h]		$\Delta r_{DS(ON)}$	V_S = 0 V, I_D = -0.1 mA		Room	6					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V V_D = ∓10 V	Room Full	0.03	-0.5 -50	0.5 50	-1 -50	1 50	nA
Drain OFF Leakage Current	DG458	$I_{D(OFF)}$		V_D = ±10 V V_S = ∓10 V	Room Full	0.1	-1 -200	1 200	-1 -200	1 200	
	DG459			V_D = ±10 V V_S = ∓10 V	Room Full	0.1	-1 -100	1 100	-2 -100	2 100	

Preliminary

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Differential OFF Drain Leakage Current		I_{DIFF}	DG459 Only	Full		-50	50	-50	50	nA
Drain ON Leakage Current	DG458	$I_{D(ON)}$	V_S = V_D = ±10 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	Room Full	0.1	-2 -200	2 200	-5 -200	5 200	
	DG459		Sequence Each Swtich ON	Room Full	0.05	-2 -100	2 100	-5 -100	5 100	
FAULT										
Output Leakage Current (with Overvoltage)		$I_{D(OFF)}$	V_S = ±33 V, V_D = 0 V (See Figure 1)	Room Full	4	-2000	2000	-2000	2000	nA
Input Leakage Current (with Overvoltage)		$I_{S(OFF)}$	V_S = ±25 V, V_D = ±10 V, (See Figure 1)	Room	1	-5	5	-10	10	µA
Input Leakage Current (with Power Supplies OFF)			V_S = ±25 V, V_{SUPS} = 0 V V_D = A_0, A_1, A_2, EN = 0 V	Room	1	-2	2	-5	5	
DIGITAL CONTROL										
Input LOW Threshold		V_{AL}		Full			0.8		0.8	V
Input LOW Threshold		V_{AL}		Full		2.4		2.4		
Logic Input Control		I_A	V_A = 2.4 V or 0.8 V	Full		-1	1	-1	1	µA
DYNAMIC CHARACTERISTICS										
Transition Time		t_A	See Figure 2	Room	200		500		500	ns
Break-Before-Make Time		t_{BBM}	See Figure 3	Room	30	10		10		
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 4	Room Full	200		250 500		250 500	
Enable Turn-OFF Time		$t_{OFF(EN)}$		Room Full	150		250 500		250 500	
Settling Time		t_s	To 0.1 %	Room	1.2					µs
			To 0.01%	Room	3.5					
OFF Isolation			V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 3 V_{RMS} f = 100 kHz	Room	68					dB
Logic Input Capacitance		C_{in}	f = 1 MHz	Room	5					pF
Source OFF Capacitance		$C_{S(OFF)}$		Room	5					
Drain OFF Capacitance	DG458	$C_{D(OFF)}$		Room	25					
	DG459			Room	12					
Drain ON Capacitance	DG458	$C_{D(ON)}$		Room	40					
	DG459			Room	35					

5

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V	TEMP[e]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	V_{EN} = HIGH or LOW	Room	0.05		0.1		0.1	mA
			Full			0.2		0.2	
Negative Supply Current	I-	V_A = 0 V	Room	-0.01	-0.1		-0.1		
			Full		-0.2		-0.2		
Power Supply Range for Continuous Operation			Room		±4.5	±18	±4.5	±18	V

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Room = 25°C, Full = as determined by the operating temperature suffix.
f. When the analog signal exceeds the +13.5 V or -12 V $r_{DS(ON)}$ starts to rise until only leakage currents flow.
g. Electrical Characteristics such as $r_{DS(ON)}$ change when supplies other than ±15 V are used.
h. $\Delta r_{DS(ON)} = \dfrac{r_{DS(ON)}MAX - r_{DS(ON)}MIN}{\Delta r_{DS(ON)}AVE}$

TEST CIRCUITS

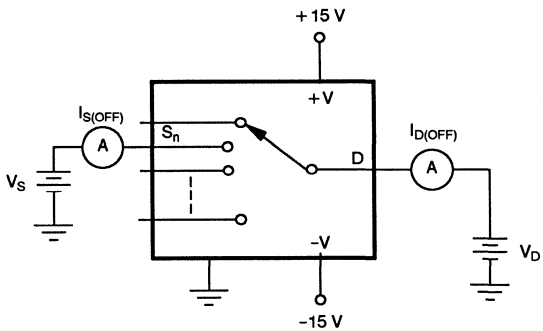
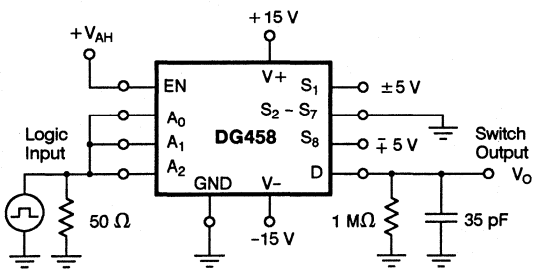


Figure 1. Analog Input Overvoltage



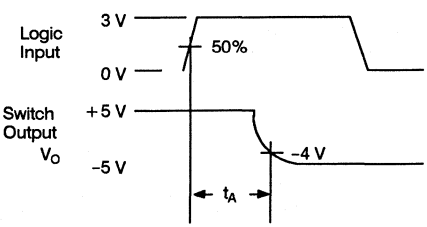
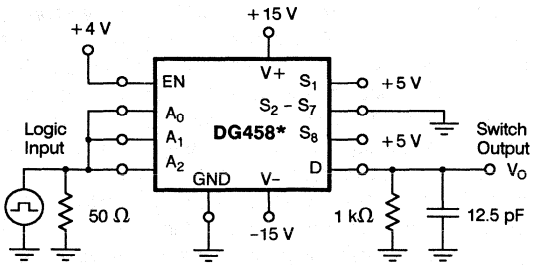


Figure 2. Transition Time

TEST CIRCUITS (Cont'd)



*Similar Connection for DG459

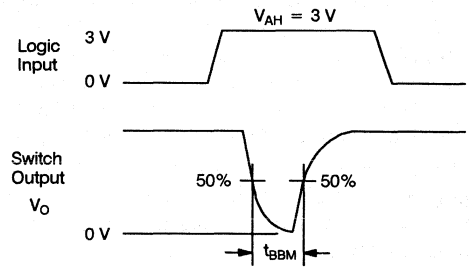
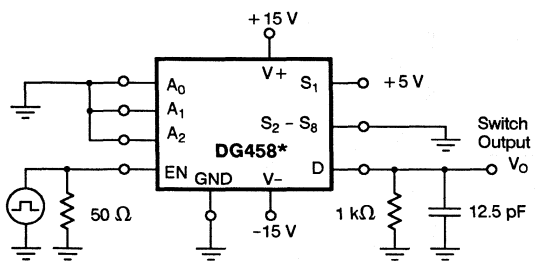


Figure 3. Break-Before-Make Time



*Similar Connection for DG459

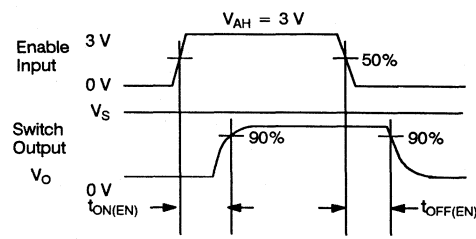


Figure 4. Enable Delay

5

TRUTH TABLES

DG458

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG459

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

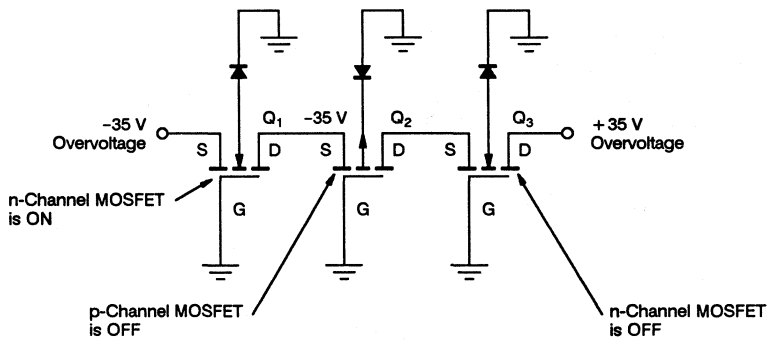
Logic "0" $V_{AL} \leq 0.8$ V, Logic "1" $V_{AH} \geq 2.4$ V

DETAILED DESCRIPTION

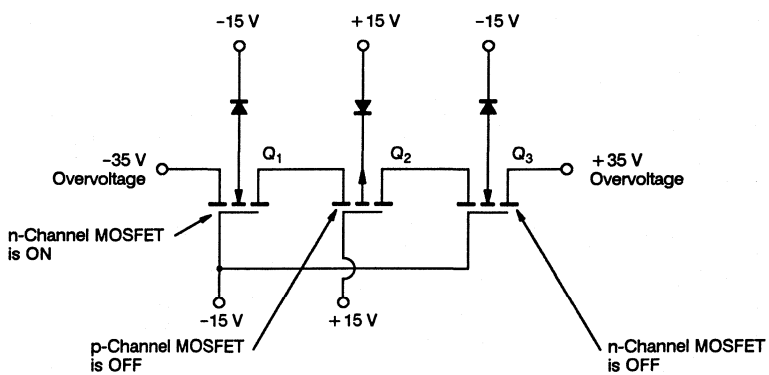
The Siliconix DG458/459 multiplexers are fully fault- and overvoltage-protected for continuous input voltages up to ±35 V whether or not voltage is applied to the power supply pins (V+, V–). These multiplexers are built on a high-voltage junction-isolated silicon-gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 5).

Within the normal analog signal range (±10 V), the $r_{DS(ON)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel n-mos and p-mos switches..

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut-off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



(a) Overvoltage with Mux Power OFF



(b) Overvoltage with Mux Power ON

Figure 5. Overvoltage Protection

Siliconix incorporated

DG485
Low-Power CMOS Octal Analog Switch Array

FEATURES

- ±15 Volt Input Range
- ON-Resistance <85 Ω
- Serial Data Input/Output
- Low-Power (P_D <105 μW)
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- ESD Protection > ±4000 V

BENEFITS

- Devices Can Be Chained for System Expansion
- Reduced Control Wires
- Reduced Board Space
- Low Signal Distortion
- Reduced Switch Errors
- Reduced Power Supply
- Simple Interfacing
- Improved Reliability

APPLICATIONS

- Audio Switching and Routing
- Audio Teleconferencing
- Serial Data Acquisition and Process Control
- Battery and Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Node Amplifiers

DESCRIPTION

The DG485 is an analog switch array that may be used as a low power 8-channel multiplexer for use in serial control applications. Any, all or none of the 8 switches may be closed at any given time. Combining low ON-resistance ($r_{DS(ON)}$ <85 Ω) and fast switching (t_{ON} <200 ns), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

The control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in via LD at any point into an octal latch which in turn controls all switches. $\overline{RS}$ resets the shift register, forcing all latch inputs to a LOW condition. The serial input (D_{IN}) and serial output (D_{OUT}) allow chaining of arrays for large systems.

Built on the Siliconix high voltage silicon gate process the DG485 has a wide 44 V range. An epitaxial layer prevents latchup.

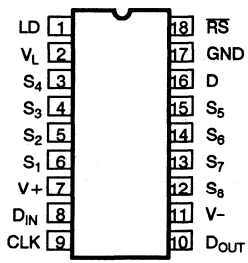
Each channel conducts equally well in either direction when ON and blocks up to 30 volts peak-to-peak when OFF.

Packaging for the DG485 consists of the 18-pin CerDIP, plastic DIP and 20-pin PLCC for surface mount. Temperature ranges available are military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C).

5

PIN CONFIGURATIONS

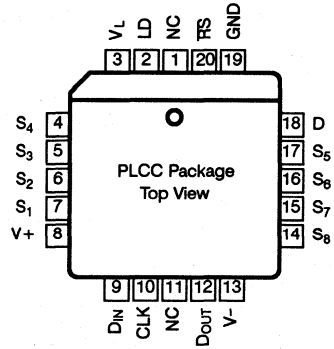
Dual-In-Line Package



Top View

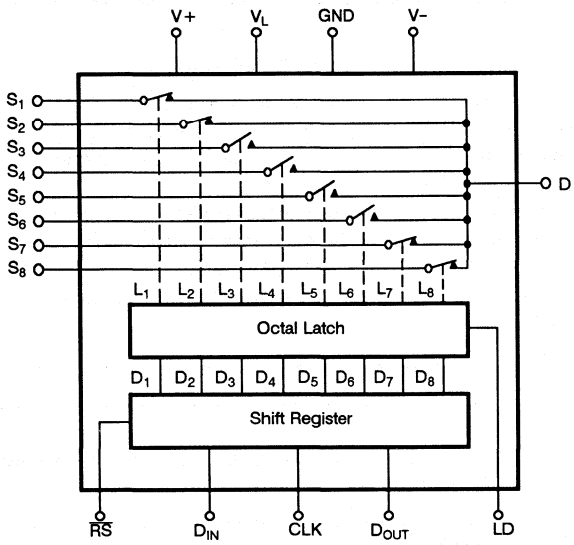
Order Numbers:

CerDIP: DG485AK, DG485AK/883
Plastic: DG485DJ



Order Number:
DG485DN

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLES



$\overline{RS}$	CLK	D_{IN}	D_1	D_N
1	↑	0	0	D_{N-1}
1	↑	1	1	D_{N-1}
1	↓	X	D_1	D_N (No Change)
0	X	X	0	0

The CLK input is edge triggered

LD	D_N	L_N	SW_N
↑	0	0	OFF
↑	1	1	ON
↓	D_n	L_n	(No Change)

The LD input is level triggered

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ ..... 44 V

GND ..... 25 V

Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+) + 2 V
or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Current, S or D (Pulsed 1 ms, 10% duty cycle) ..... 100 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*

18-Pin CerDIP** ..... 600 mW

18-Pin Plastic DIP*** ..... 470 mW

20-Pin PLCC**** ..... 450 mW

*All leads welded or soldered to PC Board.

**Derate 9.2 mW/°C above 75°C.

***Derate 16.5 mW/°C above 25°C.

****Derate 6 mW/°C above 75°C.

1 Signals on S_x, D_x, or IN_x exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		-15	15	-15	15	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V+ = 13.5 V, V- = -13.5 V I_S = -5 mA, V_D = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source ON-Resistance	$\Delta r_{DS(ON)}$	For each V_D: $\Delta r_{DS(ON)} = \frac{r_{DS(ON)\,MAX} - r_{DS(ON)\,MIN}}{r_{DS(ON)AVG}}$	Room	6		10		10	%

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)									
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 16.5 V, V- = -16.5 V	Room Hot	0.01	-1 -20	1 20	-1 -20	1 20	nA
	$I_{D(OFF)}$	V_D = -15.5 V, V_S = 15.5 V V_D = 15.5 V, V_S = -15.5 V	Room Hot	0.1	-10 -200	10 200	-10 -200	10 200	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V± = ±16.5 V V_S = V_D = ±15.5 V One Switch At A Time	Room Hot	0.11	-20 -500	20 500	-20 -500	20 500	
		V± = ±16.5 V V_S = V_D = ±15.5 V All Switches ON	Room	0.20					
INPUT									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Room Hot	-0.00001	-1 -5	1 5	-1 -5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Room Hot	0.00001	-1 -5	1 5	-1 -5	1 5	
SERIAL DATA OUTPUT									
Output Voltage with V_{IN} Low - D_{OUT}	V_{OL}	I_O = 1.6 mA, V+ = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V_{IN} High - D_{OUT}	V_{OH}	I_O = -80 µA, V+ = 16.5 V V_L = 4.75 V	Full	4.4	2.7		2.7		
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	See Figures 1, 4 V_S = ±10 V	Room Hot	170		200 275		200 275	ns
Turn-OFF Time	t_{OFF}	See Figures 1, 5, 6 V_S = ±10 V	Room Hot	150		200 275		200 276	
Data Setup Time	t_{DS}	See Figures 1, 7	Room Hot		40 60		40 60		
Data Hold Time	t_{DH}		Room Hot		40 60		40 60		
LOAD Hold Time	t_{LH}	See Figures 1, 8	Room Hot		100 150		100 150		
$\overline{\text{RESET}}$ Hold Time	t_{RH}		Room Hot		100 150		100 150		
$\overline{\text{RESET}}$ ↑ to $\overline{\text{CLOCK}}$ ↑ Delay	t_{DRC}		Room Hot		40 60		40 60		
Charge Injection	Q	Any One Channel V_S = 0 V, C_L = 1,000 pF	Room	17					pC
OFF Isolation[c]		R_L = 50 Ω, C_L = 5 pF f = 1 MHz, See Figure 2	Room	-75					dB

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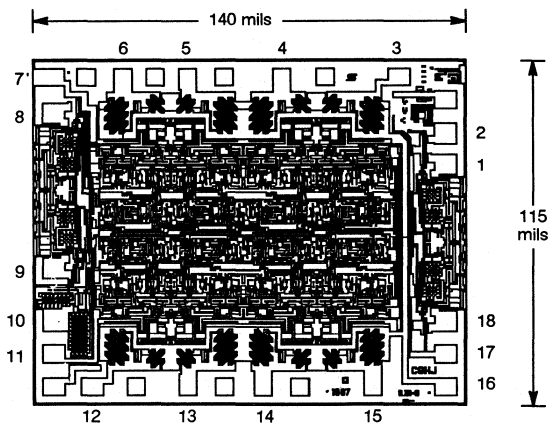
Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS									
Source OFF Capacitance[c]	$C_{S(OFF)}$	V_{gen} = 0 V, R_{gen} = 0 Ω	Room	7					pF
Drain OFF Capacitance[c]	$C_{D(OFF)}$	f = 1 MHz	Room	43					
On-State Capacitance[c]	$C_{S + D (ON)}$	V_{gen} = 0 V, R_{gen} = 0 Ω f = 1 MHz, One Channel ON	Room	53					
		V_{gen} = 0 V, R_{gen} = 0 Ω f = 1 MHz, All Channels ON	Room	122					
POWER SUPPLIES									
Positive Supply Curent	I+	V+ = 16.5 V, V- = -16.5 V V_{IN} = 0 or 5 V V_L = 5.25 V D_{OUT} Open	Room Full	0.001		3 10		3 10	µA
Negative Supply Current	I-		Room Full	-0.001	-3 -10		-3 -10		
Logic Supply Current	I_L		Room Full	0.001		3 10		3 10	
Ground Current	I_{GND}		Room Full	-0.001	-3 -10		-3 -10		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY

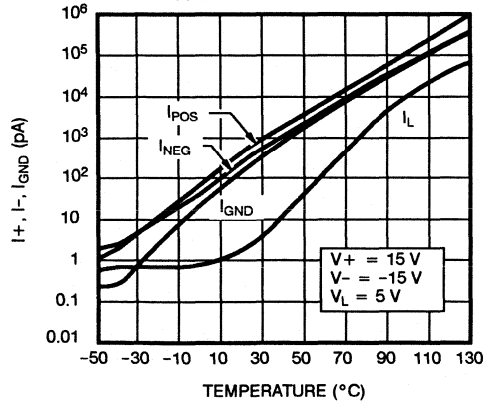


Pad No.	Function
1	LD
2	V_D
3	S_4
4	S_3
5	S_2
6	S_1
7	V+ (Substrate)
8	D_{IN}
9	CLK
10	D_{OUT}
11	V-
12	S_8
13	S_7
14	S_6
15	S_5
16	D
17	GND
18	$\overline{RS}$

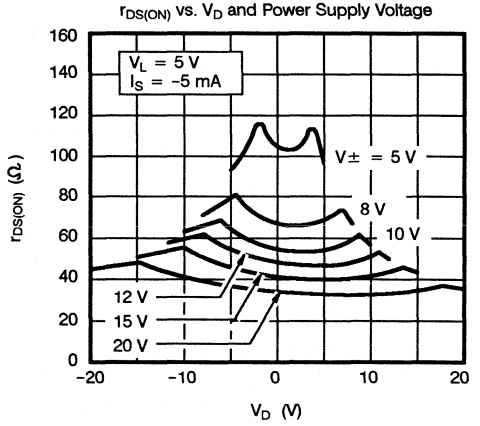
CSHJM
8 Diodes
4 Resistors
272 p-channel Enhancement MOSFET's
288 n-channel Enhancement MOSFET's

TYPICAL CHARACTERISTICS

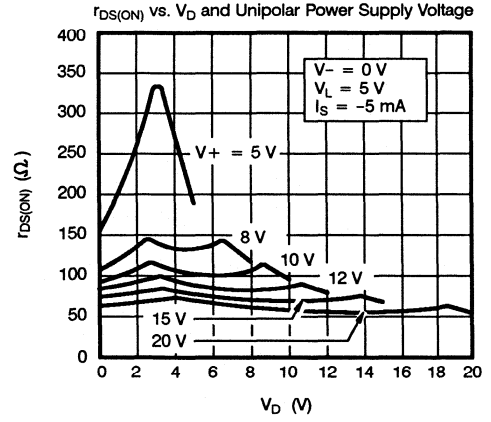
Supply Currents vs. Temperature



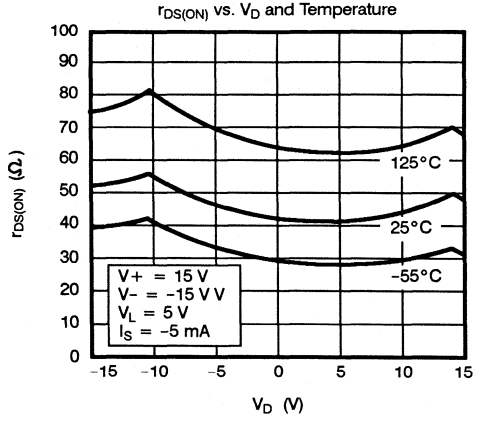
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



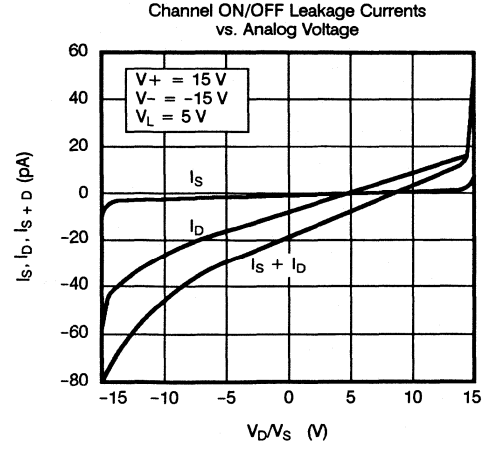
$r_{DS(ON)}$ vs. V_D and Unipolar Power Supply Voltage



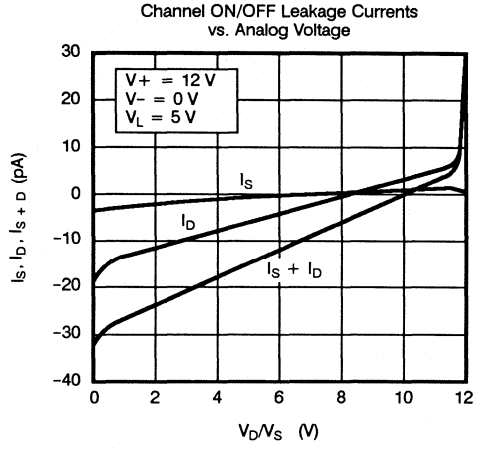
$r_{DS(ON)}$ vs. V_D and Temperature



Channel ON/OFF Leakage Currents vs. Analog Voltage



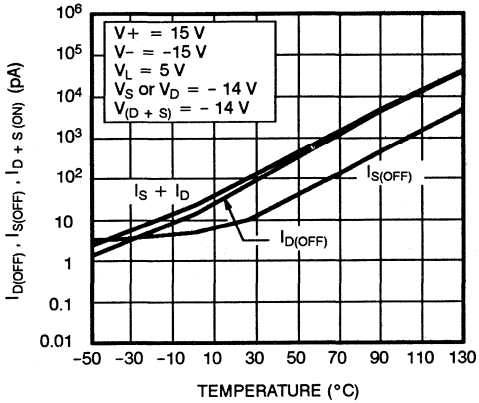
Channel ON/OFF Leakage Currents vs. Analog Voltage



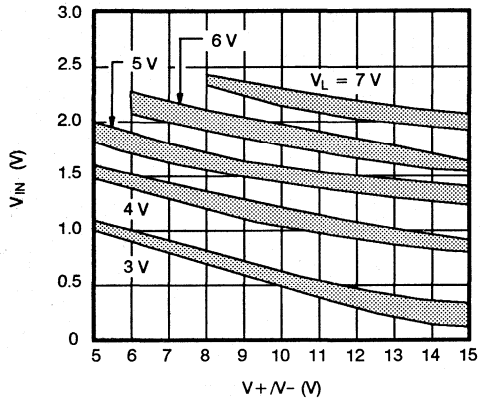
5

TYPICAL CHARACTERISTICS (Cont'd)

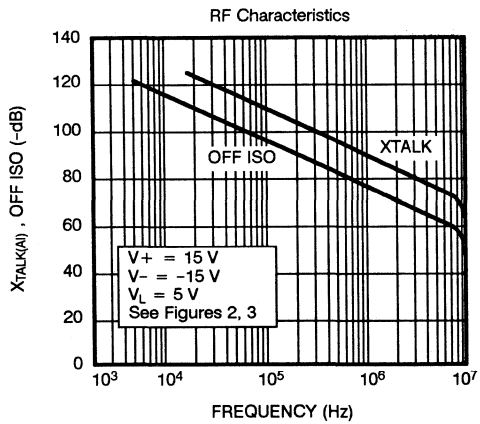
Channel ON/OFF Leakage Currents vs. Temperature



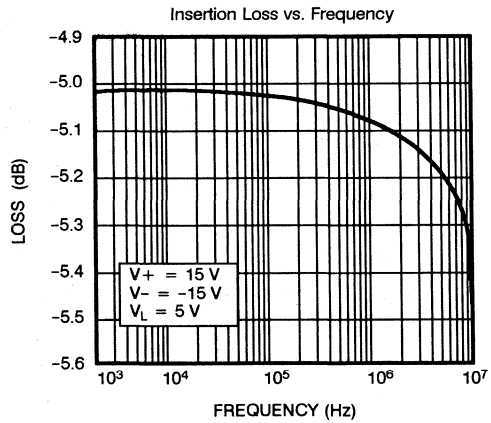
SwitchingThreshold vs. Power Supply Voltage and V_L



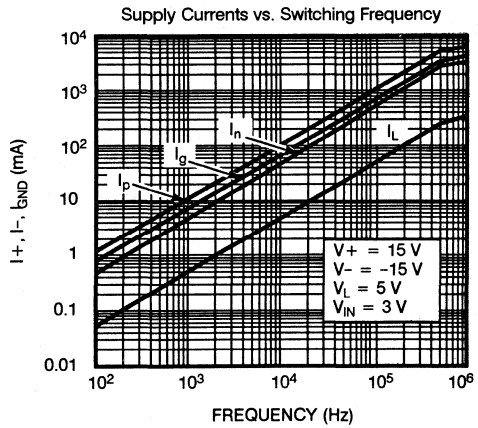
RF Characteristics



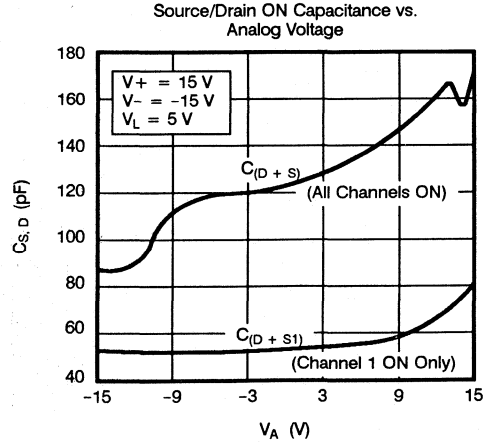
Insertion Loss vs. Frequency



Supply Currents vs. Switching Frequency

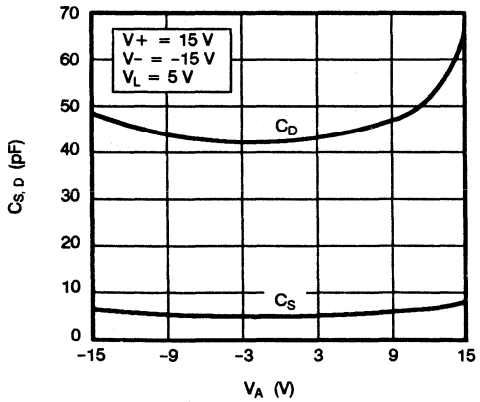


Source/Drain ON Capacitance vs. Analog Voltage

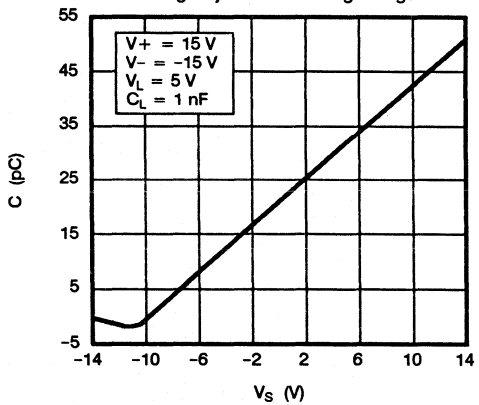


TYPICAL CHARACTERISTICS (Cont'd)

Source/Drain OFF Capacitance vs. Analog Voltage



Charge Injection vs. Analog Voltage



TEST CIRCUITS

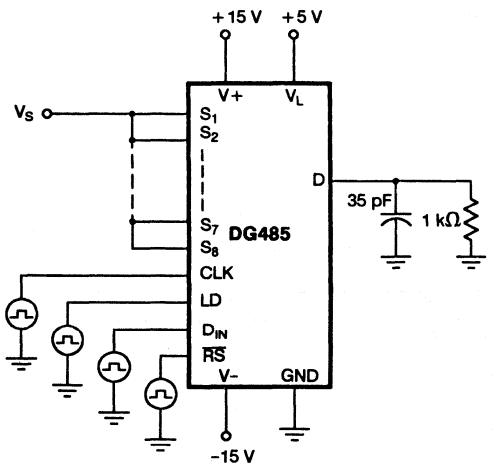


Figure 1. Switching Time Test Circuit

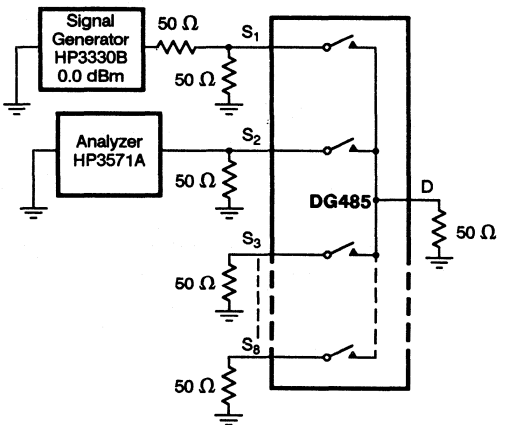


Figure 2. Adjacent Input Crosstalk

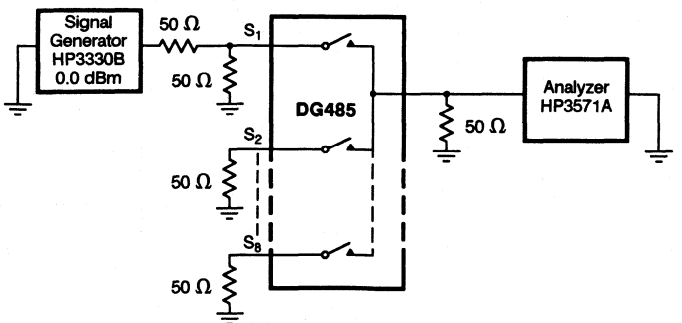


Figure 3. Off Isolation

5

TYPICAL INPUT TIMING REQUIREMENTS

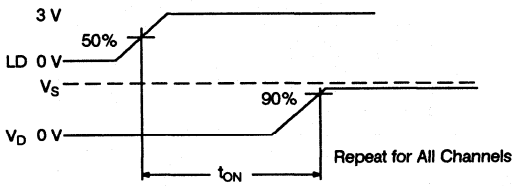


Figure 4. t_{ON} from LD

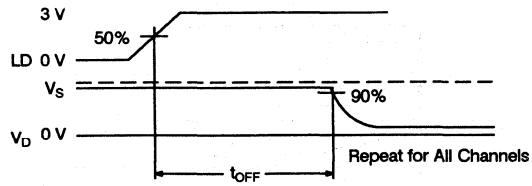


Figure 5. t_{OFF} from LD

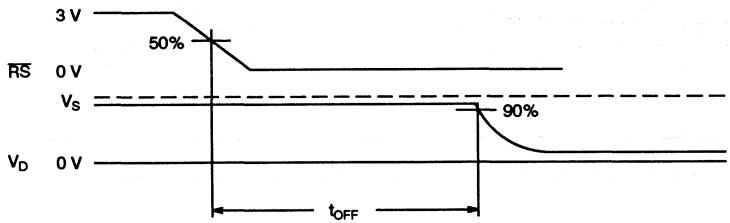


Figure 6. t_{OFF} from $\overline{RS}$

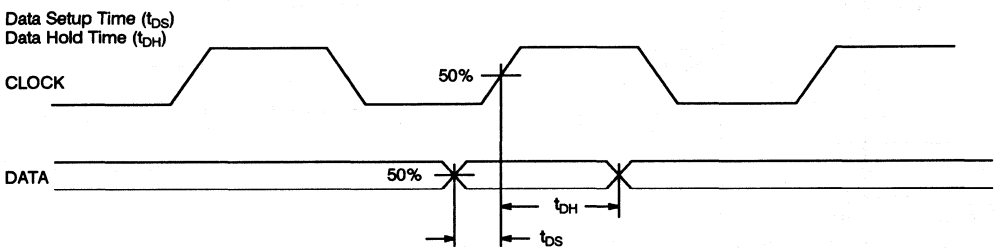


Figure 7.

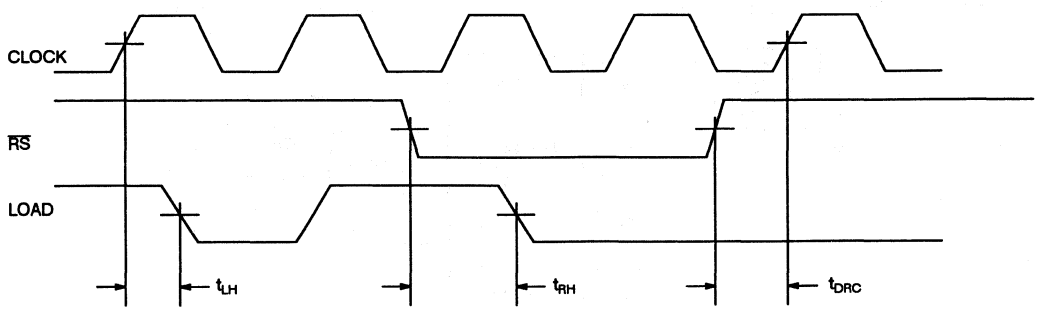
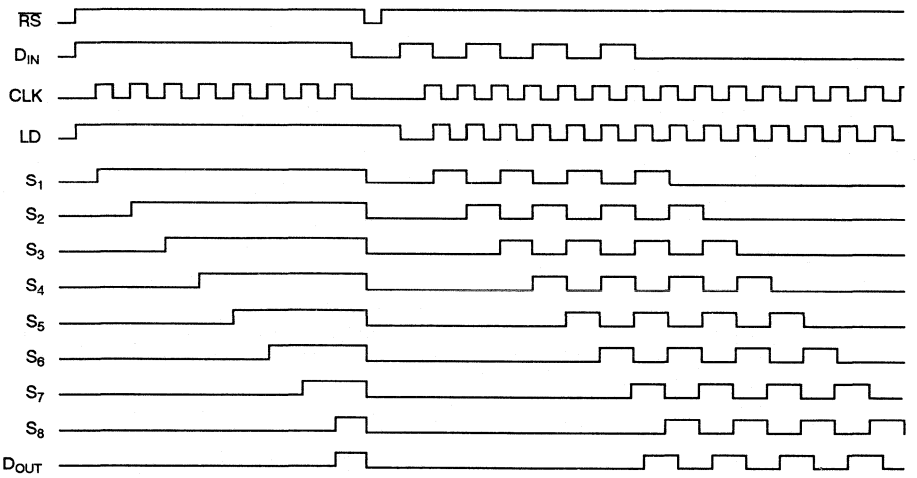


Figure 8. Timing Relationships

TIMING DIAGRAM



S_1 – S_8 and D_{OUT} are expected output with the drain connected high. The sources require pull-down of 1 kΩ.

Figure 9.

APPLICATIONS

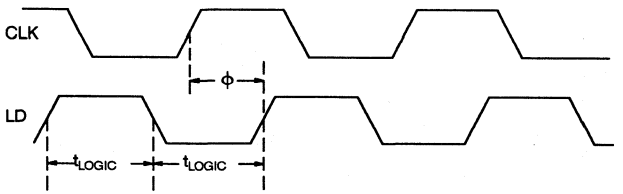


Figure 10.

ϕ = for CLK and LD inputs of the same frequency. The recommended phase delay of LD from CLK is ½ t_{LOGIC} to t_{LOGIC}:

$t_{LOGIC(MIN)}$: 80 ns at 25°C, 150 ns at 125°C

V+ = 15 V
V- = -15 V
GND = 0 V

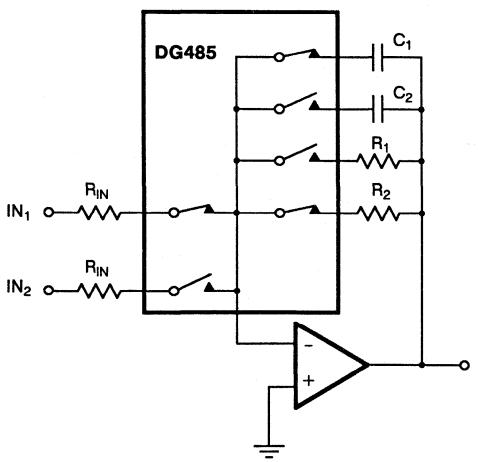


Figure 11. Multi-Function circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

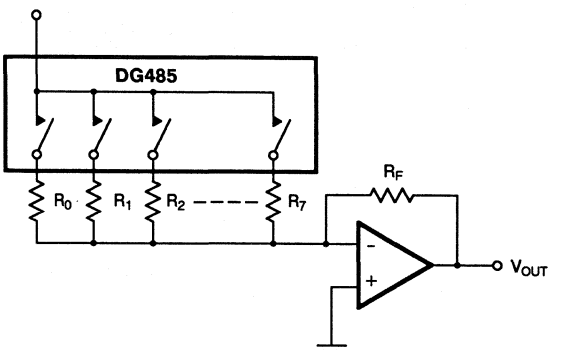


Figure 12. Non-Linear DAC Circuit

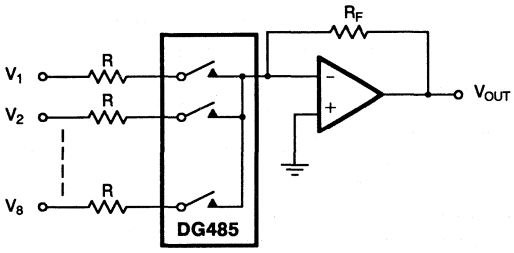


Figure 13. Summing Node Mixer

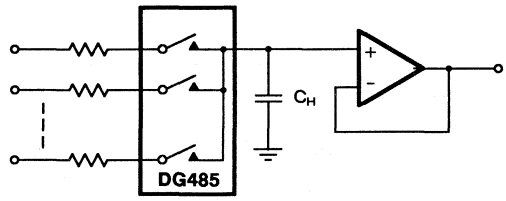


Figure 14. Multi-Channel Sampling and TDM Application

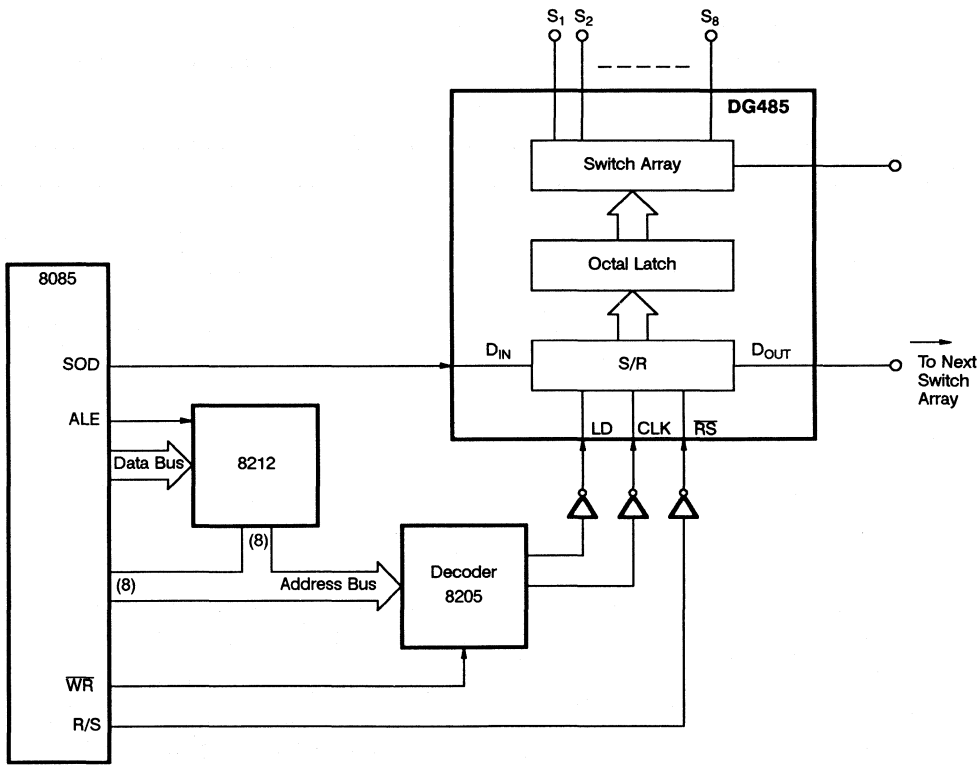


Figure 15. Direct Serial Interface (8085)

Siliconix incorporated

DG506A/507A
16-Channel and Dual 8-Channel CMOS Analog Multiplexers

FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- ESD Protection > ±2500 V
- 44 V Power Supply Rating

BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Crosstalk
- Environmentally Rugged

APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

DESCRIPTION

DG506A/507A are 16- and dual 8-channel analog multiplexers, respectively, designed for selecting 1 of 16 (or 8) analog input signals and connecting it to a common output or, conversely, routing an analog signal to 1 of 16 (or 8) output loads. Break-before-make switching action protects against momentary shorting of the input signals.

The DG506A, a 16-channel single-ended analog multiplexer, is designed to connect 1 of 16 inputs to a common output as determined by a 4-bit binary address (A_0, A_1, A_2, A_3). DG507A, a dual 8-channel analog multiplexer, is designed to connect 1 of 8 dual inputs to a common dual output as determined by its 3 bit binary address (A_0, A_1, A_2) logic.

A channel in the ON state conducts current equally well in both directions (bi-directional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address (A_X) and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

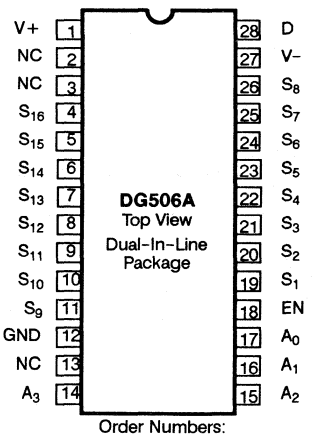
DG506A/507A are designed in the Siliconix PLUS-40 process, which includes improved ESD protection up to 2500 V for ruggedness. An epitaxial layer prevents latch up.

Both DG506A and DG507A are available in dual-in-line ceramic and plastic packages, and are specified for operation over the military, A suffix (-55 to 125°C), industrial, D suffix (-40 to 85°C), and commercial, C suffix (0 to 70°C), temperature ranges.

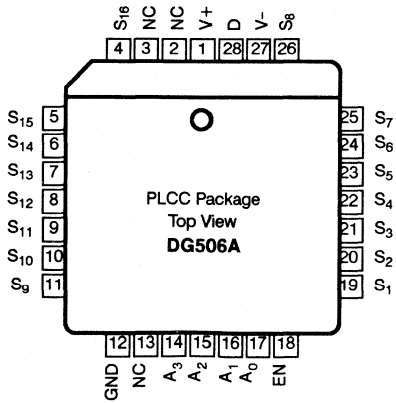
For applications requiring address data latching, the DG528/DG529 is recommended. For wideband/video routing and multiplexing applications, the DG536 is recommended.

5

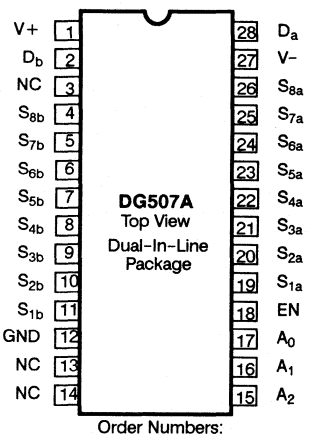
PIN CONFIGURATION



Order Numbers:
Side Braze: DG506ABR, DG506AAK/883
CerDIP: DG506AAK, DG506AAK/883
DG506ABK, DG506ACK
Plastic: DG506ACJ

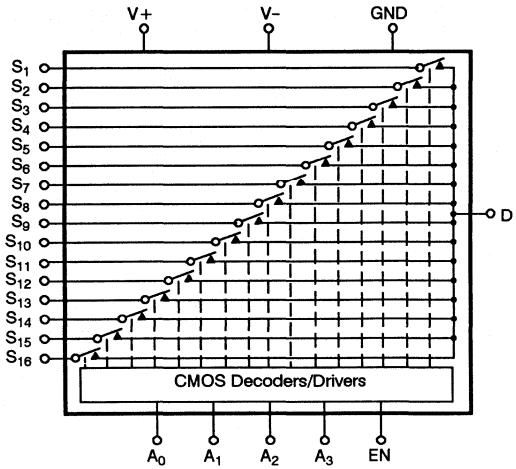


Order Number:
DG506ADN



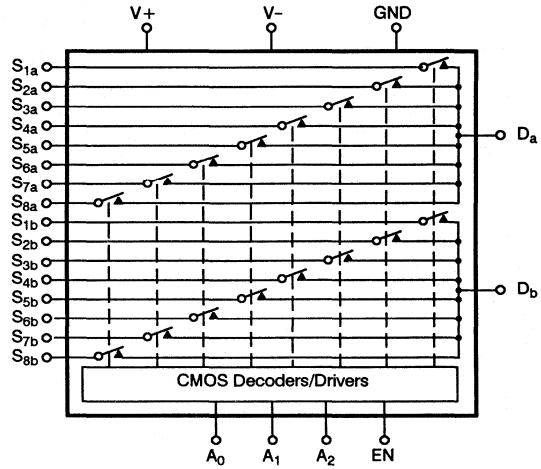
Order Numbers:
Side Braze: DG507ABR, DG507AAK/883
CerDIP: DG507AAK, DG507AAK/883
DG507ABK, DG507ACK
Plastic: DG507ACJ

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLES



DG506A
16-Channel Single Ended Multiplexer

A_3	A_2	A_1	A_0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16



DG507A
Differential 8-Channel Multiplexer

A_2	A_1	A_0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = $V_{AL} \leq 0.8$ V, Logic "1" = $V_{AH} \geq 2.4$ V

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or
..... 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak CURRENT, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C

Power Dissipation (Package)*
28-Pin Ceramic DIP** ..... 1200 mW
28-Pin Plastic DIP*** ..... 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 75°C.

SPECIFICATIONS[a]

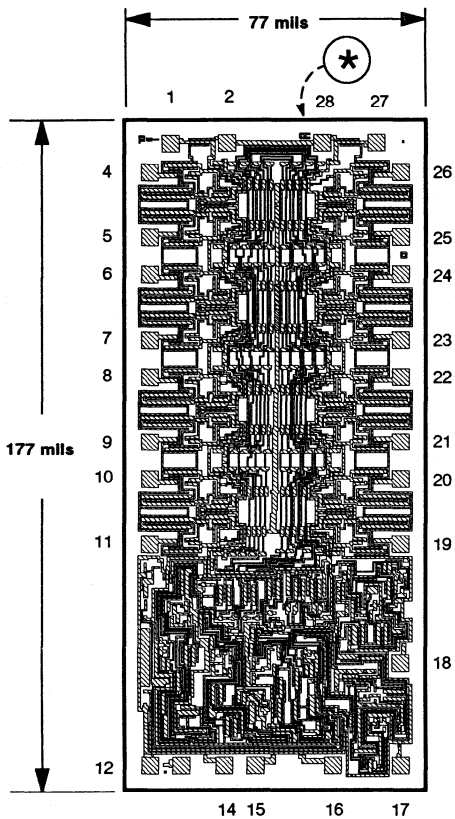
PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V		TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C SUFFIX MIN[b]	B, C SUFFIX MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	$V_D = \pm 10$ V, $V_{AL} = 0.8$ V $I_S = -200$ µA, $V_{AH} = 2.4$ V		Room Full			400 500		450 550	Ω
$r_{DS(ON)}$ Matching[f]		$\Delta r_{DS(ON)}$	-10 V < V_S < 10 V		Room	6					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	$V_S = \pm 10$ V $V_D = \mp 10$ V	Room Hot		-1 -50	1 50	-5 -50	5 50	µA
Drain OFF Leakage Current	DG506A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \pm 10$ V	Room Hot		-10 -300	10 300	-20 -300	20 300	µA
	DG507A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \pm 10$ V	Room Hot		-5 -200	5 200	-10 -200	10 200	µA
Drain ON[e, g] Leakage Current	DG506A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V $V_{AL} = 0.8$ V $V_{AH} = 2.4$ V		Room Hot		-10 -300	10 300	-20 -300	20 300	µA
	DG507A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V $V_{AL} = 0.8$ V $V_{AH} = 2.4$ V		Room Hot		-5 -200	5 200	-10 -200	10 200	µA
DIGITAL CONTROL											
Logic Input Current Input Voltage High		I_{AH}	V_A = 2.4 V		Room Hot		-10 -30		-10 -30		µA
		I_{AH}	V_A = 15 V		Room Hot			10 30		10 30	µA
Logic Input Current Input Voltage Low		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Hot		-10 -30		-10 -30		µA
DYNAMIC CHARACTERISTICS											
Transition Time		t_{TRANS}	See Figure 1		Room	0.6		1			µs
Break-Before-Make Time		t_{OPEN}	See Figure 3		Room	0.2					ns
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 2		Room	1					µs
Enable Turn-OFF Time		$t_{OFF(ON)}$	See Figure 2		Room	0.4					µs
Charge Injection		Q			Room	20					pC
OFF Isolation[l]			V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 7 V_{RMS} f = 500 kHz		Room	68					dB
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_S = 0 V	Room	6					pF
Drain OFF Capacitance	DG506A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	45					pF
	DG507A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	23					pF
POWER SUPPLIES											
Positive Supply Current		I+	V_{EN} = 0 V, V_A = 0 V		Room	1.3		2.4		2.4	mA
Negative Supply Current		I-	V_{EN} = 0 V, V_A = 0 V		Room	-0.7	-1.5		-1.5		mA

5

SPECIFICATIONS[a] (Cont'd)

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}MAX - r_{DS(ON)}MIN}{r_{DS(ON)}AVE} \right)$
g. $I_{D(ON)}$ is leakage from driver into "ON" switch.
h. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. OFF isolation = 20 log $\frac{V_D}{V_S}$, V_S = input to "OFF" switch, V_D = output due to V_S.
j. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



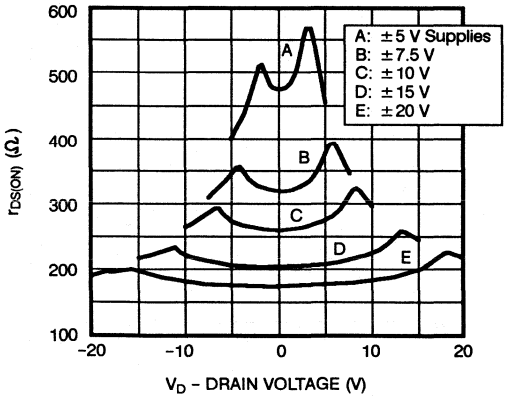
Pad No.	Function DG506A	Pad No.	Function DG507A
1	V+ (Substrate)	1	V+ (Substrate)
2	NC	2	D_b
3	NC	3	NC
4	S_{16}	4	S_{8b}
5	S_{15}	5	S_{7b}
6	S_{14}	6	S_{6b}
7	S_{13}	7	S_{5b}
8	S_{12}	8	S_{4b}
9	S_{11}	9	S_{3b}
10	S_{10}	10	S_{2b}
11	S_9	11	S_{1b}
12	GND	12	GND
13	NC	13	NC
14	A_3	14	NC
15	A_2	15	A_2
16	A_1	16	A_1
17	A_0	17	A_0
18	EN	18	EN
19	S_1	19	S_{1a}
20	S_2	20	S_{2a}
21	S_3	21	S_{3a}
22	S_4	22	S_{4a}
23	S_5	23	S_{5a}
24	S_6	24	S_{6a}
25	S_7	25	S_{7a}
26	S_8	26	S_{8a}
27	V-	27	V-
28	D	28	D_a

ICMHA-I ***A = DG506A**
5 Capacitors
152 p-channel enhancement MOSFETs
8 Resistors
169 n-channel enhancement MOSFETs

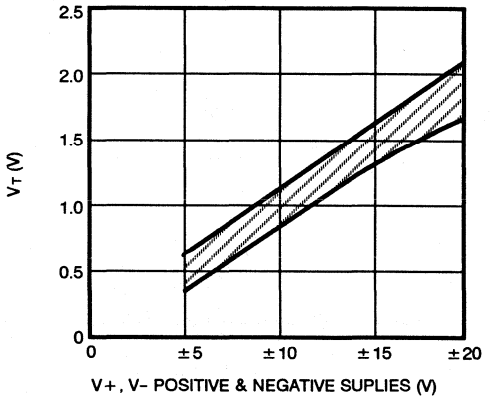
ICMHB-I ***B = DG507A**
4 Capacitors
141 p-channel enhancement MOSFETs
7 Resistors
160 n-channel enhancement MOSFETs

TYPICAL CHARACTERISTICS

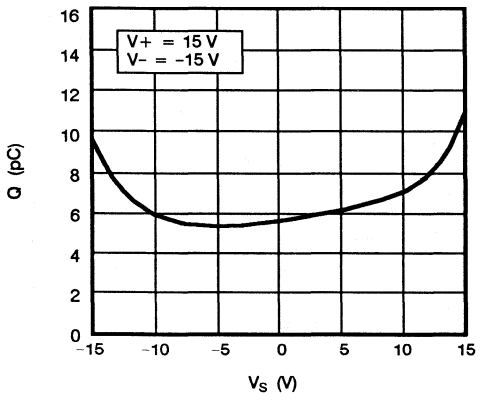
$r_{DS(ON)}$ vs. V_D and Power Supply



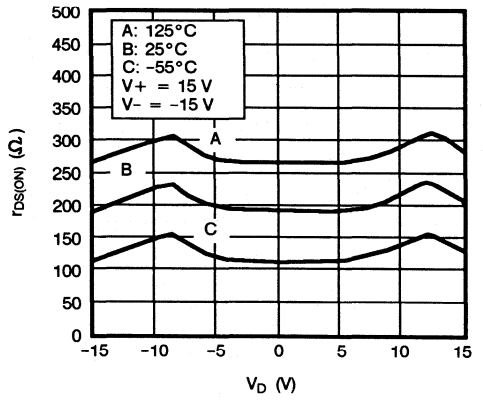
Input Switching Threshold vs. V+ and V- Supply Voltages



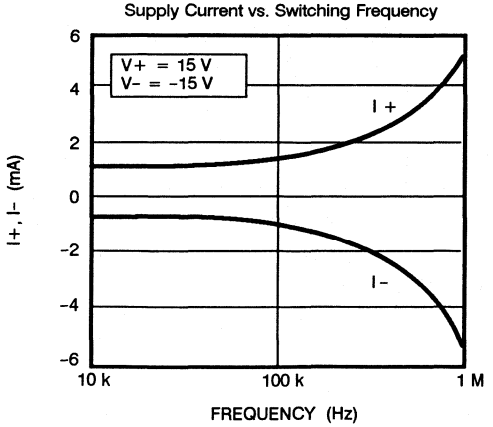
Charge Injection vs. Analog Voltage (V_S)



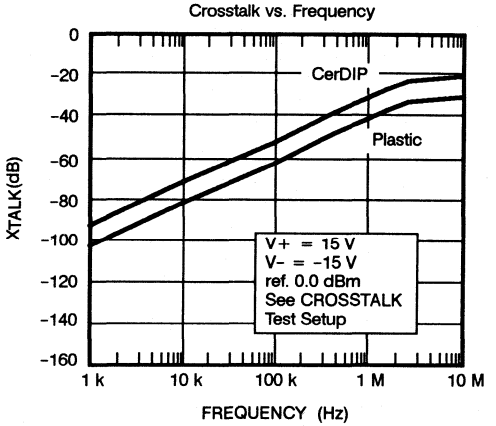
$r_{DS(ON)}$ vs. V_D and Temperature



Supply Current vs. Switching Frequency



Crosstalk vs. Frequency



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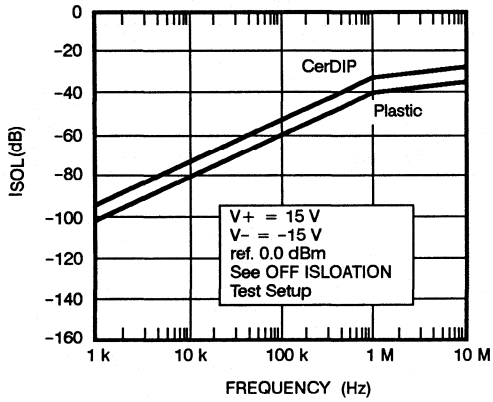
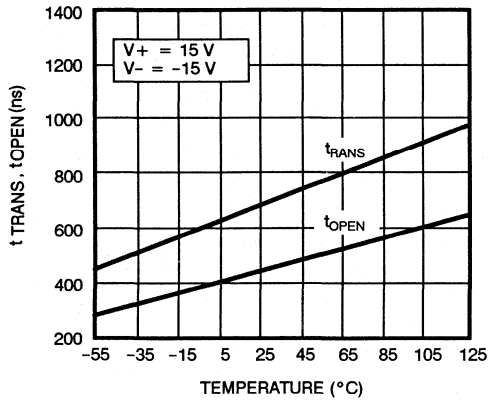
TYPICAL CHARACTERISTICS (Cont'd)

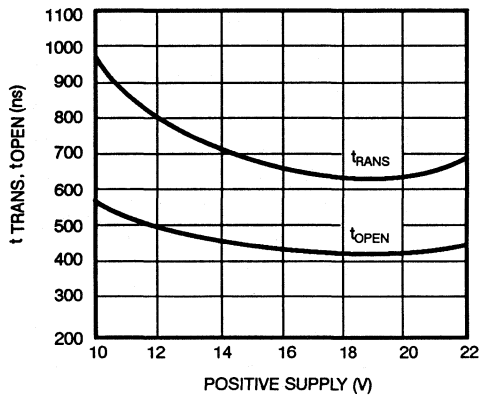
Off Isolation vs. Frequency



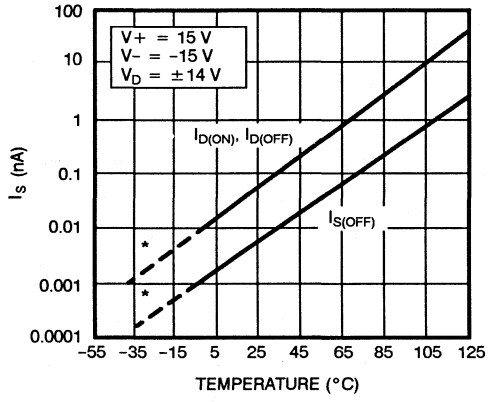
Switching Time vs. Temperature



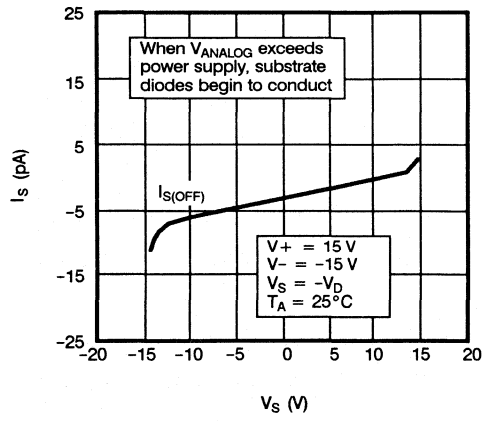
Switching Time vs. Positive Supply Voltage



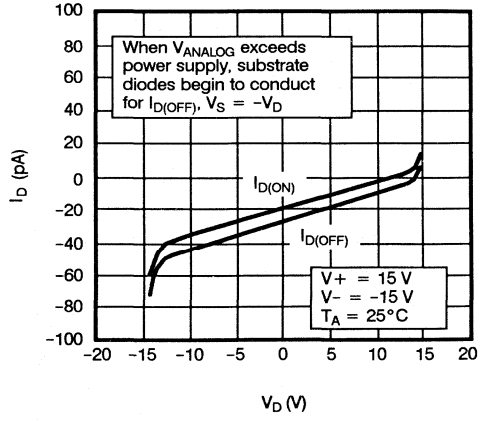
Leakages vs. Temperature



$I_{S(OFF)}$ vs. Analog Voltage

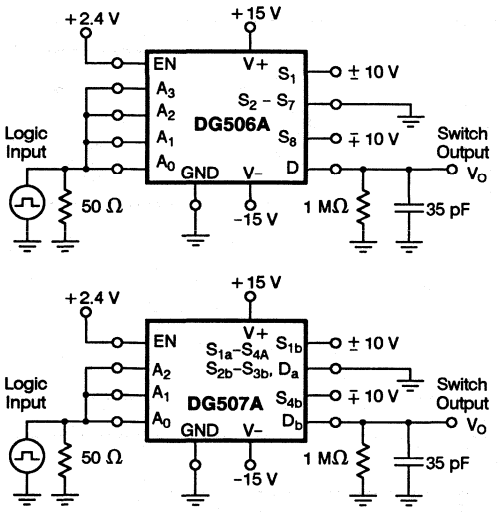


$I_{D(ON)}$, $I_{D(OFF)}$ vs. Analog Voltage



* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

TEST CIRCUITS



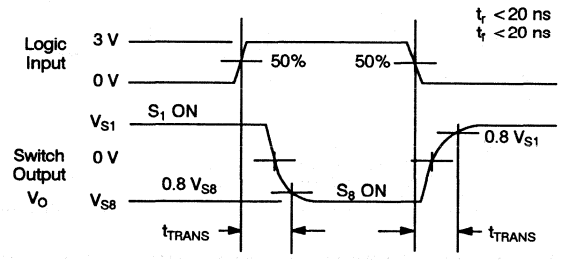
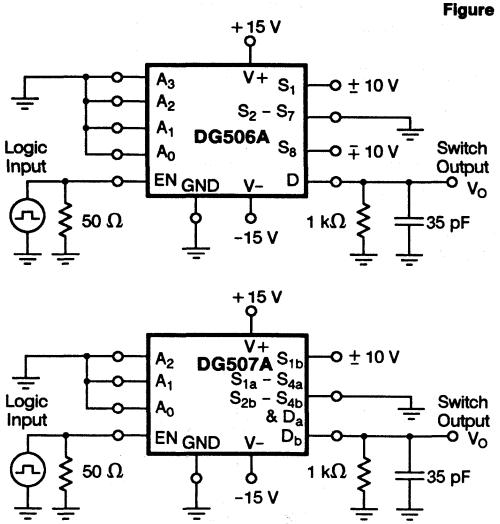


Figure 1. $t_{TRANSITION}$



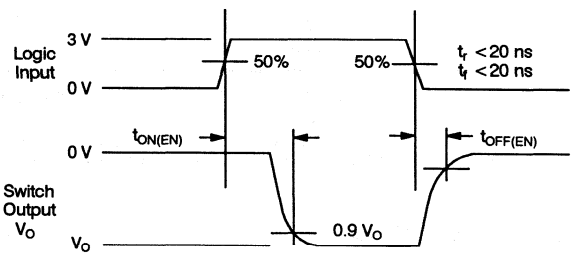
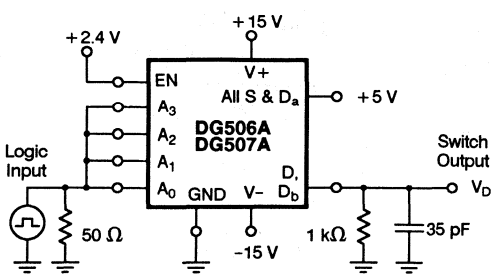


Figure 2. $t_{ON(EN)}$ and $t_{OFF(EN)}$



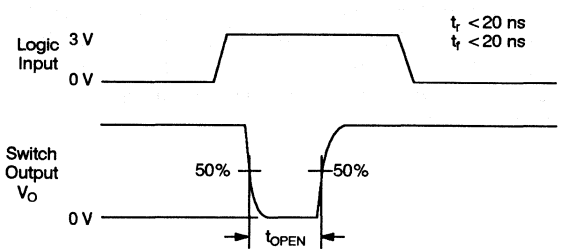


Figure 3. t_{OPEN}

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

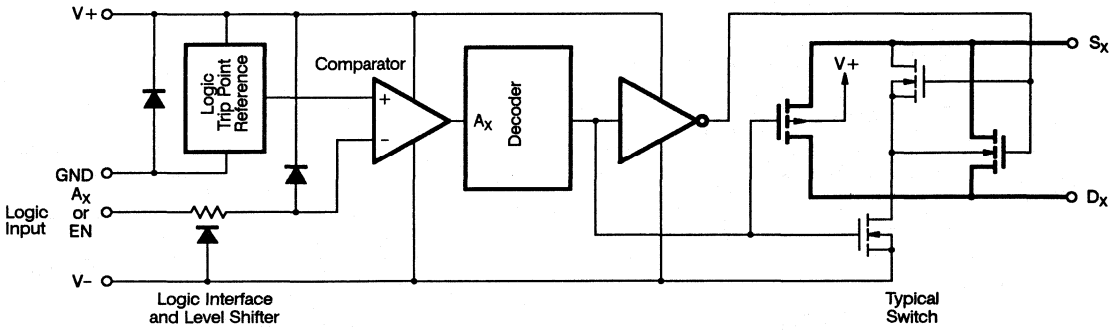


Figure 4.

APPLICATION HINTS*

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	Logic Input Voltage V_{INH} Min/V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.4/0.6	-10 to 10
8***	-8	2.4/0.4	-8 to 8

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Specifications chart based on V+ = +15 V, V- = -15 V.
*** Operation below ±8 V is not recommended due to the shift in $V_{INL(MAX)}$.

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 5). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V- rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

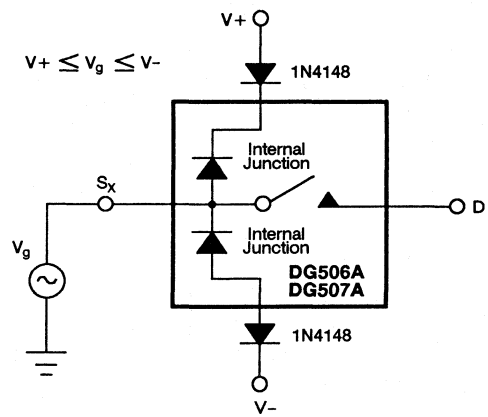


Figure 5. Overvoltage Protection Using Blocking Diodes

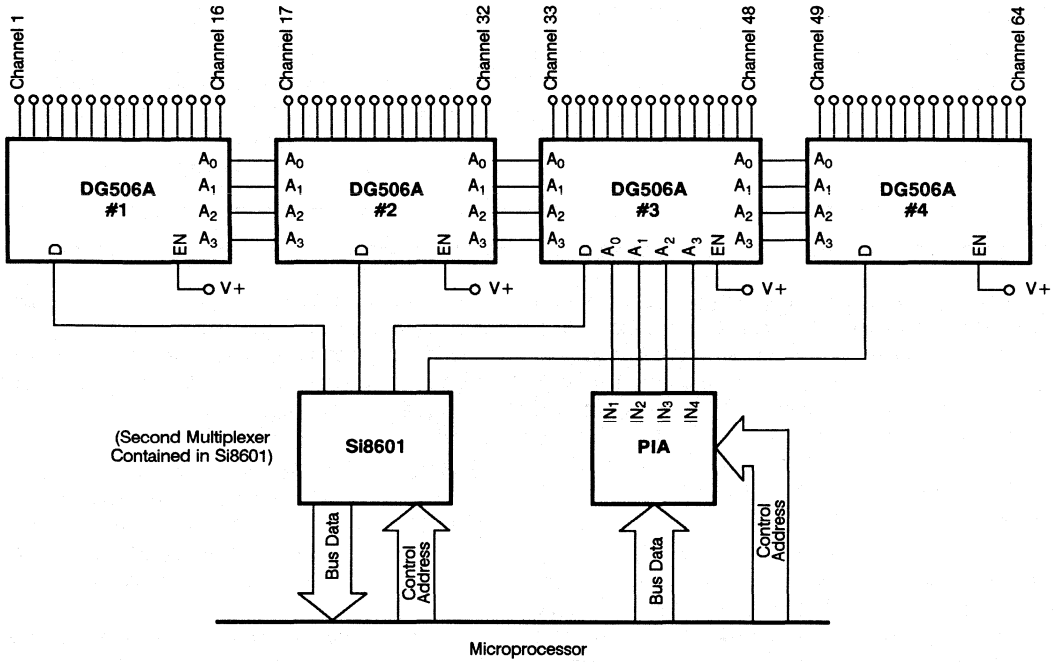


Figure 6. 64-Channel 2-Level Multiplex System

DG508A/509A
8-Channel/Dual 4-Channel CMOS Analog Multiplexers

Siliconix incorporated

FEATURES

- TTL & CMOS Direct Control Over Military Temperature Range
- Low Power (30 mW typ.)
- Break-Before-Make Switching
- 44 V Power Supply Rating

BENEFITS

- Easily Interfaced
- Reduced Power Consumption
- Reduced System Crosstalk
- Environmentally Rugged

APPLICATIONS

- Communication Systems
- Multiplexing Reference Signals
- Data Acquisition Systems
- Audio Signal Routing and Multiplexing

DESCRIPTION

The DG508A, an 8-channel single-ended analog multiplexer, is designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG509A, a dual 4-channel analog multiplexer, is designed to connect 1 of 4 dual inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1) logic. Break-before-make switching action protects against momentary shorting of the input signals.

A channel in the ON state conducts current equally well in both directions (bidirectional switches). In the OFF state each channel blocks voltages up to the power supply rails, normally 30 V peak-to-peak. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches OFF. All control inputs, address (A_X)and enable (EN) are TTL or CMOS compatible over the full specified operating temperature range.

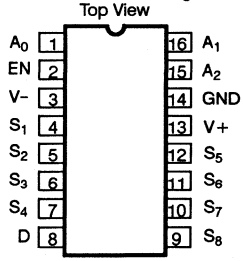
Designed in the Siliconix Plus 40 process, the absolute maximum voltage rating is extended to 44 Volts, allowing increased operating headroom for standard ± 15 V signal swings and operation with ± 20 V supplies. An epitaxial layer prevents latch up.

Both DG508A and DG509A are available in dual-in-line, CerDIP, plastic DIP and small outline packages, and are specified for operation over the military, A suffix (–55 to 125°C), industrial, B and D suffix (–25,–40 to 85°C), and commercial, C suffix (0 to 70°C), temperature ranges.

For applications requiring address data latching, the DG528/DG529 is recommended. DG408/409 is recommended for higher precision applications. For wideband/video routing and multiplexing applications, the DG538 is recommended.

PIN CONFIGURATION

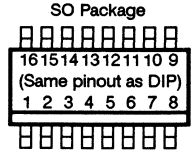
Dual-In-Line Package
Top View



Order Numbers:

CerDIP: DG508AAK, DG508ABK, DG508ACK, DG508AAK/883
Plastic: DG508ACJ

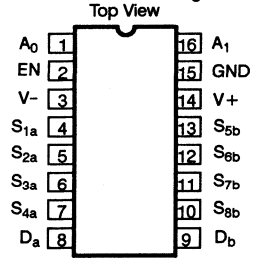
SO Package



Top View

Order Number:
DG508ADY, DG509ADY

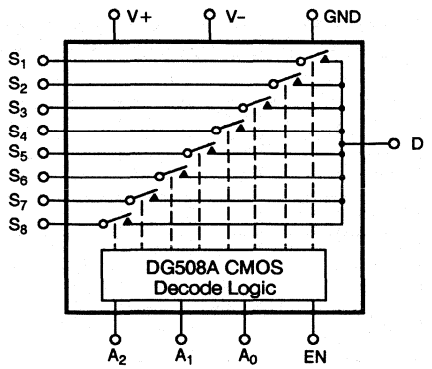
Dual-In-Line Package
Top View



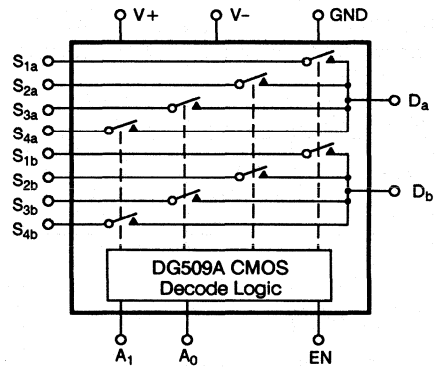
Order Numbers:

CerDIP: DG509AAK, DG509ABK, DG509ACK, DG509AAK/883
Plastic: DG509ACJ

FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES



DG508A
8-Channel Single Ended Multiplexer



DG509A
Differential 4-Channel Multiplexer

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V, Logic "1" = $V_{AH} \geq 2.4$ V

5

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C
(D Suffix) ..... -40 to 85°C
Storage Temperature (K Suffix) ..... -65 to 150°C
(J and Y Suffix) ..... -65 to 125°C
Power Dissipation (Package)*
16-Pin Ceramic DIP** ..... 900 mW
16-Pin Plastic DIP*** ..... 470 mW
16-Pin SO**** ..... 900 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.3 mW/°C above 75°C.
****Derate 7.7 mW/°C above 75°C.

SPECIFICATIONS[a]

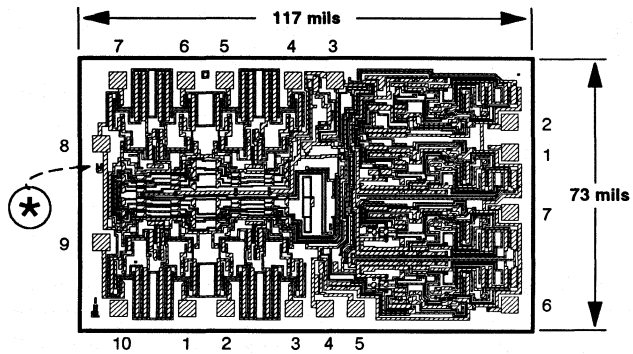
PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V		TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c, h]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	$V_D = \pm 10$ V, $V_{AL} = 0.8$ V $I_S = -200$ µA, $V_{AH} = 2.4$ V		Room Full			400 500		450 550	Ω
$r_{DS(ON)}$ Match		$\Delta r_{DS(ON)}$	-10 V < V_S < 10 V		Room	6					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	$V_S = \pm 10$ V $V_D = \mp 10$ V	Room Hot		-1 -50	1 50	-5 -50	5 50	µA
Drain OFF Leakage Current	DG508A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \mp 10$ V	Room Hot		-10 -200	10 200	-20 -200	20 200	µA
	DG509A	$I_{D(OFF)}$	V_{EN} = 0 V	$V_D = \pm 10$ V $V_S = \mp 10$ V	Room Hot		-10 -100	10 100	-20 -100	20 100	µA
Drain ON Leakage Current[e, g]	DG508A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V		Room Hot		-10 -200	10 200	-20 -200	20 200	µA
	DG509A	$I_{D(ON)}$	$V_S = V_D = \pm 10$ V $V_{AL} = 0.8$ V $V_{AH} = 2.4$ V		Room Hot		-10 -100	10 100	-20 -100	20 100	µA
DIGITAL CONTROL											
Logic Input Current Input Voltage High[h]		I_{AH}	V_A = 2.4 V		Room Hot	-0.002	-10 -30		-10 -30		µA
			V_A = 15 V		Room Hot	0.006		10 30		10 30	µA
Logic Input Current Input Voltage Low[h]		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Room Hot	-0.002	-10 -30		-10 -30		µA
DYNAMIC CHARACTERISTICS											
Transition Time		t_{TRANS}	See Figure 1		Room	0.6		1			µs
Break-Before-Make Time		t_{OPEN}	See Figure 3		Room	0.2					ns
Enable Turn-ON Time		$t_{ON(EN)}$	See Figure 2		Room	1		1.5			µs
Enable Turn-OFF Time		$t_{OFF(ON)}$			Room	0.4		1.0			µs
Charge Injection		Q			Room	20					pC
OFF Isolation[i]			V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 7 V_{RMS} f = 500 kHz		Room	68					dB
Logic Input Capacitance		C_{in}	f = 1 MHz		Room	8					pF
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_S = 0 V	Room	6					pF
Drain OFF Capacitance	DG508A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	25					pF
	DG509A	$C_{D(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_D = 0 V	Room	12					pF

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V GND = 0 V	TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	V_{EN} = 0 V or 2.4 V	Room	1.3		2.4		2.4	mA
Negative Supply Current	I-		Room	-0.7	-1.5		-1.5		

NOTES:
a: Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.
f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}\ MAX - r_{DS(ON)}\ MIN}{r_{DS(ON)}\ AVE} \right)$
g. $I_{D(ON)}$ is leakage from driver into "ON" switch.
h. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
i. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function DG508A	Function DG509A
1	A_0	A_0
2	EN	EN
3	V-	V-
4	S_1	S_{1a}
5	S_2	S_{2a}
6	S_3	S_{3a}
7	S_4	S_{4a}
8	D	D_a
9	S_8	D_b
10	NC	S_{4b}
11	S_7	S_{3b}
12	S_6	S_{2b}
13	S_5	S_{1b}
14	V+ (Substrate)	V+ (Substrate)
15	GND	NC
16	A_2	GND
17	A_1	A_1

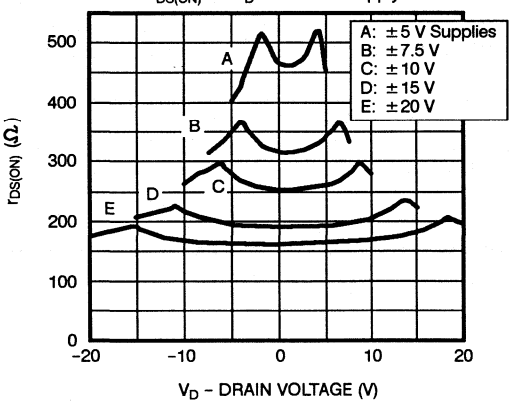
ICMG* *A = **DG508A**
4 Capacitors 85 p-channel Enhancement MOSFETs
7 Resistors 89 n-channel Enhancement MOSFETs
12 Diodes

ICMG* *B = **DG509A**
3 Capacitors 74 p-channel Enhancement MOSFETs
6 Resistors 81 n-channel Enhancement MOSFETs
10 Diodes

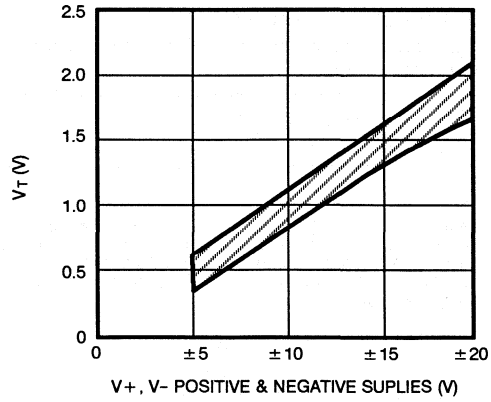
5

TYPICAL CHARACTERISTICS

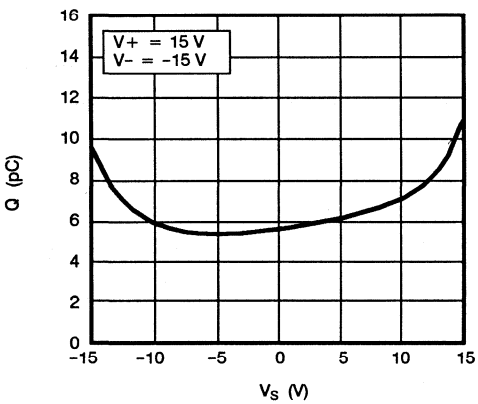
$r_{DS(ON)}$ vs. V_D and Power Supply



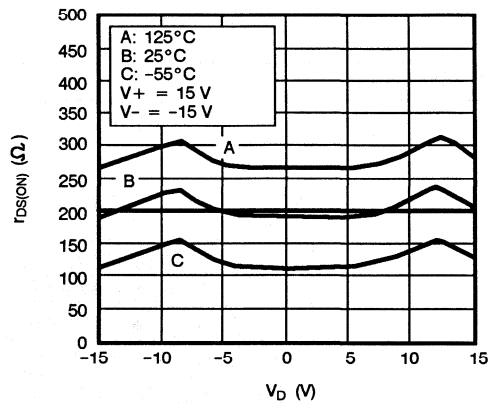
Input Switching Threshold vs. V+ and V- Supply Voltages



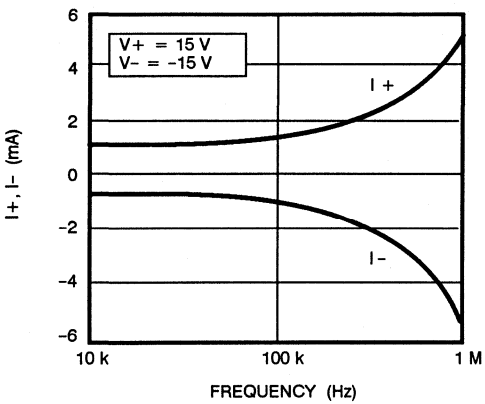
Charge Injection vs. Analog Voltage (V_S)



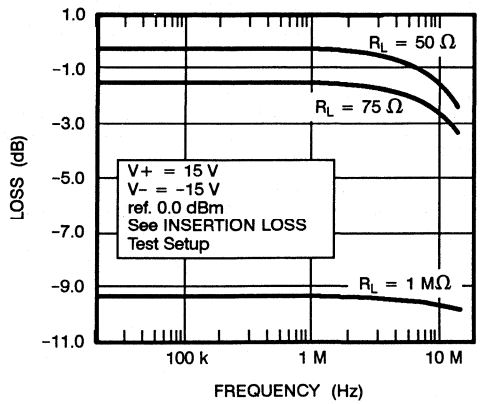
$r_{DS(ON)}$ vs. V_D and Temperature



Supply Current vs. Switching Frequency

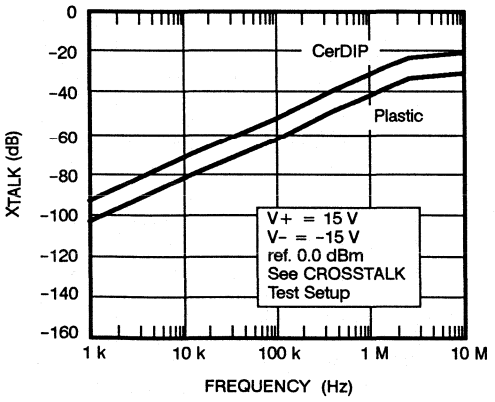


Insertion Loss vs. Frequency

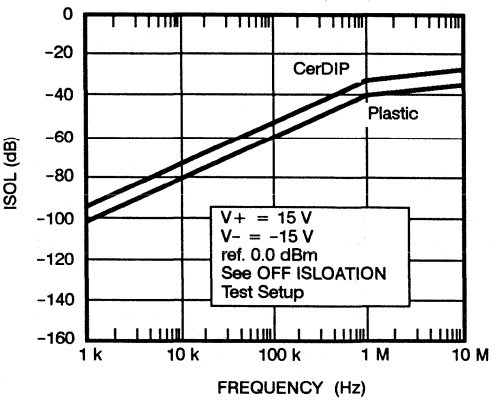


TYPICAL CHARACTERISTICS

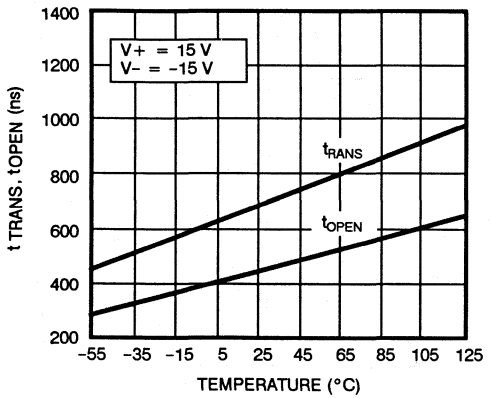
Crosstalk vs. Frequency



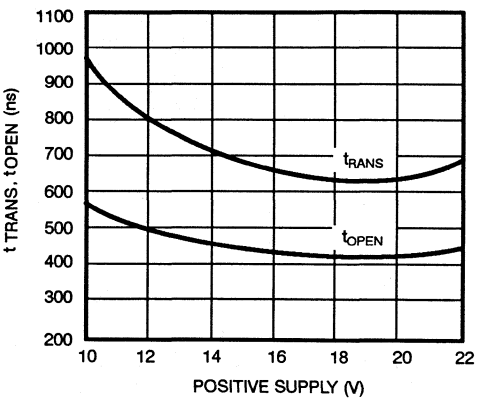
Off Isolation vs. Frequency



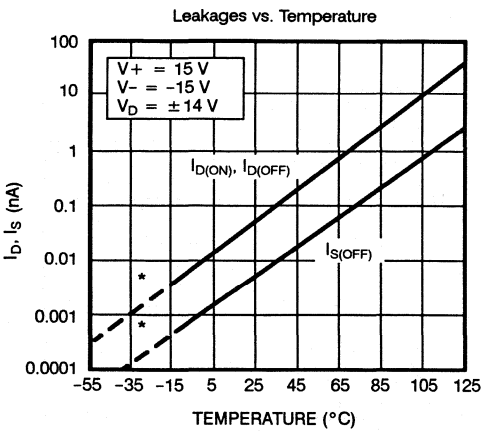
Switching Time vs. Temperature



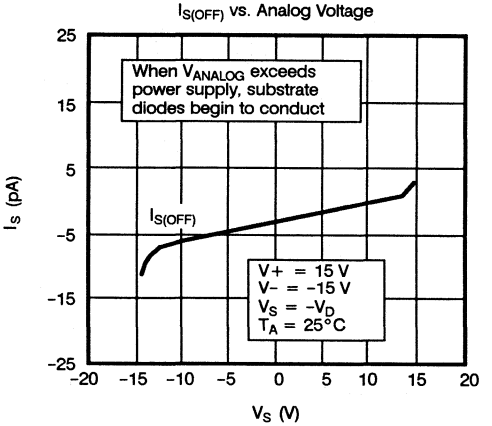
Switching Time vs. Positive Supply Voltage



Leakages vs. Temperature



IS(OFF) vs. Analog Voltage



* Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

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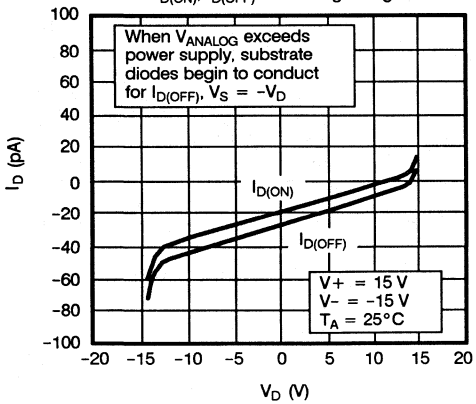
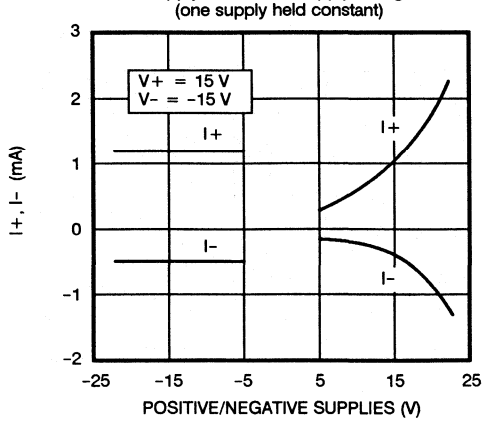
TYPICAL CHARACTERISTICS (Cont'd)

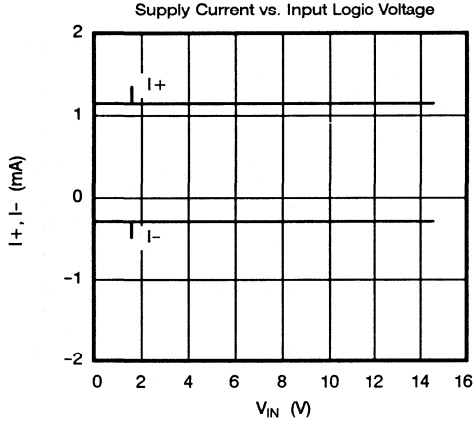
$I_{D(ON)}$, $I_{D(OFF)}$ vs. Analog Voltage



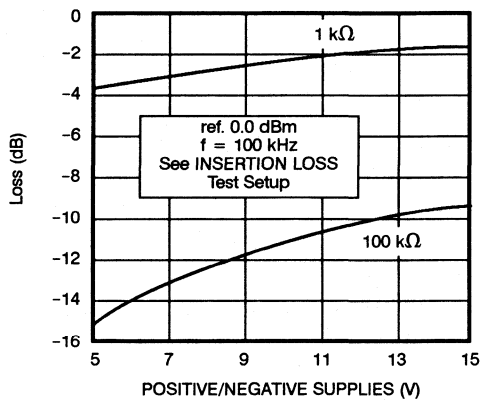
Supply Current vs. Supply Voltage (one supply held constant)



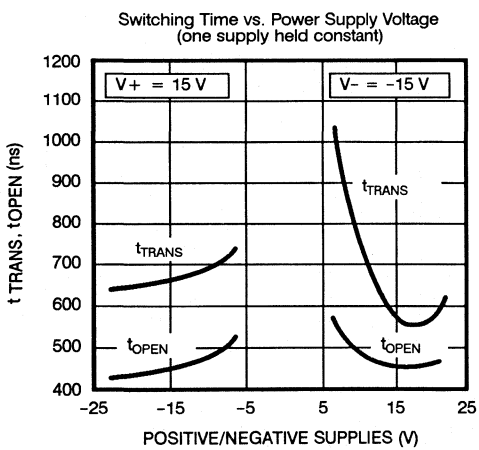
Supply Current vs. Input Logic Voltage



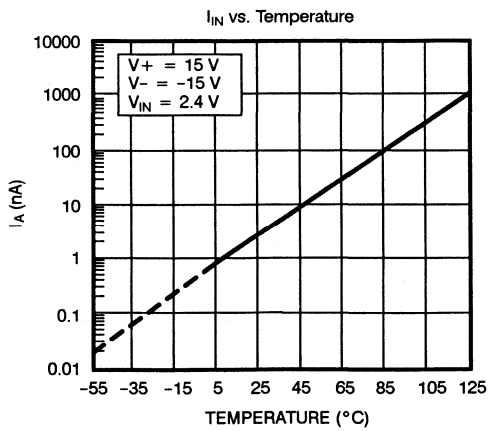
Insertion Loss vs. Power Supply Voltage



Switching Time vs. Power Supply Voltage (one supply held constant)

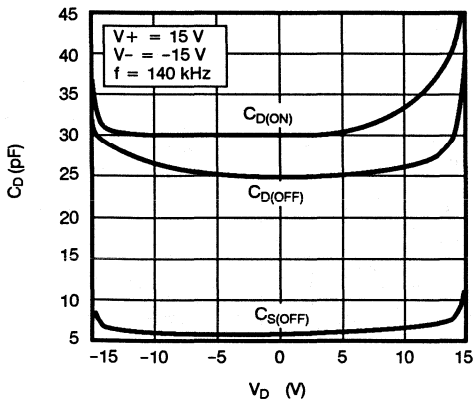


I_{IN} vs. Temperature

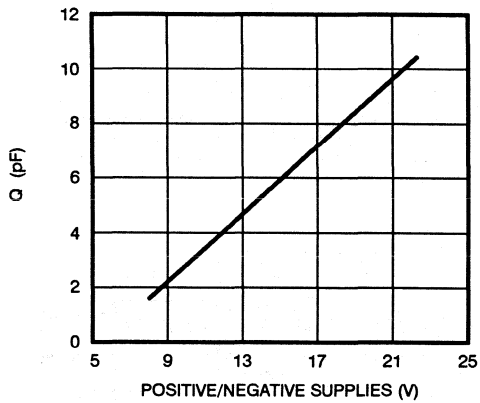


TYPICAL CHARACTERISTICS

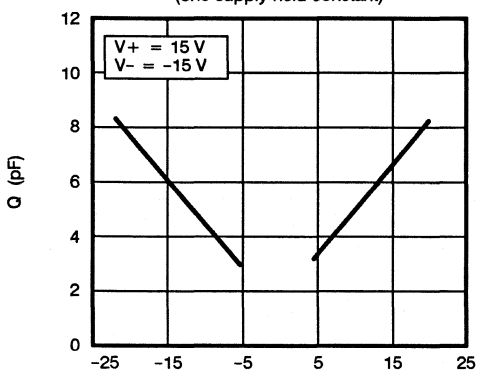
C_S, C_D vs. Analog Voltage



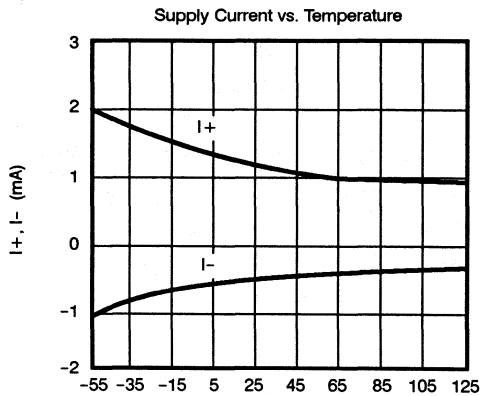
Charge Injection vs. Power Supply Voltage



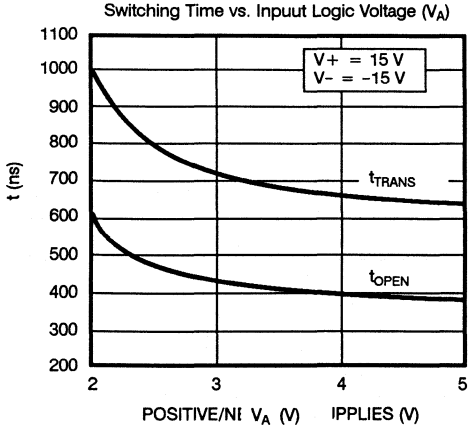
Charge Injection vs. Power Supply Voltage (one supply held constant)



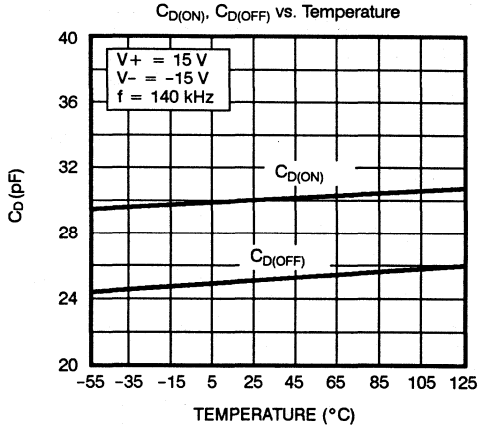
Supply Current vs. Temperature



Switching Time vs. Inpuut Logic Voltage (V_A)



$C_{D(ON)}$, $C_{D(OFF)}$ vs. Temperature



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TEST CIRCUITS

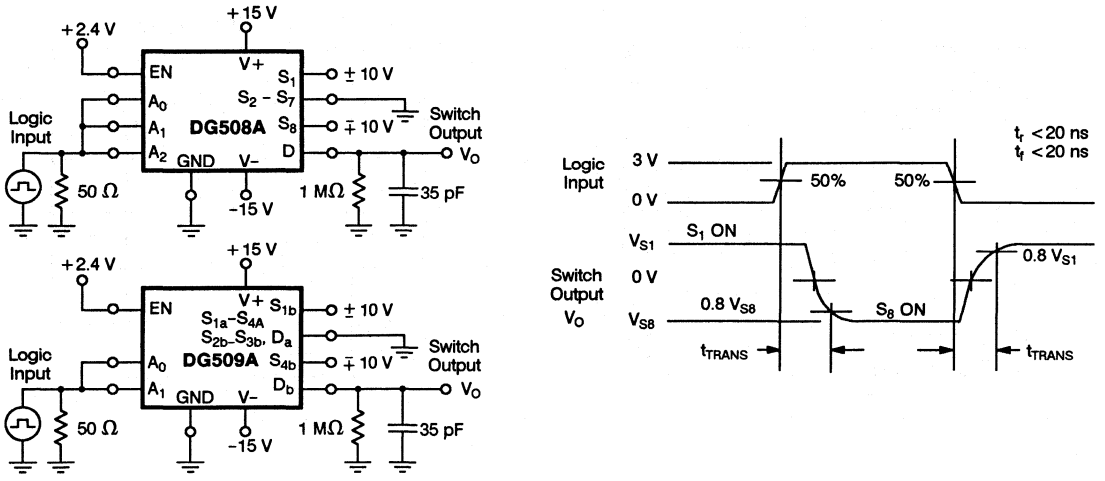

Figure 1. $t_{TRANSITION}$

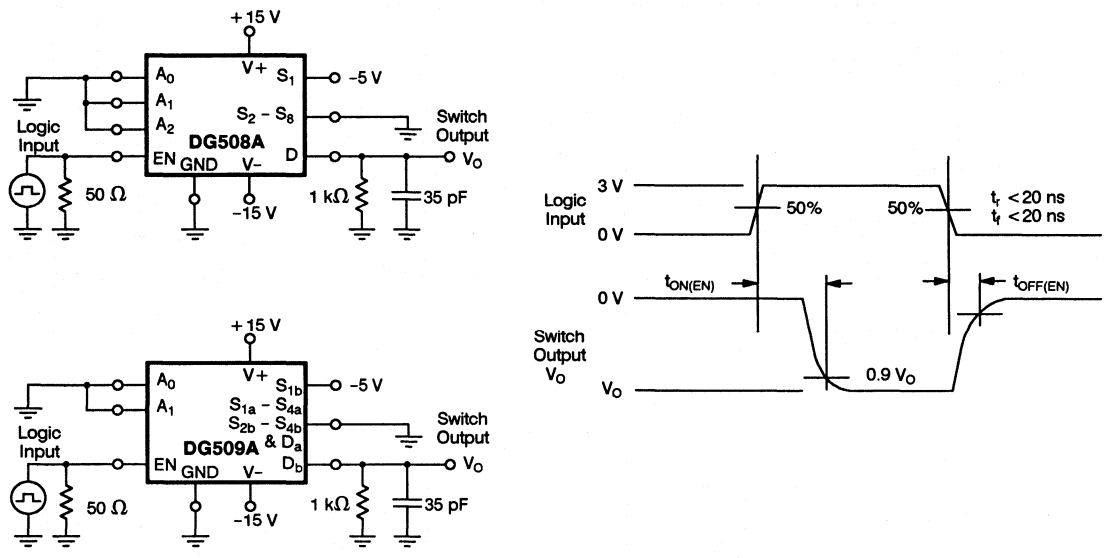

Figure 2. $t_{ON(EN)}$ and $t_{OFF(EN)}$

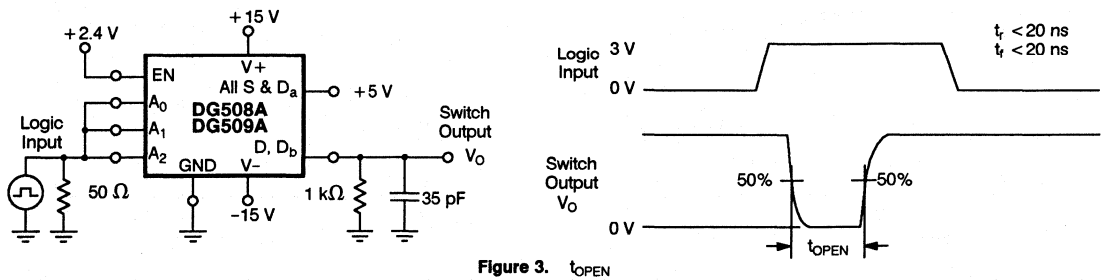

Figure 3. t_{OPEN}

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	Logic Input Voltage V_{INH} Min/V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
15**	-15	2.4/0.8	-15 to 15
12	-12	2.4/0.8	-12 to 12
10	-10	2.4/0.6	-10 to 10
8***	-8	2.4/0.4	-8 to 8

* Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
** Specifications chart based on V+ = +15 V, V- = -15 V.
*** Operation below ±8 V is not recommended due to the shift in $V_{INL(MAX)}$.

Fault Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 4). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference between V_S and the V- rail doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V-, but it preserves the low channel resistance and low leakage characteristics.

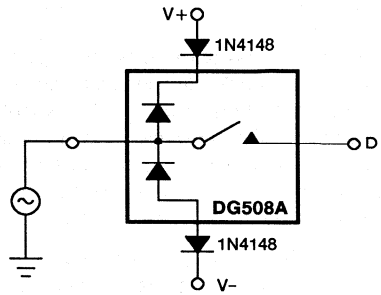

Figure 4. Overvoltage Protection Using Blocking Diodes

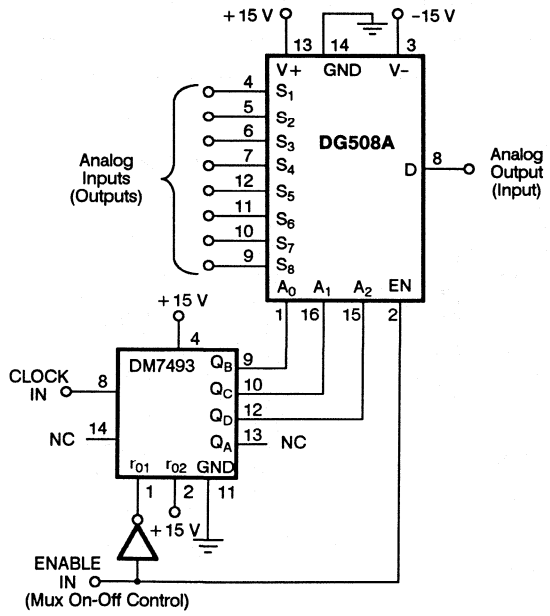

Figure 5. 8-Channel Sequential Mux/Demux

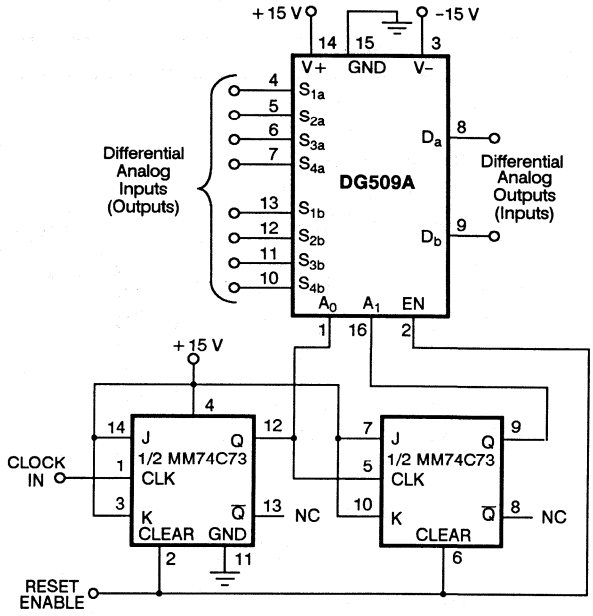

Figure 6. Differential 4-Channel Sequential Mux/Demux

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DG528/529
8-Channel and Dual 4-Channel Latchable Multiplexers

Siliconix incorporated

FEATURES

- TTL Compatible
- 44 V Power Supply
- On-Board Address Latches
- Low $r_{DS(ON)}$ (270 Ω Typ.)
- Break-Before-Make
- Improved ESD Protection >2500 V

BENEFITS

- Easily Interfaced
- Increased Analog Signal Range
- Microprocessor Bus Compatible
- Improved System Accuracy
- Reduced Crosstalk

APPLICATIONS

- Data Acquisition Systems
- Automatic Test Equipment
- Avionics and Military Systems
- Communication Systems
- Microprocessor Controlled Analog Systems
- Audio Signal Multiplexing

DESCRIPTION

DG528/529 analog multiplexers have on-chip address and control latches to simplify design in microprocessor based applications. Break-before-make switching action protects against momentary shorting of the input signals. The DG528/529 are built on the improved PLUS-40 CMOS process, which includes sandwich passivation and improved ESD protection up to 2500 V for ruggedness.

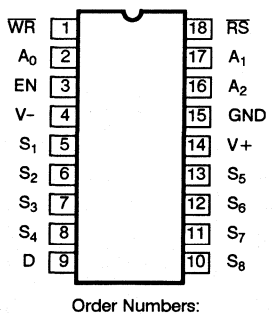
DG528 is an 8-channel single-ended analog multiplexer designed to connect 1 of 8 inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). DG529, a 4-channel dual analog multiplexer, is designed to connect 1 of 4 differential inputs to a common differential output as determined by its 2-bit binary address (A_0, A_1) logic. An epitaxial layer prevents latchup.

The on-board TTL-compatible address latches simplify the digital interface design and reduce board space in bus-controlled systems such as data acquisition systems, process controls, avionics, and ATE. The DG528 is available in 18-pin CerDIP in the military, A suffix (-55 to 125°C), industrial, B suffix (-25 to 85°C) and commercial, C suffix (0 to 70°C) temperature ranges, and in the plastic DIP for commercial temperature operation. The DG528 is also available in surface mount PLCC-20 for the extended industrial range (-40 to 85°C).

PIN CONFIGURATION

Dual-In-Line Package

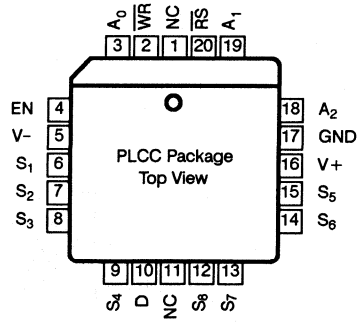
Top View



Order Numbers:

CerDIP: DG528AK, DG528AK/883
DG528BK, DG528CK

Plastic: DG528CJ

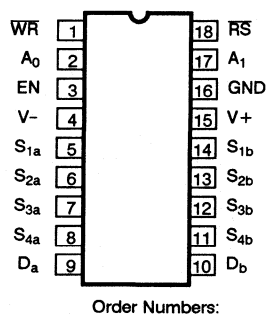


Order Number:

DG528DN

Dual-In-Line Package

Top View

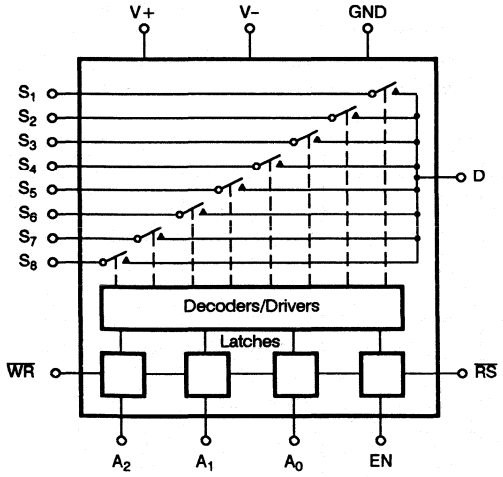


Order Numbers:

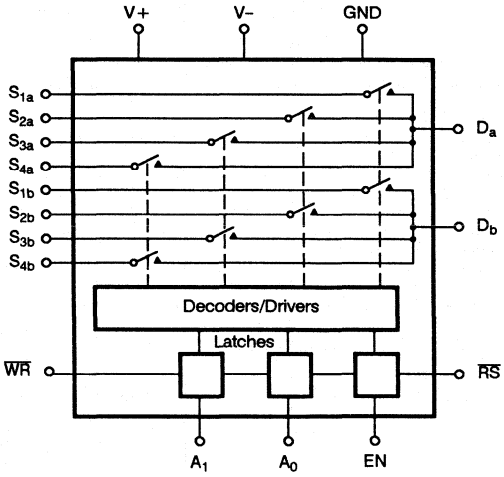
CerDIP: DG529AK/883
DG529BK

Plastic: DG529CJ

FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES



DG528
8-Channel Single-Ended Multiplexer



DG529
Differential 4-Channel Multiplexer

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching						
X	X	X	X	↓	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
Latching					
X	X	X	↓	1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "0" = $V_{AL} \leq 0.8$ V, Logic "1" = $V_{AH} \geq 2.4$ V

5

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ ..... 44 V
GND ..... 25 V
Digital Inputs[h], V_S, V_D ..... (V-) -2 V to (V+) +2 V or 20 mA, whichever occurs first.
Current (Any Terminal Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature (A Suffix) ..... -55 to 125°C
(B Suffix) ..... -25 to 85°C
(C Suffix) ..... 0 to 70°C
(D Suffix) ..... -40 to 85°C
Storage Temperature (A & B Suffix) ..... -65 to 150°C
(C & D Suffix) ..... -65 to 125°C

Power Dissipation (Package)*
18-Pin Ceramic DIP** ..... 900 mW
18-Pin Plastic DIP*** ..... 470 mW
20-Pin PLCC**** ..... 800 mW

*All leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C.
***Derate 6.3 mW/°C above 75°C.
****Derate 10 mW/°C above 75°C.

Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER		SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V		TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
ANALOG SWITCH											
Analog Signal Range[c, h]		V_{ANALOG}			Full		-15	15	-15	15	V
Drain-Source ON-Resistance[e]		$r_{DS(ON)}$	V_D = ±10 V, V_{AL} = 0.8 V I_S = -200 µA, V_{AH} = 2.4 V		Room Full	270		400 500		450 550	Ω
Greatest Change in $r_{DS(ON)}$ Between Channels[f]		$\Delta r_{DS(ON)}$	-10 V < V_S < 10 V		Room	6					%
Source OFF Leakage Current		$I_{S(OFF)}$	V_{EN} = 0 V	V_S = ±10 V V_D = ∓10 V	Room Full	-0.005	-1 -50	1 50	-5 -50	5 50	µA
Drain OFF Leakage Current	DG528	$I_{D(OFF)}$		V_D = +10 V V_S = ±10 V	Room Full	-0.015	-10 -200	10 200	-20 -200	20 200	
	DG529			V_D = +10 V V_S = ±10 V	Room Full	-0.008	-10 -100	10 100	-20 -100	20 100	
Drain ON Leakage Current[e, g]	DG528	$I_{D(ON)}$	V_S = V_D = ±10 V V_{EN} = 2.4 V		Room Full	-0.03	-10 -200	10 200	-20 -200	20 200	
	DG529		V_{AL} = 0.8 V V_{AH} = 2.4 V		Room Full	-0.015	-10 -100	10 100	-20 -100	20 100	
DIGITAL CONTROL											
Logic Input Current Input Voltage High[h]		I_{AH}	V_A = 2.4 V		Room Hot	-0.002	-10 -30		-10 -30		µA
			V_A = 15 V		Room Hot	0.006		10 30		10 30	
Logic Input Current Input Voltage Low[h]		I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V $\overline{RS}$ = 0 V, $\overline{WR}$ = 0 V		Room Hot	-0.002	-10 -30		-10 -30		
DYNAMIC CHARACTERISTICS											
Transition Time		t_{TRANS}	See Figure 3		Room	0.6		1			µs
Break-Before-Make Interval		t_{OPEN}	See Figure 5		Room	0.2					ns
Enable and Write Turn-ON Time		$t_{ON(EN, \overline{WR})}$	See Figures 4 and 6		Room	1		1.5			µs
Enable and Reset Turn-OFF Time		$t_{OFF(EN, \overline{RS})}$	See Figures 4 and 7		Room	0.4		1			
Charge Injection		Q	See Figure 8		Room	4					pC
OFF Isolation[l]			V_{EN} = 0 V, R_L = 1 kΩ C_L = 15 pF, V_S = 7 V_{RMS} f = 500 kHz		Room	68					dB
Logic Input Capacitance		C_{in}	f = 1 MHz		Room	2.5					pF
Source OFF Capacitance		$C_{S(OFF)}$	V_{EN} = 0 V f = 140 kHz	V_S = 0 V	Room	5					
Drain OFF Capacitance	DG528	$C_{D(OFF)}$		V_D = 0 V	Room	25					
	DG529				Room	12					

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V, $\overline{WR}$ = 0, $\overline{RS}$ = 2.4 V	TEMP[l]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	B, C, D SUFFIX MIN[b]	B, C, D SUFFIX MAX[b]	UNIT
MINIMUM INPUT TIMING REQUIREMENTS									
$\overline{WR}$ Pulse Width	t_{WW}	See Figure 1	Full		300		300		ns
A_X, EN Data Valid to $\overline{WR}$	t_{DW}	Stabilization Time, See Figure 1	Full		180		180		ns
A_X, EN Data Vaild after $\overline{WR}$	t_{WD}	Hold Time, See Figure 1	Full		30		30		ns
$\overline{RS}$ Pulse Width[l]	$t_{\overline{RS}}$	V_S = 5 V, See Figure 2	Full		500		500		ns
POWER SUPPLIES									
Positive Supply Current	I+	V_{EN} = 0 V, V_A = 0	Room			2.5		2.5	mA
Negative Supply Current	I-		Room		-1.5		-1.5		mA

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Sequence each switch ON.

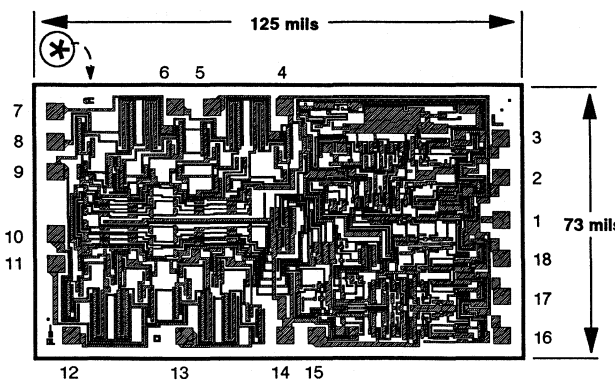
f. $\Delta r_{DS(ON)} = \left(\frac{r_{DS(ON)}MAX - r_{DS(ON)}MIN}{r_{DS(ON)}AVE} \right)$

g. $I_{D(ON)}$ is leakage from driver into "ON" switch.
h. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

i. Period of Reset ($\overline{RS}$) pulse must be at least 50 µs during or after power ON.
j. Room = 25°C, Cold and Hot = as determined by the operting temperature suffix.

5

DIE TOPOGRAPHY



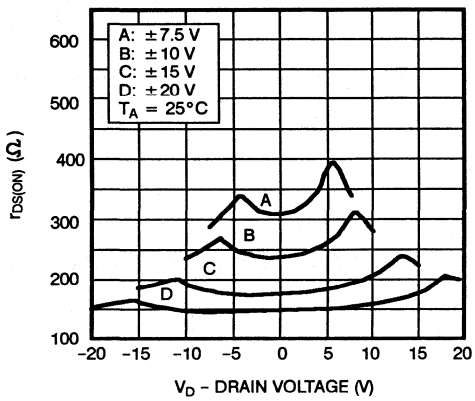
Pad No.	Function DG528	Pad No.	Function DG529
1	$\overline{WR}$	1	$\overline{WR}$
2	A_0	2	A_0
3	Enable	3	Enable
4	V-	4	V-
5	S_1	5	S_{1a}
6	S_2	6	S_{2a}
7	S_3	7	S_{3a}
8	S_4	8	S_{4a}
9	Drain	9	D_a
10	S_8	10	D_b
11	S_7	11	S_{4b}
12	S_6	12	S_{3b}
13	S_5	13	S_{2b}
14	V+ (Substrate)	14	S_{1b}
15	GND	15	V+ (Substrate)
16	A_2	16	GND
17	A_1	17	A_1
18	$\overline{RS}$	18	$\overline{RS}$

ICMLA ***A = DG528**
9 Resistors — 108 p-channel Enhancement MOSFETs
12 Diodes — 118 n-channel Enhancement MOSFETs
2 Zener Diodes — 2 PNP Bipolar Transistors

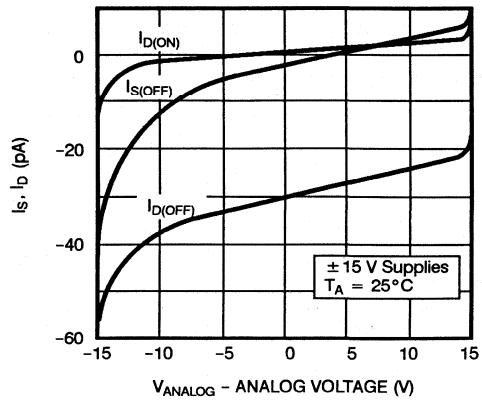
ICMLB ***B = DG527**
9 Resistors — 95 p-channel Enhancement MOSFETs
10 Diodes — 106 n-channel Enhancement MOSFETs
2 Zener Diodes — 2 PNP Bipolar Transistors

TYPICAL CHARACTERISTICS

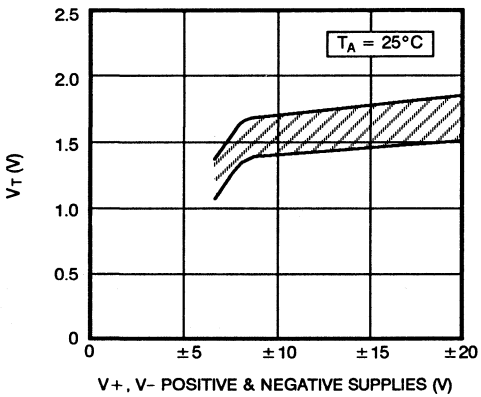
$r_{DS(ON)}$ vs. V_D and Power Supply



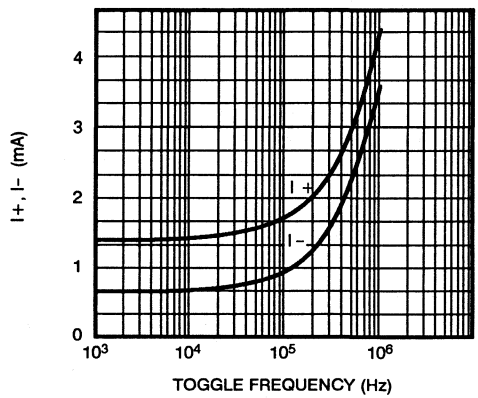
Leakage Currents vs. Analog Voltage



Input Switching Threshold vs. V+ and V- Supply Voltages



Supply Currents vs. Toggle Frequency



TIMING DIAGRAMS

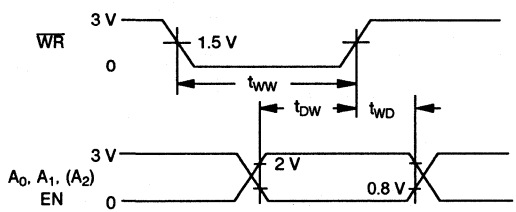


Figure 1.

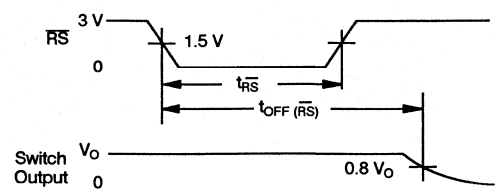
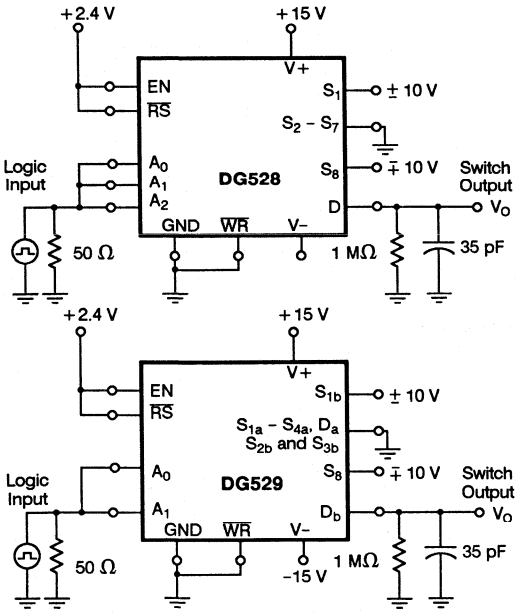


Figure 2.

TEST CIRCUITS



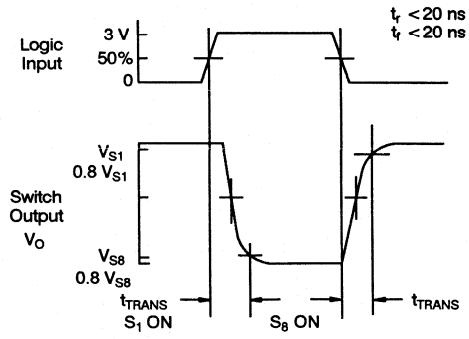
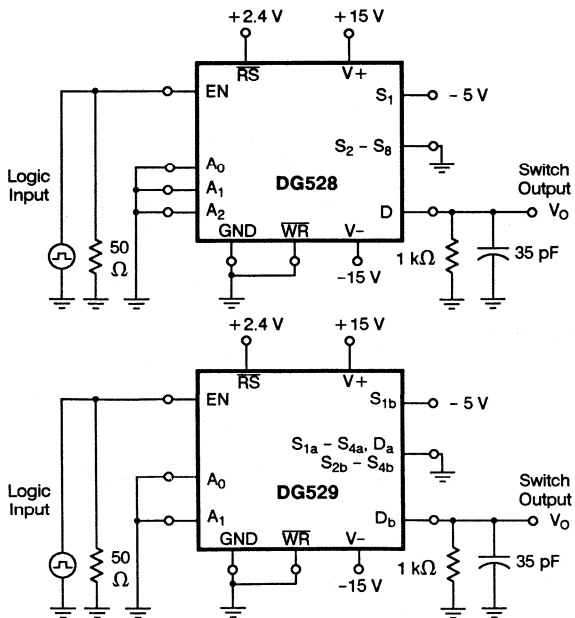


Figure 3. Transition Time



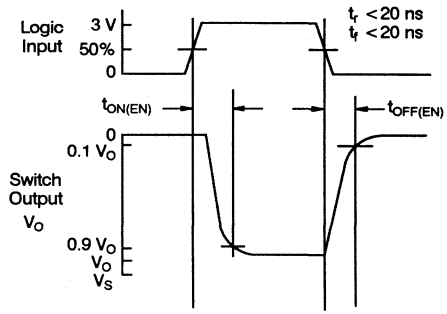


Figure 4. Enable t_{ON}/t_{OFF} Time

TEST CIRCUITS (Cont'd)

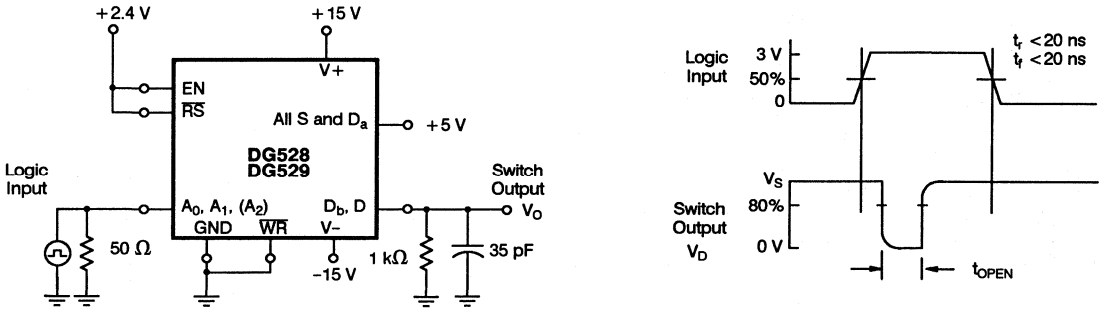
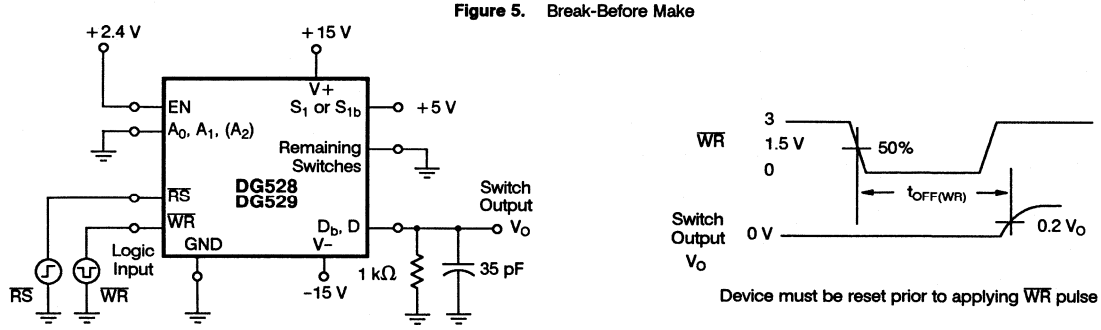


Figure 5. Break-Before Make



Device must be reset prior to applying $\overline{WR}$ pulse

Figure 6. Write Turn-On Time $t_{ON(\overline{WR})}$

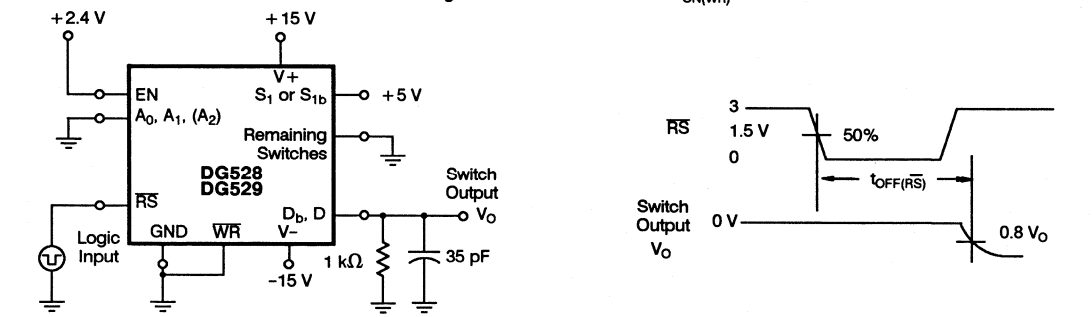
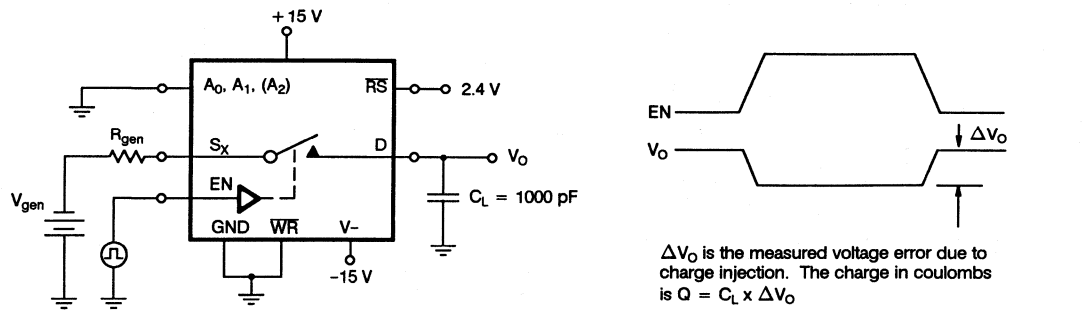


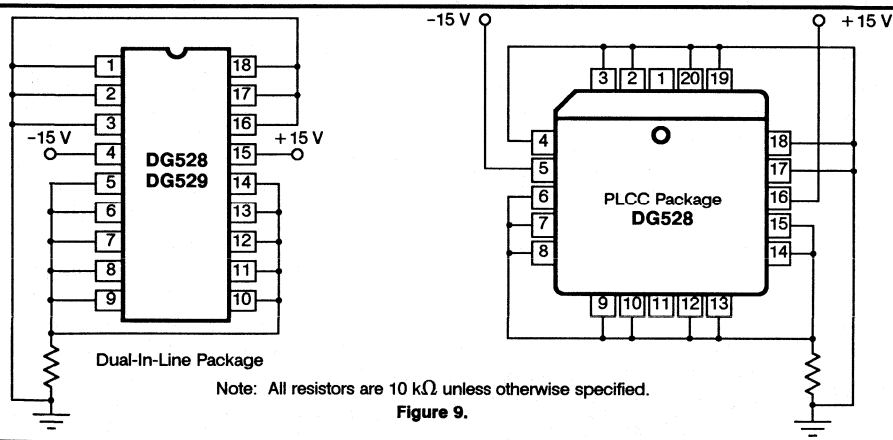
Figure 7. Reset Turn-Off Time $t_{OFF(\overline{RS})}$



ΔV_O is the measured voltage error due to charge injection. The charge in coulombs is $Q = C_L \times \Delta V_O$

Figure 8. Charge Injection

BURN-IN DIAGRAMS



Note: All resistors are 10 kΩ unless otherwise specified.

Figure 9.

DETAILED DESCRIPTION

The internal structure of the DG528 and DG529 includes a 5 V logic interface with input protection circuitry followed by a latch, level shifter, decoder and finally the switch constructed with parallel n- and p-channel MOSFETs (see Figure 10).

The input protection on the logic lines A_0, A_1, A_2, EN and control lines $\overline{WR}$, $\overline{RS}$ shown in Figure 10 minimize susceptibility to static encountered during handling and operational transients.

The logic interface circuit compares the TTL input signal against a TTL threshold reference voltage. The output of the comparator feeds the data input of a D type latch. The level sensitive D latch continuously places the D_X input signal on the Q_X output when the CLK ($\overline{WR}$) input is low, resulting in transparent latch operation. As soon as CLK ($\overline{WR}$) returns high the latch holds the data last present on the D_X input at the Q_X output, subject to the "Minimum Input Timing Requirements" table.

Following the latches the Q_X signals are level shifted and decoded to provide proper drive levels for the CMOS switches. This level shifting insures full ON/OFF switch operation for any analog signal present between the V+ and V- supply rails.

The enable (EN) pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply or to V+ if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used as a master reset. All latches are cleared regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low (see Truth Tables).

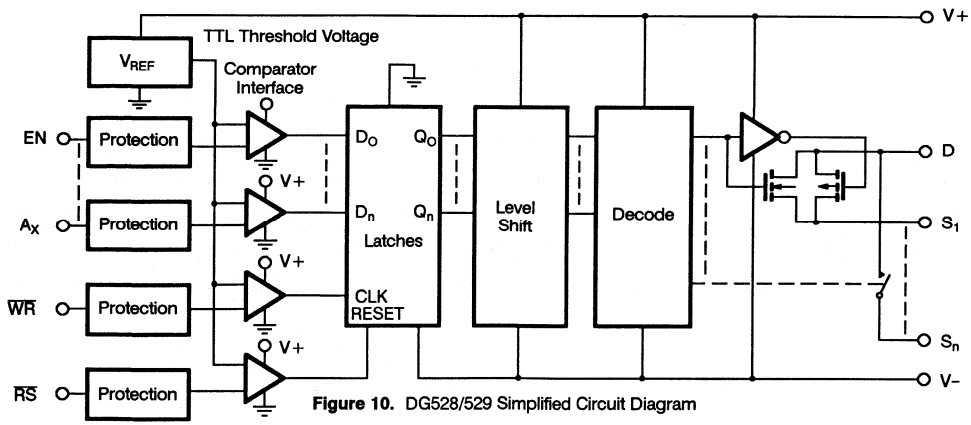


Figure 10. DG528/529 Simplified Circuit Diagram

BUS INTERFACING (See Figure 11)

The DG528 and DG529 minimize the amount of interface hardware between a microprocessor system bus and the analog system being controlled or measured. The internal TTL compatible latches give these multiplexers write-only memory, that is, they can be programmed to stay in a particular switch state (e.g., switch 1 ON) until the microprocessor determines it is necessary to turn different switches ON or turn all switches OFF.

The input latches become transparent when $\overline{WR}$ is held low; therefore, these multiplexers operate by direct command of the coded switch state on A_2, A_1, A_0. In this mode the DG528 is identical to the very popular DG508. The same is true of the DG529 versus the popular DG509A.

Initially during system power-up $\overline{RS}$ would be active LOW maintaining all 8 switches in the OFF state. After $\overline{RS}$ returned HIGH the DG528 maintains all switches in the OFF state. As soon as the system program was ready to perform a write operation to the address assigned to the DG528, the address decoder would provide a $\overline{CS}$ active LOW signal which is gated with the WRITE ($\overline{WR}$) control signal. At this time the data on the DATA BUS (that will determine which switch to close) is stabilizing. When the $\overline{WR}$ signal returns to the HIGH state, (positive edge) the input latches of the DG528 save the data from the DATA BUS. The coded information in the A_0, A_1, A_2 and EN latches is decoded and the appropriate switch is turned ON.

The EN latch allows all switches to be turned OFF under program control. This becomes useful when two or more DG528s are cascaded to build 16-line and larger multiplexers.

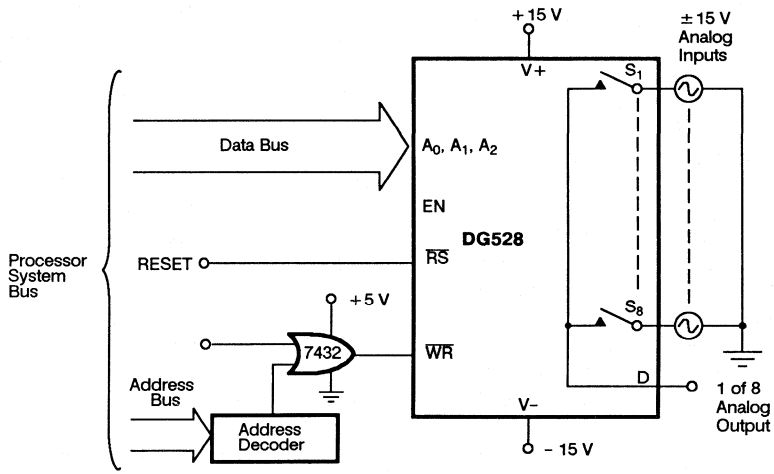


Figure 11. Bus Interface

APPLICATIONS HINTS

V+ Positive Supply Voltage (V)	V- Negative Supply Voltage (V)	GND Digital GND (V)	Logic Input Voltage V_{INH}Min/V_{INL}Max (V)	V_S or V_D Analog Voltage Range (V)
20	-20	0	2.4/0.8	±20
15	-25	0	2.4/0.8	±15
8	-8 (Min)	0	2.4/0.8	±8

Siliconix incorporated

DG601
High-Speed Quad SPST CMOS Analog Switch

FEATURES

- Fast Switching Action
  t_{ON} = 30 ns (typ)
  t_{OFF} = 14 ns (typ)
- Low ON-Resistance
  ($r_{DS(ON)}$ <20 Ω)
- Single-Supply Operation
- Low Charge Injection
- TTL Compatible
- ESD Protection > ±4000 V

BENEFITS

- Improved Data Throughput
- Reduced Switching Errors
- Simplified Power Supply
- Reduced Switching Transients
- Simplified Interfacing
- Improved Reliability

APPLICATIONS

- Disk Drives
- Fast Sample/Hold
- Precision Instrumentation
- Computer Peripherals
- Low Noise Op Amp Gain Switching
- Military Systems

DESCRIPTION

The DG601 is a high performance quad SPST CMOS analog switch intended for applications where fast switching, low charge injection and low ON resistance are required. The DG601 features single-supply operation, and is TTL-compatible with either a single 12 V supply, a single 5 V supply, or with ±5 V supplies.

Applications for the DG601 include 12 V systems requiring TTL or 5 V logic levels, such as disk drives and other computer peripherals. The fast switching time and low charge injection make the DG601 ideal for high speed data acquisition applications such as sample and hold amplifiers, channel selection and gain ranging.

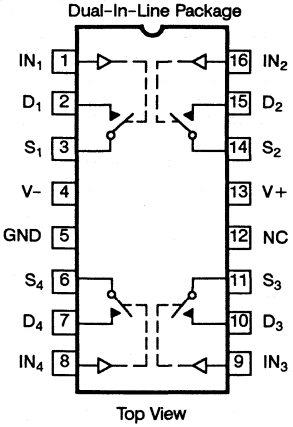
The DG601 is built on the Siliconix proprietary PolyMOS process, allowing low parasitic capacitance to facilitate high speed switching. It is available in 16-pin plastic DIP and SO packages for industrial, D suffix (-40 to 85°C), and in the CerDIP for military, A suffix (-55 to 125°C) temperature ranges.

For additional information refer to Technical Article TA89-3.

5

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package

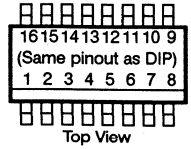


Top View

Order Numbers:

CerDIP: DG601AK
Plastic: DG601DJ

Narrow Body
SO Package



Top View

Order Number:

DG601DY

Four SPST Switches per Package*

Truth Table

Logic	Switch
0	ON
1	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

* Switches shown for logic "1" input.

Siliconix incorporated

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V–[1]

V+ ..... 22 V

GND ..... 13 V

Digital Inputs[1], V_S, V_D ..... (V–) –2 V to (V+) plus 2 V or 30 mA, whichever occurs first

Current (any terminal) ..... 30 mA

Current (S or D)
(Pulsed 1 ms at 10% duty cycle) ..... 100 mA

ESD Protection[c] (method 3015.5) ..... ±4000 V

Storage Temperature (A Suffix) ..... –65 to 150°C
(D Suffix) ..... –65 to 125°C

Operating Temperature (A Suffix) ..... –55 to 125°C
(D Suffix) ..... –40 to 85°C

Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 470 mW
16-Pin CerDIP*** ..... 900 mW
16-Pin SO**** ..... 900 mW

*All leads welded or soldered to PC board
**Derate 6.5 mW/°C above 25°C
***Derate 12 mW/°C above 75°C
****Derate 7.7 mW/°C above 25°C

[1]Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to 30 mA.

SPECIFICATIONS[a] (SINGLE +12 V SUPPLY)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V– = 0 V, V_{IN} = 2.0 V, 0.8 V[e]	TEMP[g]	TYP[d]	A SUFFIX –55 to 125°C MIN[b]	A SUFFIX –55 to 125°C MAX[b]	D SUFFIX –40 to 85°C MIN[b]	D SUFFIX –40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V+ = 10.8 V, I_S = 10 mA, V_D = 10 V, 2 V	Room	20		35			Ω
			Full			50			
Delta Drain-Source ON-Resistance	$\Delta r_{DS(ON)}$		Room	2.2		6		6	
			Full			10		10	
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 13.2 V, V– = 0 V, V_D = 12.2 V, 1 V, V_S = 1 V, 12.2 V	Room	0.01	–4	4	–4	4	nA
			Hot		–100	100	–100	100	
	$I_{D(OFF)}$		Room	0.01	–4	4	–4	4	
			Hot		–100	100	–100	100	
Channel ON Leakage Current	$I_{D(ON)}$	V+ = 13.2 V, V– = 0 V, V_S, V_D = 1 V, 12.2 V	Room	0.1	–4	4	–4	4	
			Hot		–200	200	–200	200	
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Full	-10^{-5}	–10		–10		µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Full	10^{-5}		10		10	
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF, See Figure 1	Room	30		45		45	ns
Turn-OFF Time	t_{OFF}		Room	14		30		30	
Charge Injection	Q	C_L = 1,000 pF, V_{gen} = 6 V, R_{gen} = 0 Ω, See Figure 2	Room	13					pC
OFF Isolation Reject Ratio	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	69					dB
Crosstalk (Channel-to-Channel)		R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	88					
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 6 V	Room	8					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	8					
Channel ON Capacitance[d]	$C_{D+S(ON)}$		Room	20					

SPECIFICATIONS[a] (SINGLE +12 V SUPPLY)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 12 V, V- = 0 V V_{IN} = 2.0 V, 0.8 V[e]	TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Curent	I+	V_{IN} = 0 V or 5 V	Room	2.2		6		6	mA
			Full			8		8	
Negative Supply Current	I-		Room	-2.1	-6		-6		
			Full		-8		-8		

SPECIFICATIONS[a] (DUAL SUPPLIES)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = -5 V V_{IN} = 2.0 V, 0.8 V[e]	TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		-5	5	-5	5	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V+ = 4.5 V, V- = -4.5 V	Room	27		40		40	Ω
			Full			60		60	
Delta Drain-Source ON-Resistance	$\Delta r_{DS(ON)}$	I_S = -10 mA, V_D = ±3.5 V	Room	2		6		6	
			Full			10		10	
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 5.5 V, V- = -5.5 V	Room	0.01					nA
	$I_{D(OFF)}$	V_D = -4.5 V, V_S = 4.5 V V_D = 4.5 V, V_S = -4.5 V	Room	0.01					
Channel ON Leakage Current	$I_{D(ON)}$	V+ = 5.5 V, V- = 5.5 V V_S = V_D = ±4.5 V	Room	0.1					
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V All Other = 5 V	Room	-10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V All Other = 0 V	Room	10					
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF	Room	34					ns
Turn-OFF Time	t_{OFF}	See Figure 1	Room	20					
Charge Injection	Q	C_L = 1,000 pF V_{gen} = 0 V, R_{gen} = 0 Ω See Figure 2	Room	11					pC
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 0 V	Room	8					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	8					
Channel ON Capacitance[d]	$C_{D+S(ON)}$		Room	21					
POWER SUPPLIES									
Positive Supply Curent	I+	V+ = 5.5 V, V- = -5.5 V	Room	2.2					mA
Negative Supply Current	I-	V_{IN} = 0 V or 5 V	Room	-1.8					

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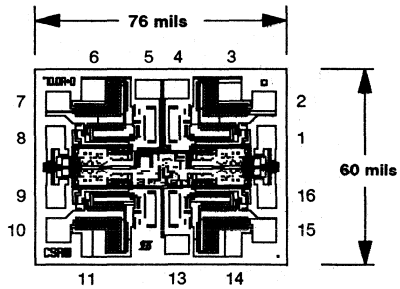
SPECIFICATIONS[a] (SINGLE +5 V SUPPLY)

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = 0 V V_{IN} = 2.0 V, 0.8 V[e]	TEMP[g]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[c]	V_{ANALOG}		Full		0	5	0	5	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	V+ = 4.5 V	Room	50		100		100	Ω
		I_S = -10 mA, V_D = 2 V, 3.5 V	Full			140		140	
Delta Drain-Source ON-Resistance	$\Delta r_{DS(ON)}$		Room	2		10		10	
			Full			15		15	
Switch OFF Leakage Current	$I_{S(OFF)}$	V+ = 5.5 V V_D = 1 V, V_S = 4.5 V	Room	0.01					nA
	$I_{D(OFF)}$	V+ = 5.5 V V_D = 4.5 V, V_S = 1 V	Room	0.01					
Channel ON Leakage Current	$I_{D(ON)}$	V+ = 5.5 V V_S = V_D = 4.5 V, 1 V	Room	0.1					
DIGITAL CONTROL									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0 V	Room	-10					pA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 5 V	Room	10					
DYNAMIC CHARACTERISTICS									
Turn-ON Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF	Room	32					ns
Turn-OFF Time	t_{OFF}	See Figure 1	Room	25					
Charge Injection	Q	C_L = 1,000 pF, V_{gen} = 2.5 V, R_{gen} = 0 Ω, See Figure 2	Room	6					pC
Source OFF Capacitance[d]	$C_{S(OFF)}$	f = 1 MHz, V_S = 2.5 V	Room	8					pF
Drain OFF Capacitance[d]	$C_{D(OFF)}$		Room	8					
Channel ON Capacitance[d]	$C_{D + S (ON)}$		Room	22					
POWER SUPPLIES									
Positive Supply Current	I+	V+ = 5.5 V	Room	1.2					mA
Negative Supply Current	I-	V_{IN} = 0 V or 5 V	Room	-0.8					

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. $\Delta r_{DS(ON)}$ compares ON-resistance at a fixed value for V_D, i.e., the change is specified between channels, not over analog range.
g. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



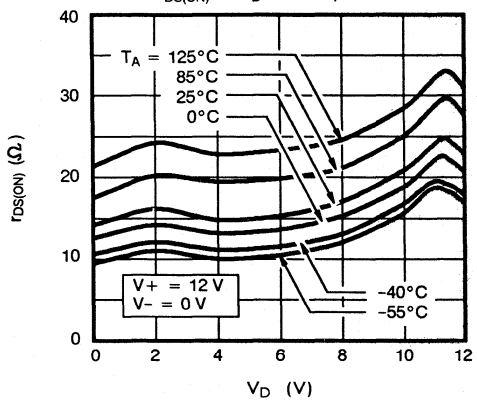
Pad No.	Function
1	IN_1
2	D_1
3	S_1
4	V-
5	GND
6	S_4
7	D_4
8	IN_4
9	IN_3
10	D_3
11	S_3
12	NC
13	V+ (Substrate)
14	S_2
15	D_2
16	IN_2

CSAW

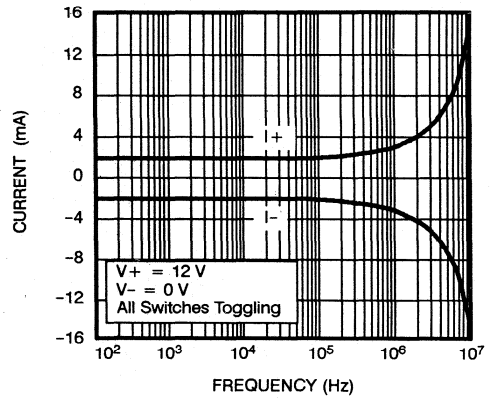
42 n-channel MOS Transistors
36 p-channel MOS Transistors
1 NPN Transistors
5 Resistors
8 Diodes
9 Capacitors
2 Zener Diodes

TYPICAL CHARACTERISTICS

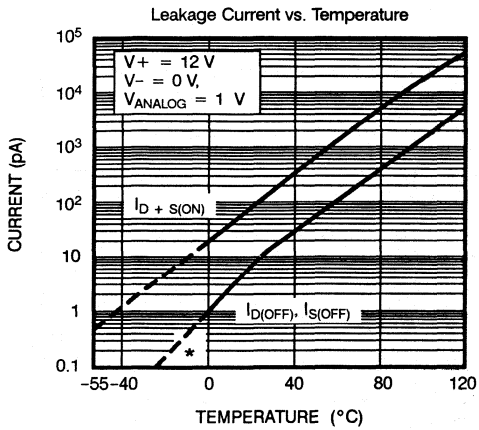
$r_{DS(ON)}$ vs. V_D and Temperature



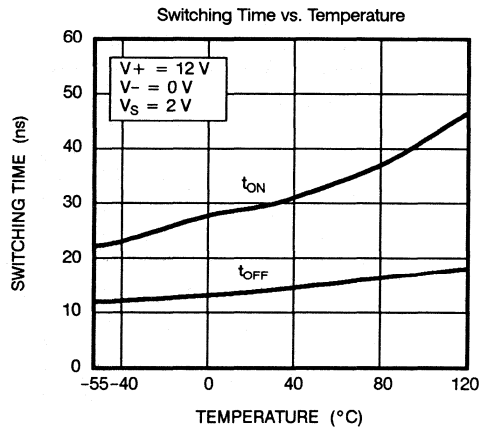
Supply Current vs. Switching Frequency



Leakage Current vs. Temperature



Switching Time vs. Temperature

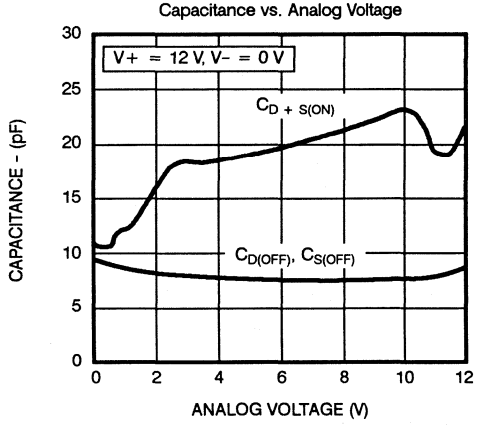


*Leakage currents in this region are determined by extrapolation. Attempts to measure in production are limited by the ability to control humidity and leakages pin to pin below the dew point (where water condenses).

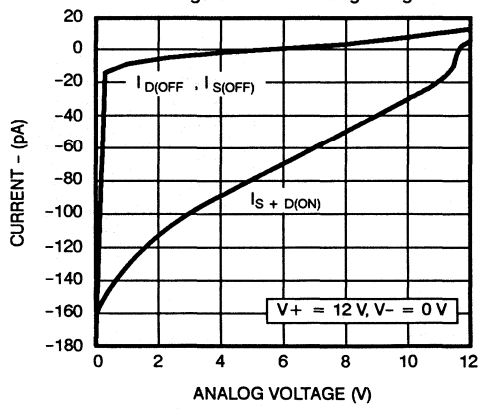
5

TYPICAL CHARACTERISTICS (Cont'd)

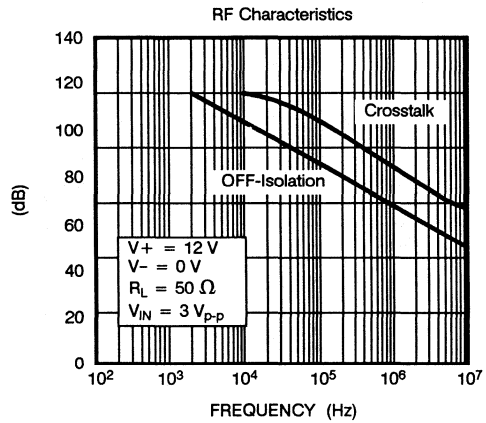
Capacitance vs. Analog Voltage



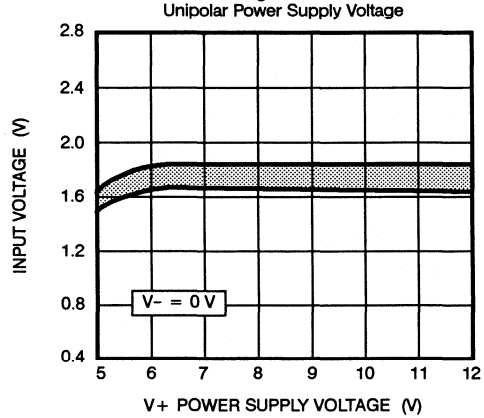
Leakage Current vs. Analog Voltage



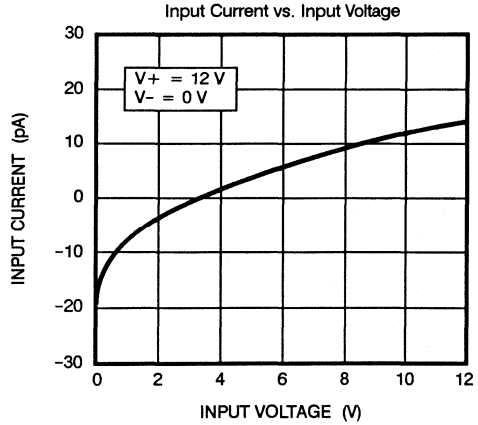
RF Characteristics



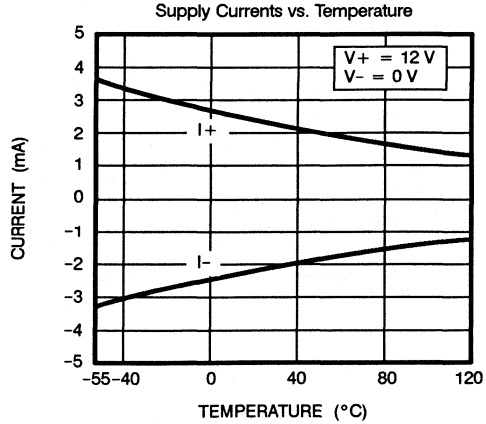
Switching Threshold vs. Unipolar Power Supply Voltage



Input Current vs. Input Voltage

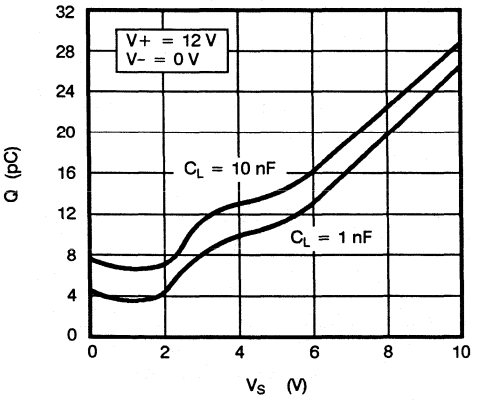


Supply Currents vs. Temperature

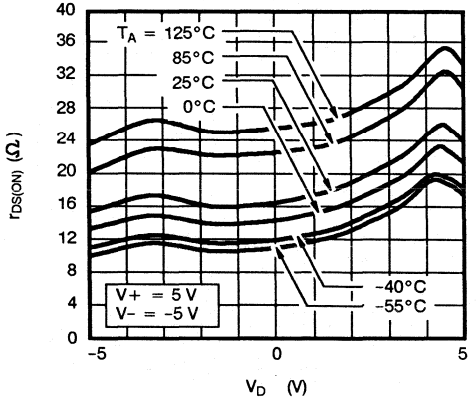


TYPICAL CHARACTERISTICS (Cont'd)

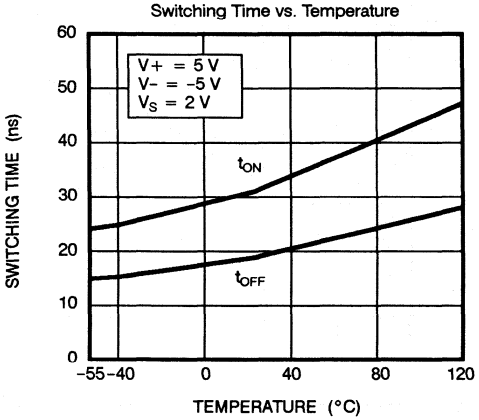
Charge Injection vs. V_S



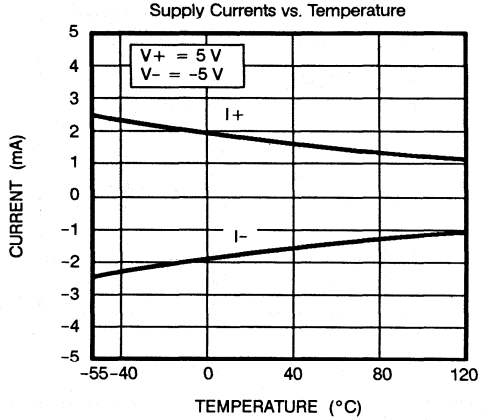
$r_{DS(ON)}$ vs. V_D and Temperature



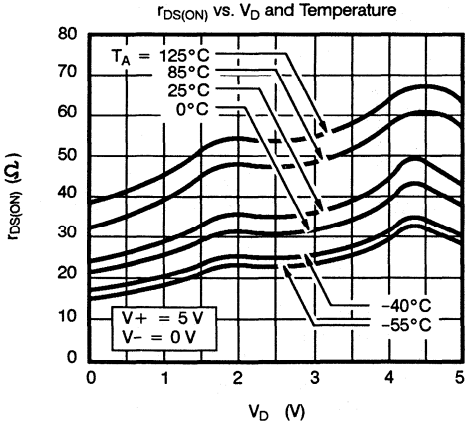
Switching Time vs. Temperature



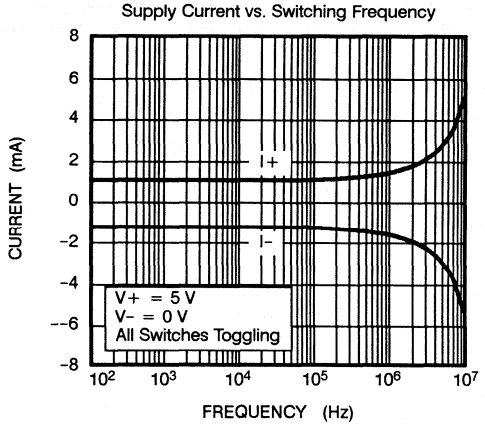
Supply Currents vs. Temperature



$r_{DS(ON)}$ vs. V_D and Temperature



Supply Current vs. Switching Frequency



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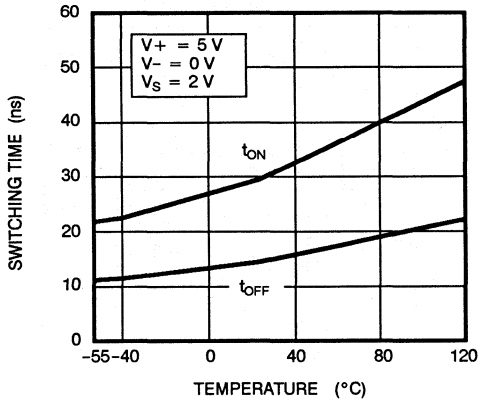
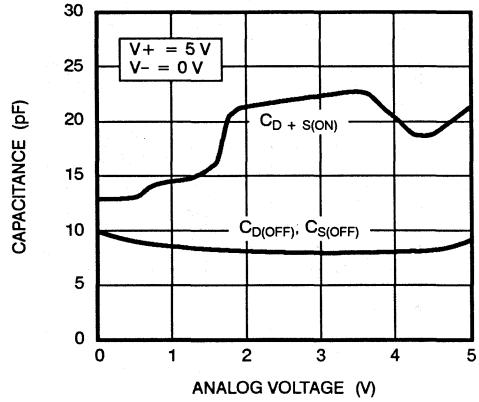
TYPICAL CHARACTERISTICS (Cont'd)

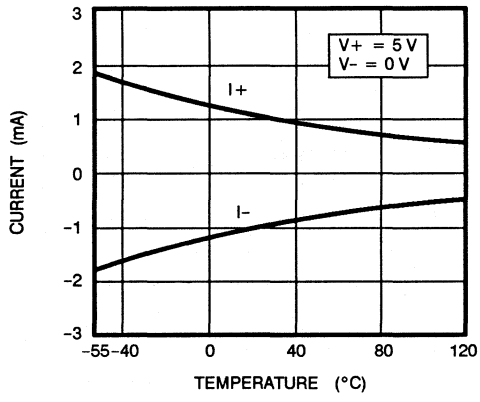
Switching Time vs. Temperature



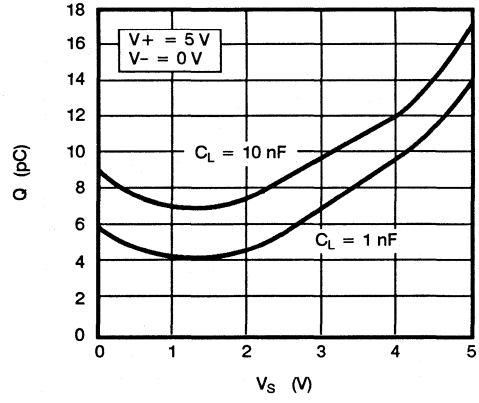
Capacitance vs. Analog Voltage



Supply Currents vs. Temperature

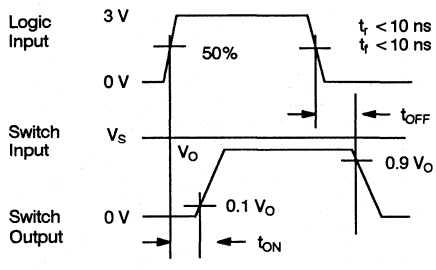


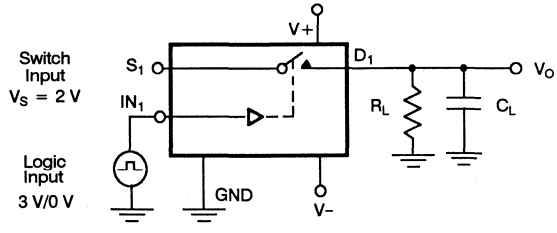
Charge Injection vs. V_S



TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.





Repeat test for Channels 2, 3, and 4.

For load conditions, See Specifications

C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

Figure 1. Switching Time

TEST CIRCUITS (Cont'd)

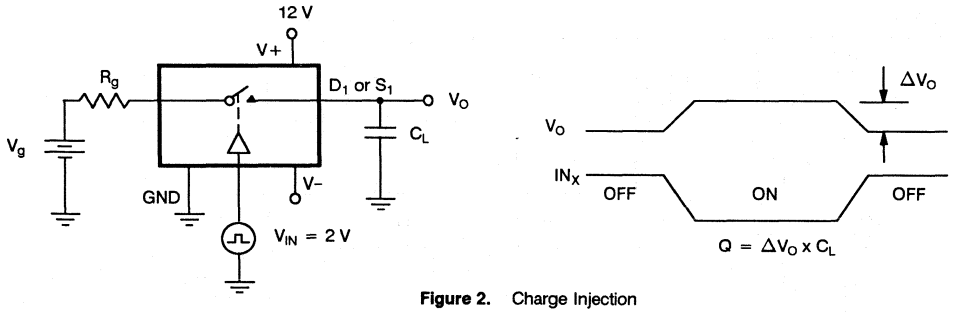


Figure 2. Charge Injection

Frequency Tested	Signal Generator	Analyzer
100 Hz to 13 MHz	HP3330B Automatic Synthesizer	HP3571A Tracking Spectrum Analyzer

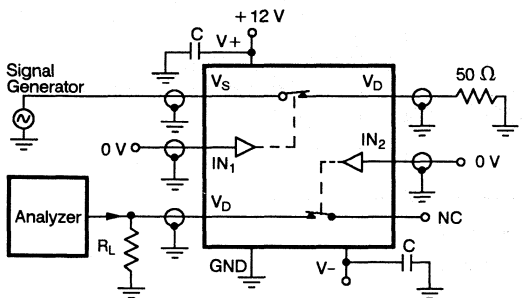


Figure 3. Crosstalk

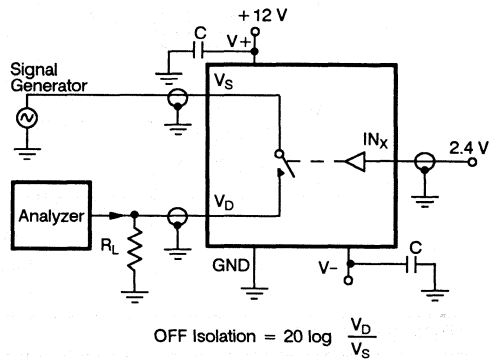


Figure 4. OFF Isolation

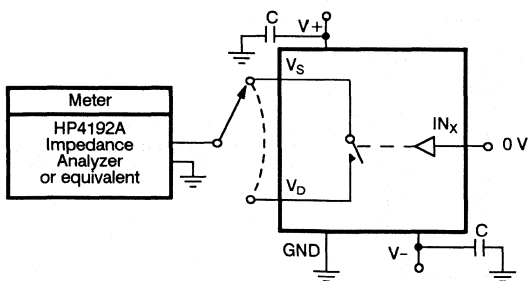
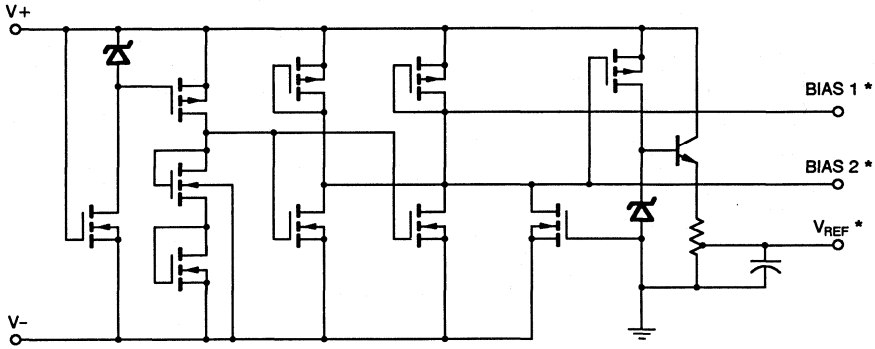


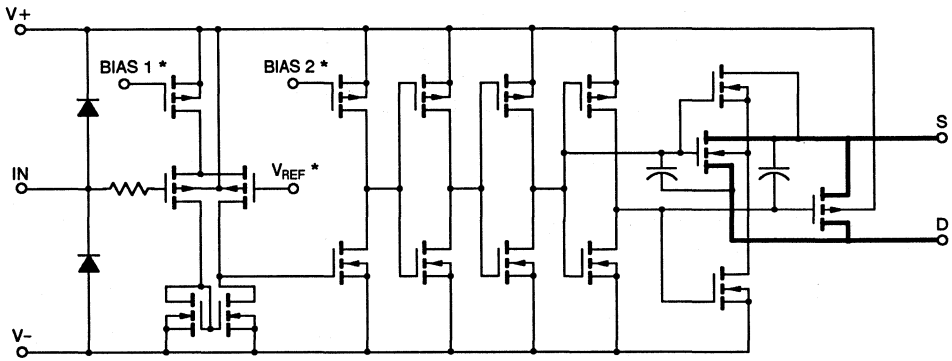
Figure 5. Source/Drain Capacitances

SCHEMATIC DIAGRAMS



* Internal Connection Only

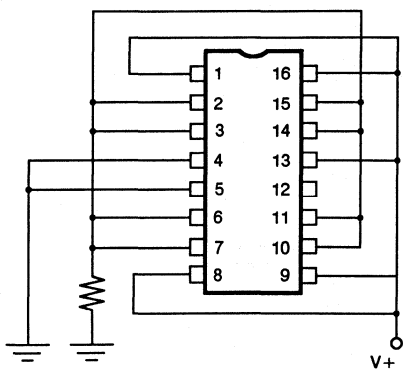
Figure 6. Regulator/Bias Circuit (Common to 4 Channels)



* Internal Connection Only

Figure 7. Typical Channel

BURN-IN CIRCUIT



Note: All resistors are 10 kΩ unless otherwise specified.
SO package is the same as the DIP.

Figure 8.

APPLICATIONS

This circuit allows data to be written to or read from the disk. In the write mode, SW_2 is closed. A "one" is created by momentarily closing SW_1. This causes current to flow on the left half of the head coil. A "zero" is produced by closing SW_3. This causes current flow on the right half of the coil and reverses the magnetic flux direction. In the read mode, switches SW_4 and SW_5 are closed. This connects the head coil to the read preamplifier so that the voltages picked up by the head as the disk glides by can be amplified.

Single-supply operation with +12 V, low on-resistance, and fast switching speed allow about a 25X improvement in data rates when DG601s are used in place of the industry standard DG211s.

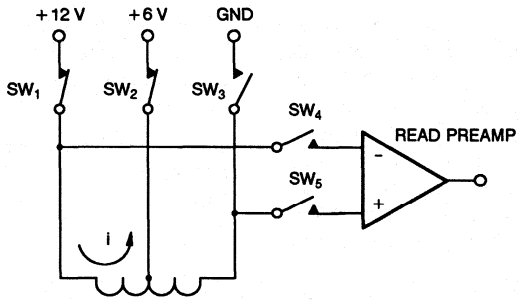


Figure 9. DG601s in the Head Switching Circuit of a Hard Disk Drive

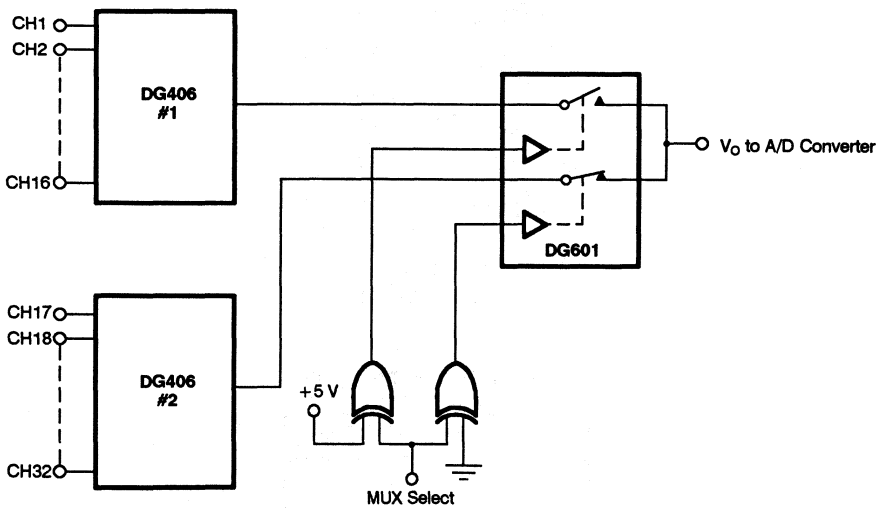


Figure 10. Super Multiplexing Improves Settling Times

5

DG5043
Monolithic General Purpose CMOS Analog Switch

Siliconix incorporated

FEATURES

- ±15 Volt Input Range
- ON-Resistance <50 Ω
- Break-Before-Make Switching
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

- Audio Switching
- Sample and Hold Circuits

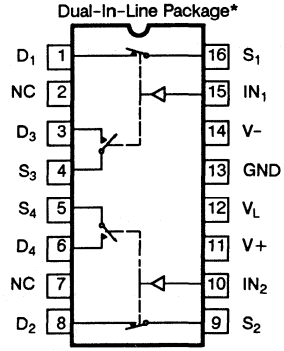
DESCRIPTION

The DG5043 solid state analog switch is recommended for general purpose applications in instrumentation, and process control. Built on the Siliconix PLUS 40 high voltage CMOS monolithic process, this device provides ease-of-use and performance advantages to the system designer. Key performance features of this device are 1 μs switching, low power supply requirements, and break-before-make switching which guarantees that an ON channel will be turned OFF before an OFF channel can turn ON. Each switch conducts equally well in either direction, when ON, and blocks up to 30 volts peak-to-peak when OFF. OFF leakage current is 1 nA maximum, and an epitaxial layer prevents latch up.

The DG5043 is available in 16-pin plastic Dip in the commercial, C suffix (0 to 70°C). For new designs, DG403/405 are recommended.

FUNCTIONAL BLOCK DIAGRAM, PIN CONFIGURATION AND TRUTH TABLE

Dual-In-Line Package*



Top View

Order Number:

Plastic: DG5043CJ

DG5043

Two SPDT Switches per Package

Truth Table*

Logic	Switch 1 Switch 2	Switch 3 Switch 4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V

Logic "1" ≥ 2.0 V

*Switches shown for logic "1" input

ABSOLUTE MAXIMUM RATINGS

V+ ..... 44 V
GND to V- ..... 25 V
V_L ..... (GND - 0.3 V) to 44 V
Digital Inputs[1] V_S, V_D ..... (V-) -2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA

Storage Temperature (C Suffix) ..... -65 to 125°C
Operating Temperature (C Suffix) ..... 0 to 70°C
Power Dissipation (Package)*
16-Pin Plastic DIP** ..... 450 mW

*All leads welded or soldered to PC board.
**Derate 6 mW/°C above 75°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2 V, 0.8 V[e]	TEMP[f]	TYP[d]	C SUFFIX 0 to 70°C MIN[b]	C SUFFIX 0 to 70°C MAX[b]	UNIT
ANALOG SWITCH							
Analog Signal Range[d]	V_{ANALOG}		Full		-15	15	V
Drain-Source ON-resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = ±10 V	Room Full			50 75	Ω
Switch OFF Leakage Current	$I_{S(OFF)}$	V_D = -14 V, V_S = 14 V	Room Full		-1 -100	1 100	nA
	$I_{D(OFF)}$	V_D = 14 V, V_S = -14 V	Room Full		-1 -100	1 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 14 V	Room Full			2 200	
		V_S = V_D = -14 V	Room Full		-2 -200		
DIGITAL CONTROL							
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full		-1	1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2 V	Full		-1	1	
DYNAMIC CHARACTERISTICS							
Turn-ON Time	t_{ON}	V_S = ±10 V R_L = 300 Ω, C_L = 35 pF	Room			1200	ns
Turn-OFF Time	t_{OFF}	See Figure 1A	Room			700	
Charge Injection[c]	Q	C_L = 10,000 pF V_{gen} = 0 V, R_{gen} = 0 Ω	Room	30			pC
OFF Isolation[c]		R_L = 75 Ω, C_L = 5 pF f = 1 MHz	Room	75			dB
Crosstalk[c] (Channel-to-Channel)		R_L = 75 Ω, V_S = 2 V_{P-P} f = 1 MHz	Room	89			
Source OFF Capacitance[c]	$C_{S(OFF)}$	V_D = V_S = 0 V f = 1 MHz	Room	15			pF
Drain OFF Capacitance[c]	$C_{D(OFF)}$		Room	17			
Channel ON Capacitance[c]	$C_{D+S(ON)}$		Room	45			

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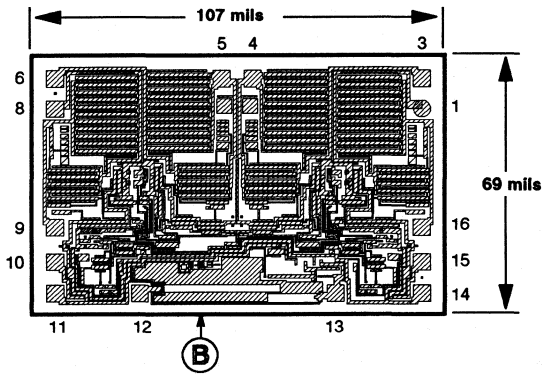
Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -15 V V_L = 5 V, V_{IN} = 2 V, 0.8 V[e]	TEMP[f]	TYP[d]	C SUFFIX 0 to 70°C MIN[b]	C SUFFIX 0 to 70°C MAX[b]	UNIT
POWER SUPPLIES							
Positive Supply Curent	I+	V_{IN} = 0 or 2.4 V	Full			300	µA
Negative Supply Current	I-		Full		-300		
Logic Supply Current	I_L		Full			300	
Ground Current	I_{GND}		Full		-300		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = input voltage to perform proper function.
f. Room = 25°C, Full = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function
1	D_1
3	D_3
4	S_3
5	S_4
6	D_4
8	D_2
9	S_2
10	IN_2
11	V+ (Substrate)
12	V_L
13	GND
14	V-
15	IN_1
16	S_1

ICMKB

6 Resistors
7 Capacitors
9 Diodes

31 p-channel Depletion MOSFETs
33 n-channel Depletion MOSFETs

TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

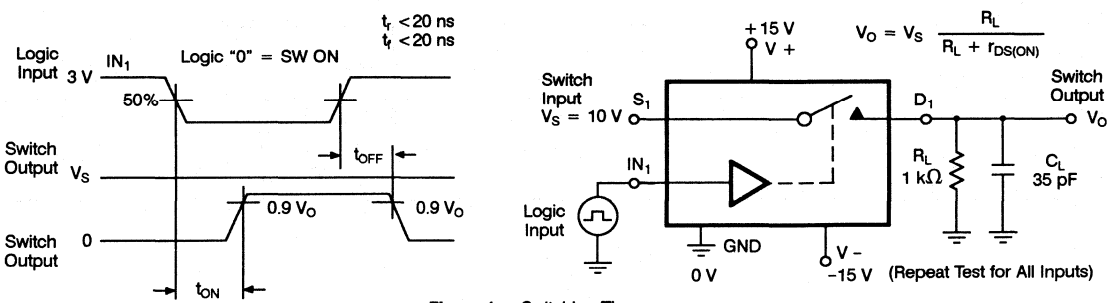
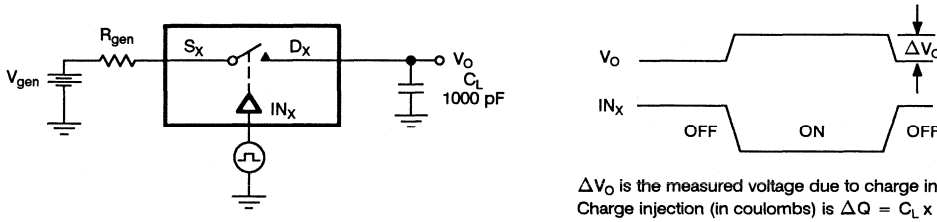


Figure 1. Switching Time

TEST CIRCUITS (Cont'd)



ΔV_O is the measured voltage due to charge injection.
Charge injection (in coulombs) is $\Delta Q = C_L \times \Delta V_O$.

Figure 2.

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

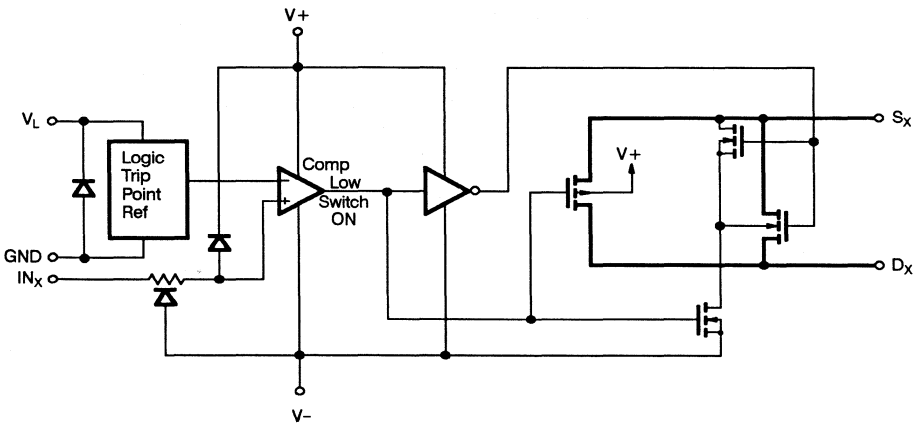


Figure 3.

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TABLE OF CONTENTS

WIDEBAND/VIDEO

INTRODUCTION

Siliconix manufactures analog switches and multiplexers for wideband/video applications using Double Diffused MOS (DMOS) technology. DMOS FETs are n-channel enhancement-mode MOSFET's which exhibit very low capacitance and ON-resistance, compared to conventional CMOS devices. The result is wide bandwidth switches, from discretes such as the SD210 and SD5000 families, through D/CMOS "T" switches and multiplexers which feature crosstalk and off isolation performance as high as 100 dB at 5 MHz and 3 dB bandwidths in excess of 500 MHz. These devices are ideal for broadcast video, digital data routing, high end workstation networks and imaging applications from medical to military.

DMOS Switch Arrays

The SD500X and SD540Xs are monolithic arrays of four DMOS FETs without drivers. Their low capacitance and low ON-resistance make them ideal for high speed wideband switching and sampling applications. These data sheets can be found in the Low Power Discrete data book.

D/CMOS "T" Switches

The DG54X family of wideband/video "T" switches includes the DG540, DG541 and DG542 devices. The DG540 and DG541 are quad SPST switches, and the DG542 is a dual SPDT (or dual changeover) function. The DG540 employs interstitial ground lines between adjacent channels to achieve improved isolation and reduced crosstalk. The DG541 uses the standard DG201A pin-out, hence has slightly inferior performance than the DG540, but is available in a lower cost, smaller package. Each of these switches uses DMOS "T" switches for fast switching, wide bandwidths and excellent isolation.

D/CMOS Wideband/Video Multiplexers

The DG535 and DG536 are 16-channel wideband/video multiplexers which use the Siliconix D/CMOS process to combine wideband DMOS "T" switches with high density, high speed CMOS logic and switch drivers to form complete monolithic wideband/video multiplexing systems. These devices include on-board latches to hold the address selection data and all of the necessary control logic to facilitate connection into larger arrays, matrices and multiplexers. The DG534 and DG538 are 4- and 8-channel wideband/video multiplexers which, like the DG535 and DG536, feature address latches and control logic with the addition of data readback and TTL-compatibility. They make excellent wideband/video crosspoints, routers, and multiplexers, reducing board space, power dissipation, component count and cost while simplifying system design and improving reliability.

For detailed information on these products please refer to their individual data sheets and to application notes LPD-10, AN86-1, and AN88-2.

Crosspoints

The DG884 is the first monolithic wideband/video crosspoint switch available for commercial use. Any of eight video inputs can simultaneously be routed to any of four outputs. This highly integrated device offers a major reduction on the physical size and component count needed to implement a video switching matrix. The DG884 utilizes double-diffused (DMOS) switching elements to maintain low capacitances and low levels of crosstalk among signal paths.

Double-differed CMOS latches, chip select, reset, readback and disable functions are all included on-chip to ease system design, save power and improve system reliability.

Video Buffers and Amplifiers

To complement the wideband/video switching product line Siliconix offers the Si581 video buffer and the Si582 video amplifier. These two devices are built on an advanced complementary bipolar process and offer bandwidths of 450 MHz and 200 MHz, respectively. Their excellent bandwidths and low power dissipation make the Si581 and Si582 ideal for high-end applications such as broadcast video, color workstations, medical- and infrared-imaging, etc.

GLOSSARY OF TERMS

Bandwidth

The "3 dB down" point of the frequency response characteristic.

Crosspoint Switch

A two-dimensional array of analog switches or analog multiplexers that allows for the routing of signals from any input to any output.

Crosstalk

A measure of how much of an unwanted signal appears on a given analog channel due to spurious capacitive or inductive coupling from another channel.

D/CMOS

Semiconductor process that combines DMOS FETs and CMOS logic on a monolithic chip.

Differential Gain

Expressed as a percentage, this is a form of distortion that appears as changes in the amplitude of the chrominance (color) signal as a function of luminance (brightness) amplitude.

Differential Multiplexer

Analog multiplexer that selects both the high and the low side of each signal. It can be thought of as two single-ended multiplexers operating in tandem.

Differential Phase

Measured in degrees is the phase shift of the color subcarrier resulting from changes in luminance level.

DMOS

(Double Diffused MOS) Type of field effect transistor featuring low $r_{DS(ON)}$ and low capacitance.

Input Capacitance

Capacitive load that the input terminal of an analog switch presents to the signal source. It is specified both with the switch ON or OFF.

Insertion Loss

Expressed in dB, is a measure of the signal loss caused by the impedance of the analog switch at a given frequency.

Off Isolation

A measure of how much of the signal applied to an "open" switch appears at its output due to parasitic components such as gate-to-channel capacitance and lead inductances.

ON-Resistance

DC input-to-output resistance of an analog switch channel when the switch is turned ON.

Output Capacitance

Capacitive load that the output of an OFF switch adds to the output node.

PLCC Package

Plastic leaded chip carrier. Surface mount package characterized for its small size and reliable lead-to-printed circuit board mechanical interface.

Readback

Feature that allows for the inspection of the control latch contents in a multiplexer or crosspoint switch.

Single Ended Multiplexers

Array of analog switches that selects one of several analog input signals.

"T" Switch

Analog switch configuration consisting of two series switches and a shunt switch to ground. It is used to dramatically improve the off-isolation of the array.

Video

Electrical signals carrying dynamic visual information.

Video Amplifier

An amplifier, typically with a gain of two, which is normally used at the output of a video multiplexer or crosspoint to drive a length of double terminated coaxial cable.

Video Buffer

A current amplifier whose function is to preserve signal quality by eliminating the capacitive loading effect of several video multiplexer inputs on a common signal source. This is normally a unity gain buffer.

Wideband

A relative term, as used in this book it refers to a frequency spectrum at least more than 2 MHz wide.

Siliconix incorporated

DG534/538
Dual 4-Channel/8-Channel Wideband/Video Multiplexers

FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk (–97 dB @ 5 MHz)
- On-Board TTL-Compatible Latches with Readback
- Optional Negative Supply Input
- Low $r_{DS(ON)}$ (90 Ω max)
- Single-Ended or Differential Operation

BENEFITS

- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- Allows Differential Signal Switching

APPLICATIONS

- Wideband Signal Routing and Multiplexing
- HDTV Systems
- µP-Controlled Systems
- Direct Coupled Systems
- ATE Systems
- Infrared Imaging

DESCRIPTION

The DG534 is a digitally selectable 4-channel or dual 2-channel multiplexer. The DG538 is an 8-channel or dual 4-channel multiplexer. These analog multiplexers/demultiplexers are designed for wideband operation. On-chip TTL-compatible address decoding logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low ON-resistance and low capacitance of the these devices make them ideal for wideband data multiplexing and video and audio signal routing in channel selectors and crosspoint arrays. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

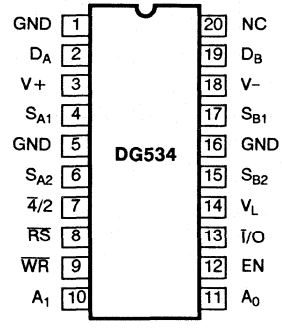
The DG534/DG538 are built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of OFF isolation. Crosstalk is reduced to –97 dB at 5 MHz by including a ground line between each adjacent signal path.

The DG534/DG538 are available in plastic DIP and PLCC packages for operation over the industrial, D suffix (–40 to 85°C) temperature range. The side braze DIP is available for military, A suffix (–55 to 125°C) temperature range operation.

For more information refer to Siliconix Applications Note AN88-2.

PIN CONFIGURATIONS

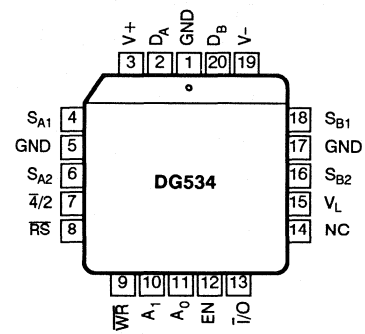
Dual-In-Line Package
Top View



Order Numbers:

Side Braze: DG534AP, DG534AP/883
Plastic: DG534DJ

PLCC Package
Top View



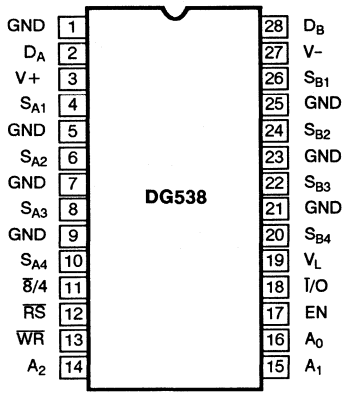
Order Number:

DG534DN

6

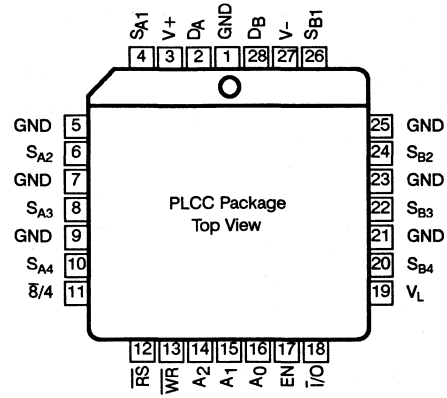
PIN CONFIGURATIONS (Cont'd)

Dual-In-Line Package
Top View



Order Numbers:

Side Braze: DG538AP, DG538AP/883
Plastic: DG538DJ

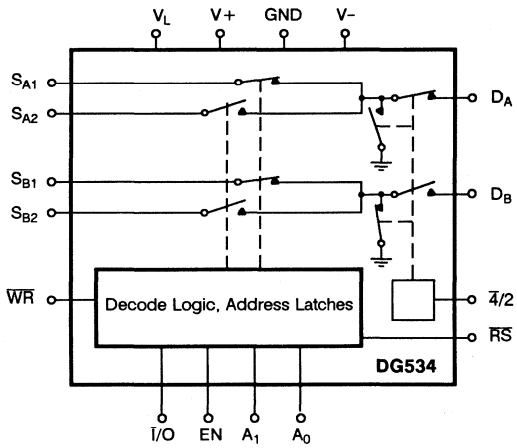


Order Number:

DG538DN
Quad J-Lead
Plastic Chip Carrier

FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

All input switches are "T" switches.

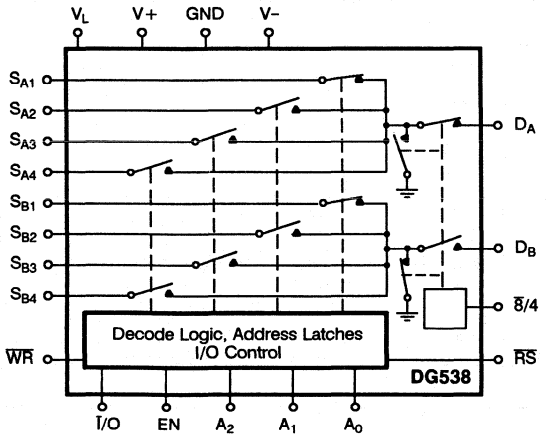


I/O	A_0	A_1	EN	WR	RS	4/2*	ON Switch	
X	X	X	X	↓	1	1	Maintains previous state	
X	X	X	X	X	0	X	None (latches cleared)	
X	X	X	0	0	1	X	None	
0	0	0	1	0	1	0	S_{A1}	DA & DB may be connected externally; Latches Transparent
0	0	1	1	0	1	0	S_{A2}	
0	1	0	1	0	1	0	S_{B1}	
0	1	1	1	0	1	0	S_{B2}	
0	X	0	1	0	1	1	S_{B1} & S_{B1}	
0	X	1	1	0	1	1	S_{B2} & S_{B2}	
1	Note 2		1	1	1	Note 1		

Logic "1": $V_{AH} \geq 2.0$ V
Logic "0": $V_{AL} \geq 8.0$ V

*D_A and D_B must be connected together externally if single-ended operation is desired.

FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES (Cont'd)



I/O	A_0	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	$\overline{8}/4$*	ON Switch
X	X	X	X	X	⌐	1	1	Maintains previous state
X	X	X	X	X	X	0	X	None (latches cleared)
X	X	X	X	0	0	1	X	None
0	0	0	0	1	0	1	0	S_{A1}
0	0	0	1	1	0	1	0	S_{A2}
0	0	1	0	1	0	1	0	S_{A3}
0	0	1	1	1	0	1	0	S_{A4}
0	1	0	0	1	0	1	0	S_{B1}
0	1	0	1	1	0	1	0	S_{B2}
0	1	1	0	1	0	1	0	S_{B3}
0	1	1	1	1	0	1	0	S_{B4}
0	X	0	0	1	0	1	1	S_{B1} & S_{B1}
0	X	0	1	1	0	1	1	S_{B2} & S_{B2}
0	X	1	0	1	0	1	1	S_{B3} & S_{B3}
0	X	1	1	1	0	1	1	S_{B4} & S_{B4}
1	Note 2			1	1	1	Note 1	

DA & DB should be connected externally

Latches Transparent

*D_A and D_B must be connected externally if single-ended operation is desired.

NOTES:
1. $\overline{4}/2$ or $\overline{8}/4$ can be either H or L but should not change during these operations.
2. With $\overline{I}/O$ high, A_n pins become outputs and reflect the contents of the latches. See timing diagrams for more detail.

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3 V to +21 V
V+ to V- ..... -0.3 V to +21 V
V- to GND ..... -10 V to +0.3 V
V_L ..... 0 V to (V+) + 0.3 V
Digital Inputs ..... (V-) -0.3 V to (V+) + 0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V-) -0.3 V to (V-) + 21V
or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current(S or D) Pulsed I ms 10% Duty ..... 40 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 150°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)
Plastic DIP** ..... 625 mW
Side Braze DIP*** ..... 1200 mW
Quad J Lead Plastic**** ..... 450 mW

*All leads welded or soldered to PC board.
**Derate 8.3 mW/°C above 75°C.
***Derate 16 mW/°C above 75°C.
****Derate 6 mW/°C above 75°C.

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SPECIFICATIONS[a]

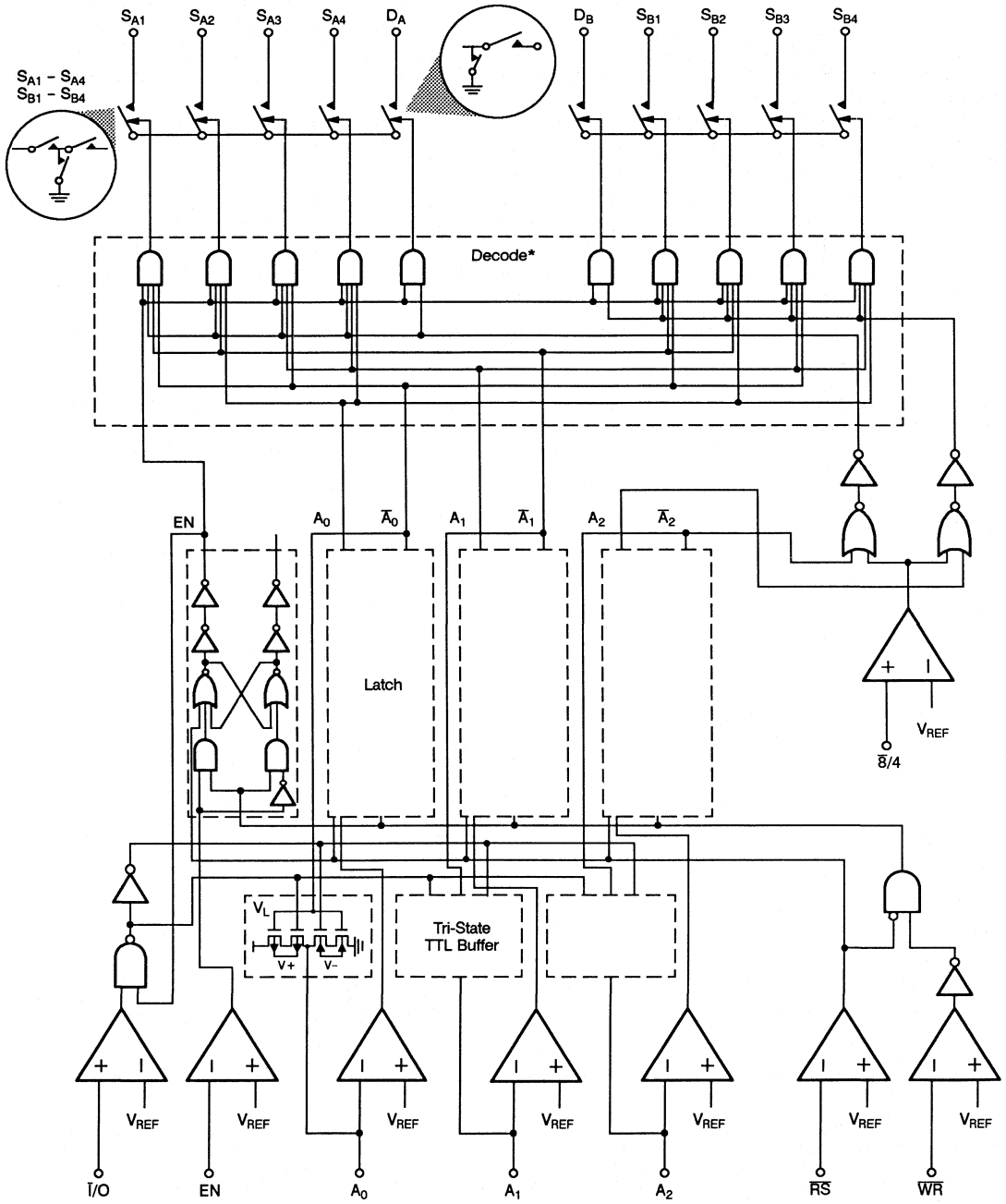
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V, V_L = 5 V, $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH										
Analog Signal Range[e]	V_{ANALOG}	V- = -5 V		Full		-5	8	-5	8	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_S = 0 V V_{AIL} = 0.8 V, V_{AIH} = 2 V		Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(ON)}$	Sequence Each Switch ON		Room			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 8 V, V_D = 0 V EN = 0.8 V		Room Full		-5 -50	5 50	-5 -50	5 50	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = 0 V, V_D = 8 V EN = 0.8 V		Room Full		-20 -500	20 500	-20 -100	20 100	
Drain ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 8 V		Room Full		-20 -1000	20 1000	-20 -200	20 200	
DIGITAL CONTROL										
Input Voltage High	V_{AIH}			Full		2		2		V
Input Voltage Low	V_{AIH}			Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V, or 2 V or 15 V		Room Full	-0.1	-1 -10	1 10	-1 -10	1 10	µA
Address Output Current[f]	I_{AO}	V_{AO} = 2.7 V		Room	-300					
		V_{AO} = 0.4 V		Room	300					
DYNAMIC CHARACTERISTICS										
ON State Input Capacitance[c]	$C_{S(ON)}$	See Figure 11	PLCC DIP	Room	23 27		35		30 35	pF
OFF State Input Capacitance[c]	$C_{S(OFF)}$	See Figure 12	PLCC DIP	Room	2 3		5		4 5	
OFF State Output Capacitance[c]	$C_{D(OFF)}$		PLCC DIP	Room	4 6		10		8 10	
Transition Time	t_{TRANS}	See Figure 4		Room Full			300 500		300 500	ns
Break-Before-Make Interval	t_{OPEN}			Full		50		50		
EN, $\overline{WR}$ Turn ON Time	t_{ON}	See Figure 2 and 3		Room Full			300 500		300 500	
EN, Turn OFF Time	t_{OFF}	See Figure 2		Room Full			150 300		150 300	
Charge Injection	Qi	See Figure 8		Room	-70					pC
Chip Disabled Crosstalk (See Figure 8)	$X_{TALK(CD)}$	R_L = 75 Ω f = 5 MHz EN = 0.8 V	PLCC DIP	Room	-75 -65					dB
Adjacent Input Crosstalk (See Figure 9)	$X_{TALK(AI)}$	R_{IN} = 10 Ω R_L = 10 Ω f = 5 MHz	PLCC DIP	Room	-97 -87					
		R_{IN} = 75 Ω R_L = 75 Ω f = 5 MHz	PLCC DIP	Room	-80 -70					

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V, V_L = 5 V, $\overline{WR}$ = 0.8 V, $\overline{RS}$, EN = 2 V		TEMP[h]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
DYNAMIC CHARACTERISTICS (Cont'd)										
All Hostile Crosstalk (See Figure 9)	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 Ω, f = 5 MHz	PLCC DIP	Room	-77 -72					dB
		R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz	PLCC DIP	Room	-77 -72					
Differential Crosstalk (See Figure 9)	$X_{TALK(DIFF)}$	R_{IN} = 10 Ω, R_L = 10 Ω, f = 5 MHz		Room	-84					
		R_{IN} = R_L = 75 Ω, f = 5 MHz		Room	-84					
Bandwidth	BW	R_L = 50 Ω, See Figure 6		Room	500					MHz
POWER SUPPLIES										
Positive Supply Current	I+	Any One Channel Selected with Address Inputs at GND or V+		Room Full	0.6		2 5		2 5	mA
Negative Supply Current	I-			Room Full	0.6	-1.8 -2		-1.8 -2		
Functional Check of Maximum Operating Supply Voltage Range	V+ to V-	Functional Test Only		Full		10	21	10	21	V
	V- to GND			Full		-5.5	0	-5.5	0	
	V+ to GND			Full		10	21	10	21	
Logic Supply Current	I_L			Full	150		500		500	µA
TIMING										
Reset to Write	t_{RW}	See Figure 1		Full		50		50		ns
$\overline{WR}$, $\overline{RS}$ Minimum Pulse Width	t_{MPW}			Full		200		200		
A_0, A_1, EN Data Valid to Strobe	t_{DW}			Full		100		100		
A_0, A_1, EN Data Valid after Strobe	t_{WD}			Full		50		50		
Address Bus Tri-state[g]	t_{AZ}			Room	50					
Address Bus Output	t_{AO}			Room	200					
Address Bus Input	t_{AI}			Room	200					

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY at 25°C, not guaranteed nor subject to production testing.
e. Analog signal range is measured from the GND pin to the designated Source (Input) pin, and indicates the limits of functionality. Performance limits are only guaranteed for states test conditions.
f. Each individual pin shown as GND must be grounded.
g. Defined by system bus requirements.
h. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

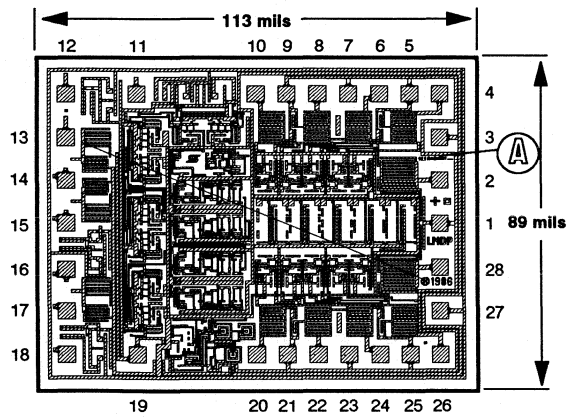
CONTROL CIRCUITRY



Note: V_{REF} is internally generated from V_L.

* Decode section includes delay circuitry in AND gating to ensure proper break-before-make operation.

DIE TOPOGRAPHY



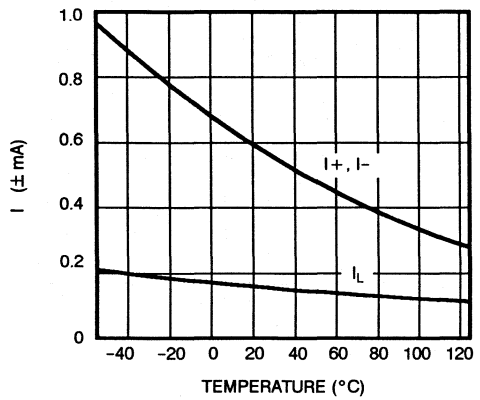
Pad No.	Function	Pad No.	Function
1	GND	15	A_1
2	D_A	16	A_0
3	V+	17	EN
4	S_{A1}	18	$\overline{I}/O$
5	GND	19	V_L
6	S_{A2}	20	S_{B4}
7	GND	21	GND
8	S_{A3}	22	S_{B3}
9	GND	23	GND
10	S_{A4}	24	S_{B2}
11	$\overline{8}/4$	25	GND
12	$\overline{RS}$	26	S_{B1}
13	$\overline{WR}$	27	V- (Substrate)
14	A_2	28	D_B

LNDPA

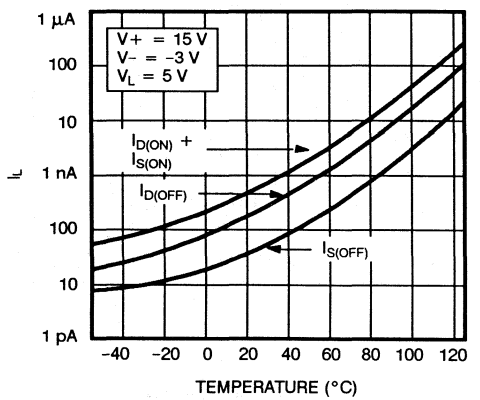
222 PMOS Transistors
243 NMOS Transistors
1 NPN Transistor
3 P + Resistors
18 Diodes

TYPICAL CHARACTERISTICS

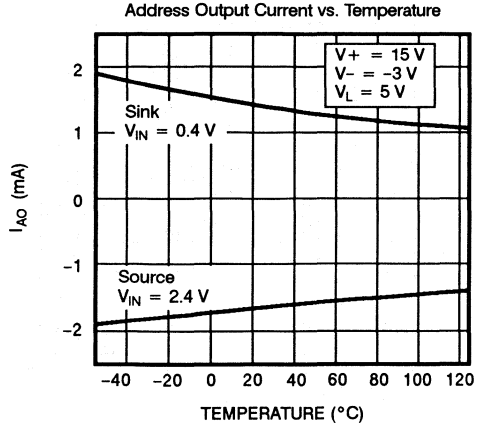
Supply Currents vs. Temperature



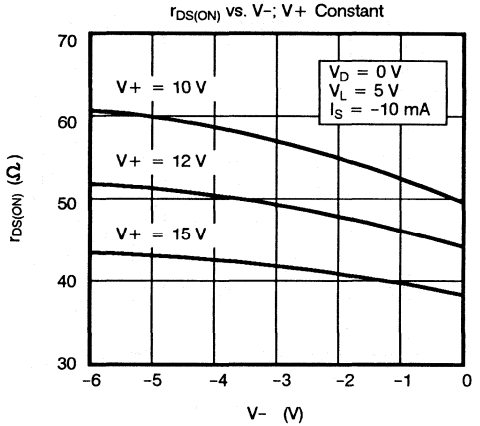
Leakage vs. Temperature



Address Output Current vs. Temperature



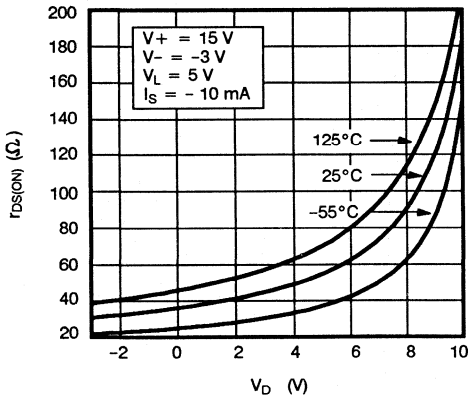
$r_{DS(ON)}$ vs. V-; V+ Constant



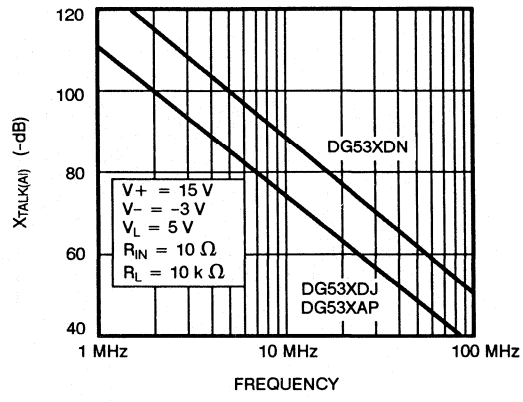
6

TYPICAL CHARACTERISTICS (Cont'd)

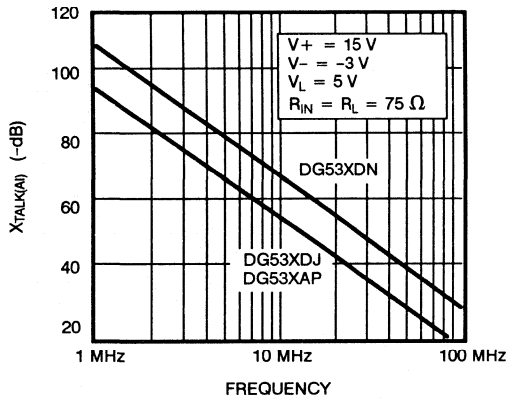
$r_{DS(ON)}$ vs. Drain Voltage



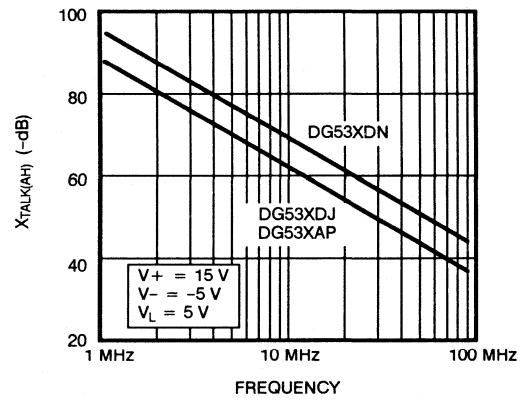
Adjacent Input Crosstalk



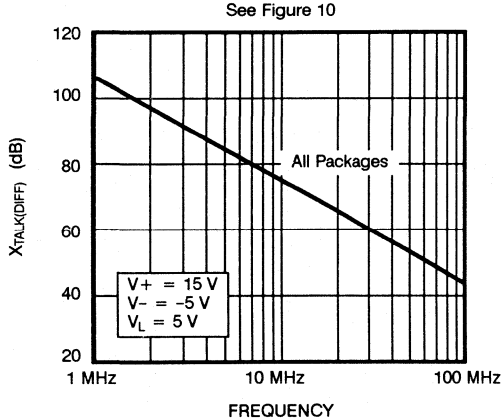
Adjacent Input Crosstalk
See Figure 9



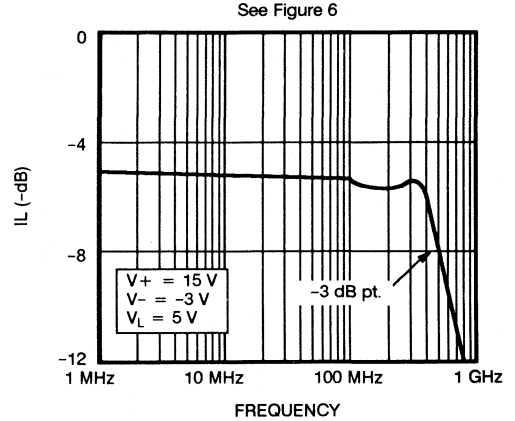
All Hostile Crosstalk
See Figure 7



Differential Crosstalk
See Figure 10

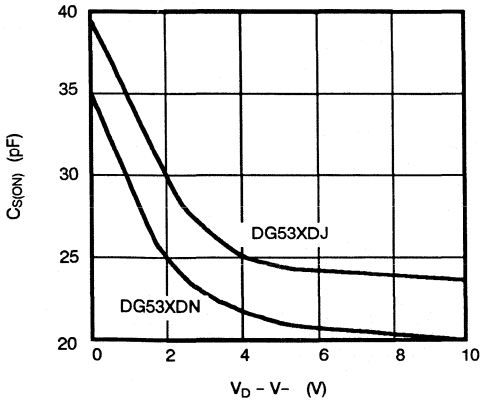


Insertion Loss
See Figure 6

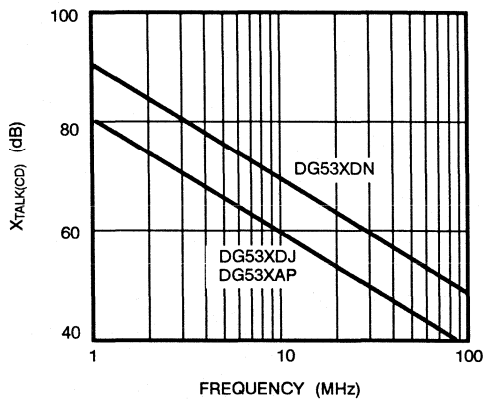


TYPICAL CHARACTERISTICS (Cont'd)

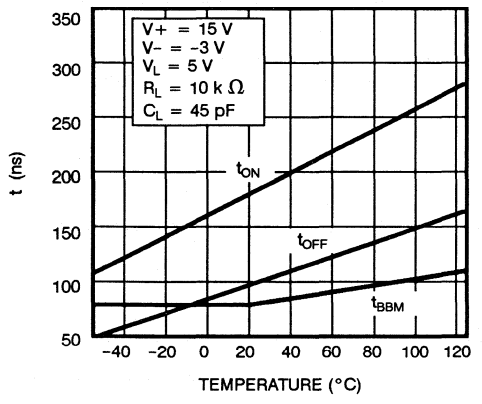
ON State Capacitance
See Figure 11



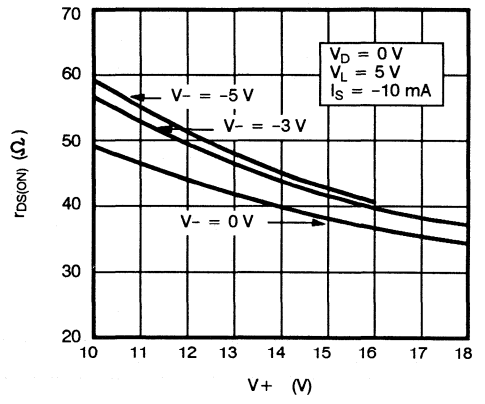
Chip Disabled Crosstalk
See Figure 8



Switching Times vs. Temperature

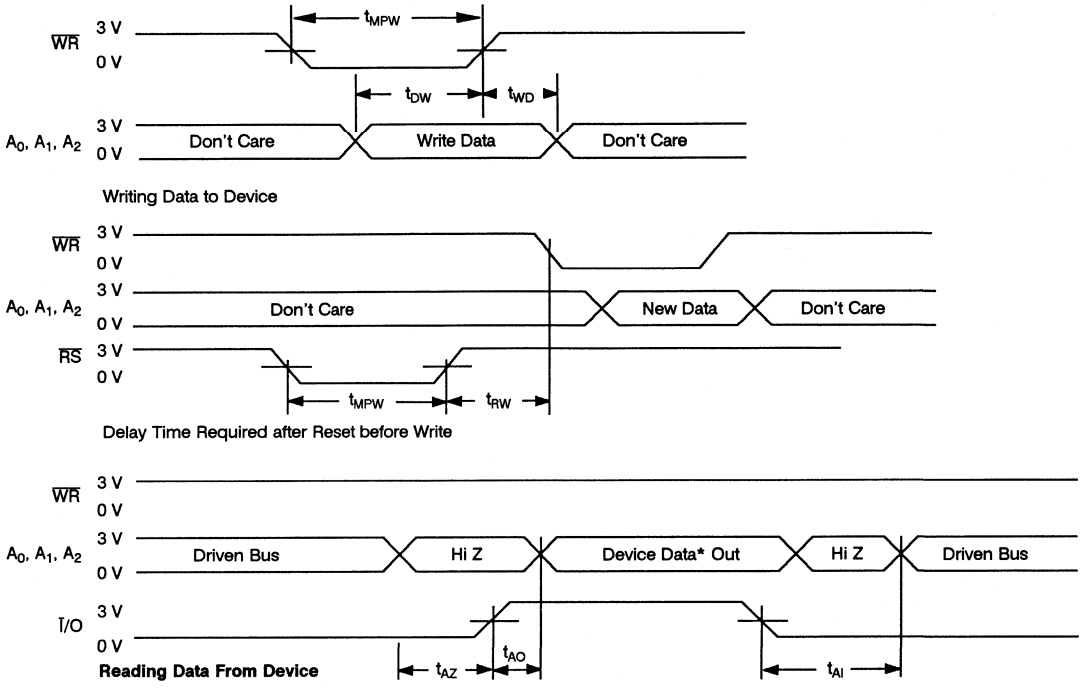


$r_{DS(ON)}$ vs. V+; V- Constant



6

INPUT TIMING REQUIREMENTS



*Enable must be latched "High" to read back data, otherwise BUS is high Z. V- ≤ -3 V required for readback functionality.

Figure 1.

TEST CIRCUITS

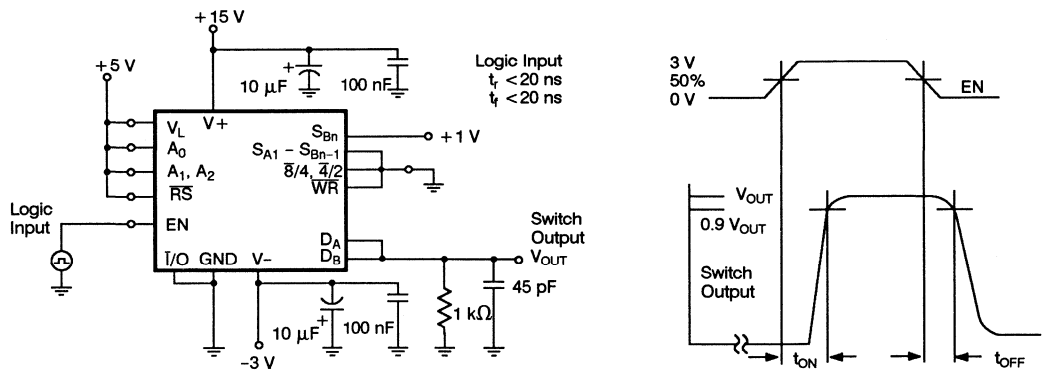


Figure 2. EN, CS, $\overline{CS}$, Turn ON/OFF Time

TEST CIRCUITS (Cont'd)

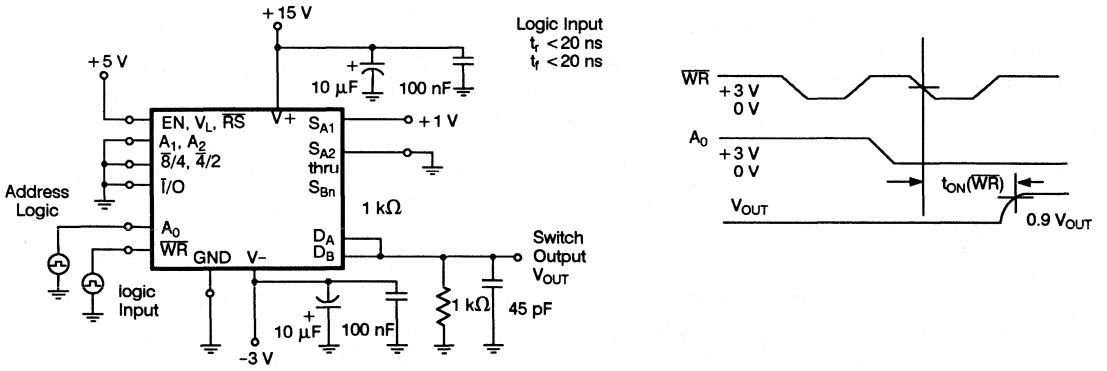


Figure 3. WR, Turn ON Time

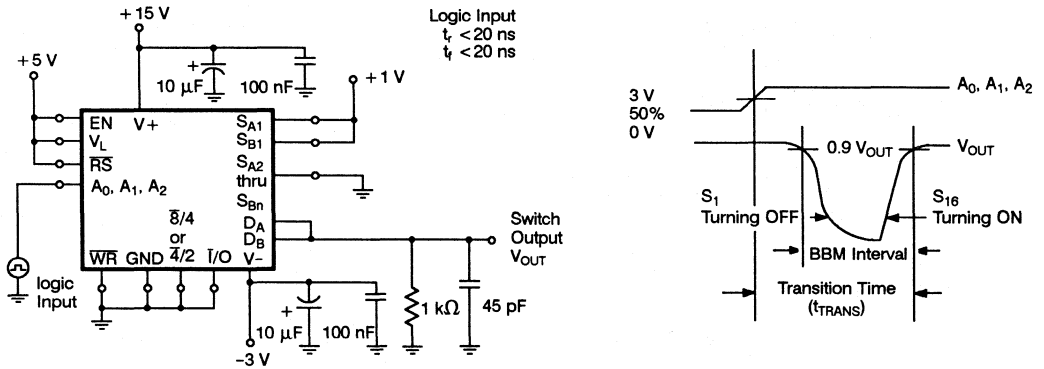
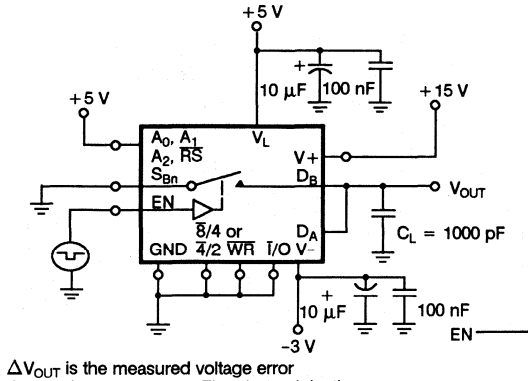


Figure 4. Transition Time and Break-before-make Interval

6



ΔV_{OUT} is the measured voltage error due to charge injection. The charge injection in Coulombs is $Q = C_L \times \Delta V_{OUT}$

Figure 5. Charge Injection

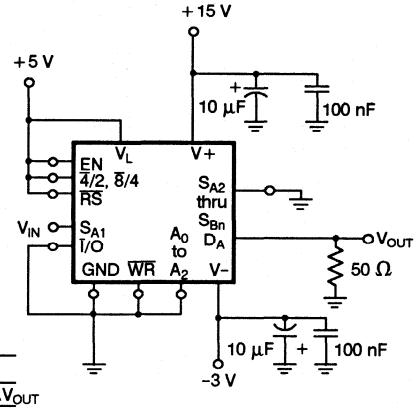


Figure 6. Bandwidth

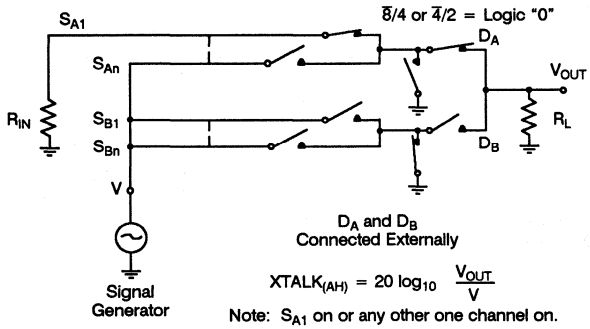


Figure 7. All Hostile Crosstalk

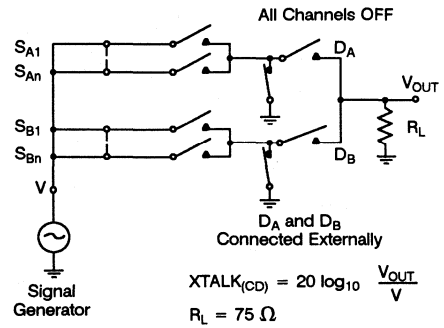


Figure 8. Chip Disabled Crosstalk

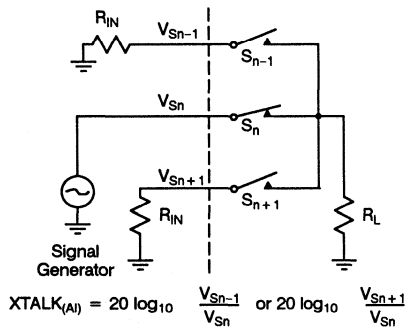


Figure 9. Adjacent Input Crosstalk

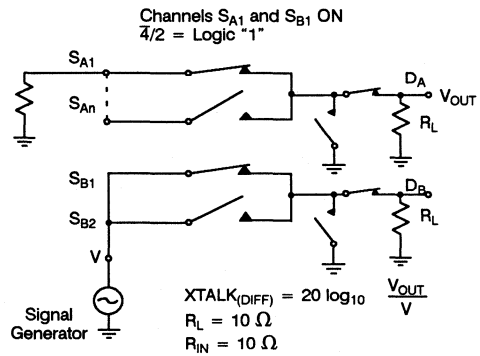


Figure 10. Differential Crosstalk

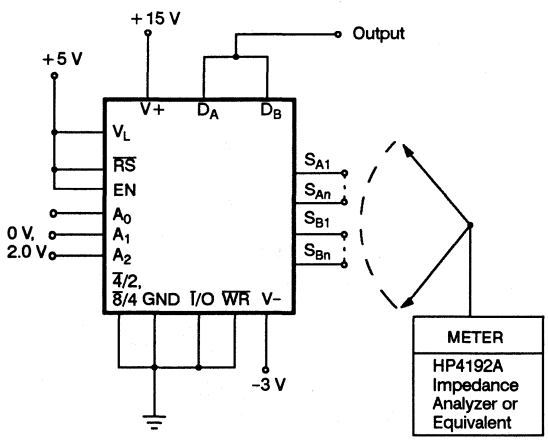


Figure 11. ON State Input Capacitance

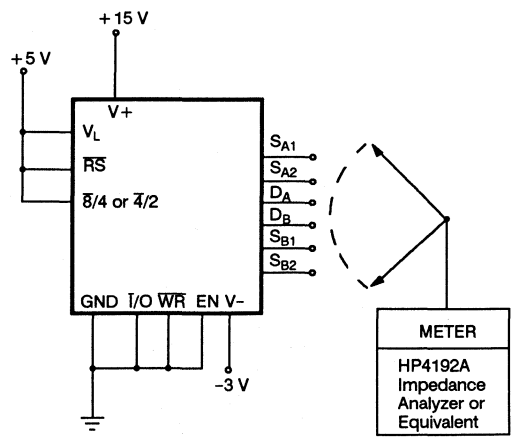
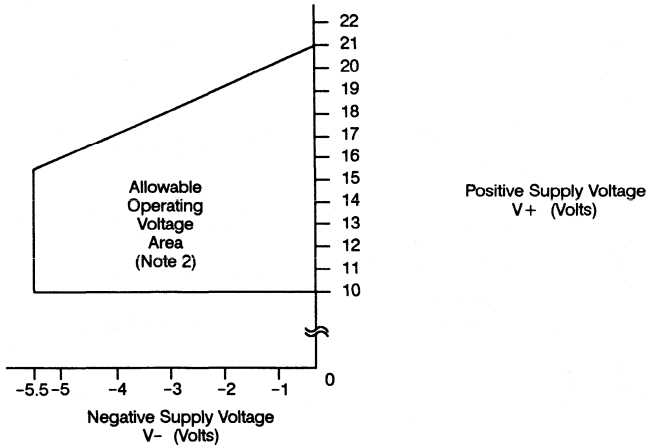


Figure 12. OFF State Input/Output Capacitance

OPERATING VOLTAGE RANGE



Notes:
1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10 µF tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V.
3. At V_L = 5 V ±10%, 0.8/2.0 TTL compatibility is maintained over the entire operating voltage range.

Figure 13.

BURN-IN CIRCUITS

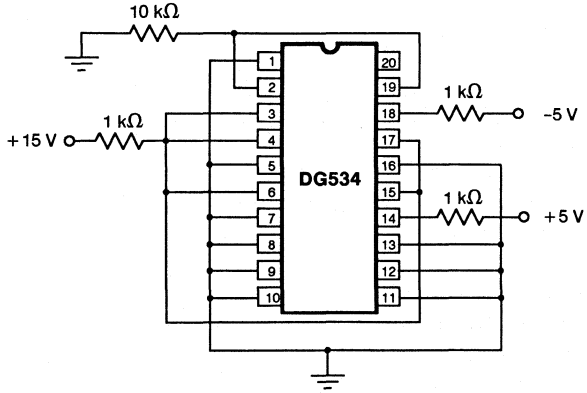


Figure 14. DG534 - 20-Lead Dual-In-Line

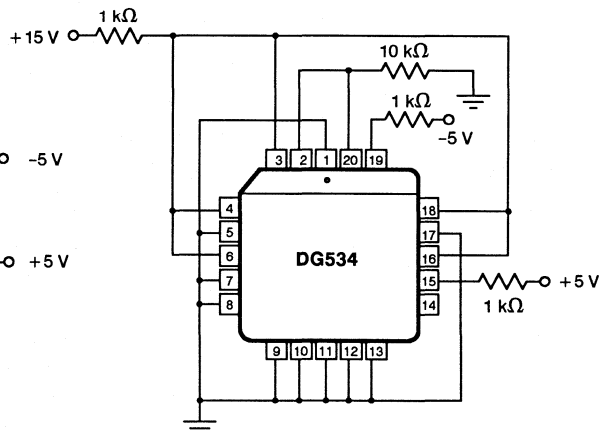


Figure 15. DG534 - 20-Lead PLCC

BURN-IN CIRCUITS (Cont'd)

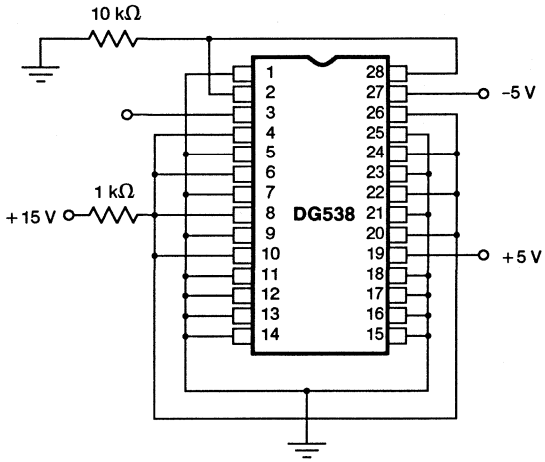


Figure 16. DG538 - 28-Lead Dual-In-Line

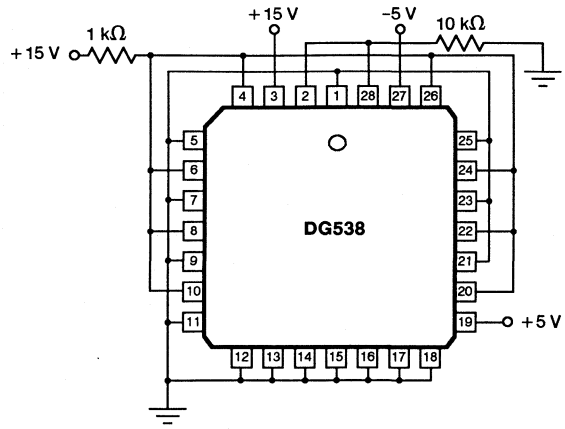


Figure 17. DG538 - 28-Lead PLCC

PIN DESCRIPTION

SYMBOL	DG534 PIN NUMBER	DG538 PIN NUMBER	DESCRIPTION
D_A	2	2	Analog Output/Input
V+	3	3	Positive Supply Voltage
S_{A1}	4	4	Analog Input/Output
S_{A2}	6	6	Analog Input/Output
S_{A3}	-	8	Analog Input/Output
S_{A4}	-	10	Analog Input/Output
$\overline{4}/2$	7	-	4 x 1 or 2 x 2 Select
$\overline{8}/4$	-	11	8 x 1 or 4 x 2 Select
$\overline{RS}$	8	12	Reset
$\overline{WR}$	9	13	Write command that latches A, EN
A_0, A_1, A_2	11, 10, -	16, 15, 14	Binary address inputs that determine which channel(s) is/are connected to the output(s)
EN	12	17	Enable. If EN = 0, all channels are open
$\overline{I}$/O	13	18	Input/Output control. Used to write to or read from the address latches
V_L	14	19	Logic Supply Voltage, usually +5 V
S_{B4}	-	20	Analog Input/Output
S_{B3}	-	22	Analog Input/Output
S_{B2}	15	24	Analog Input/Output
S_{B1}	17	26	Analog Input/Output
V-	18	27	Negative Supply Voltage
D_B	19	28	Analog Output/Input
GND	1, 5, 16	1, 5, 7, 9, 21, 23, 25	Analog and Digital Grounds. All grounds should be connected externally to optimize dynamic performance

Device Description

The DG534/538 D/CMOS wideband multiplexers offer single-ended or differential functions. A $\overline{8}/4$ or $\overline{4}/2$ logic input pin selects the single-ended or dual mode.

To meet the high dynamic performance demands of video, high definition TV, digital data routing (in excess of 100 Mbps), etc., the DG534/538 are fabricated with DMOS transistors configured in 'T' arrangements with second level 'L' configurations (see Functional Block Diagram).

Use of DMOS technology yields devices with very low capacitance and low $r_{DS(ON)}$. This directly relates to improved high frequency signal handling and higher switching speeds, while maintaining low insertion loss figures. The 'T' and 'L' switch configurations further improve dynamic performance by greatly reducing crosstalk and output node capacitances.

Frequency Response

A single multiplexer on-channel exhibits both resistance ($r_{DS(ON)}$) and capacitance ($C_{S(ON)}$). This RC combination causes a frequency dependent attenuation of the analog signal. The -3 dB bandwidth of the DG534/538 is typically 500 MHz (into 50 Ω). This figure of 500 MHz illustrates that the switch-channel cannot be represented by a simple RC combination. The ON capacitance of the channel is distributed along the ON resistance, and hence becomes a more complex multi-stage network of R's and C's making up the total $r_{DS(ON)}$ and $C_{S(ON)}$.

Power Supplies and Decoupling

A useful feature of the DG534/538 is its power supply flexibility. It can be operated from unipolar supplies (V- connected to 0 V) if required. Allowable operating voltage ranges are shown in Figure 13.

Note that the analog signal must not go below V- by more than 0.3 V (see absolute maximum ratings). However, the addition of a V- pin has a number of advantages:

1) It allows flexibility in analog signal handling, i.e. with V- = -5 V and V+ = 15 V, up to ±5 V ac signals can be accepted.

2) The value of ON capacitance ($C_{S(ON)}$) may be reduced by increasing the reverse bias across the internal FET body to source junction. For more information see curve of $C_{S(ON)}$ versus (V_D minus V-) voltage in typical characteristic data section. V+ has no effect on $C_{S(ON)}$.

   It is useful to note that tests indicate that optimum video differential phase and gain occur when V- is -3 V.

3) V- eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG534/538 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

(a) Decoupling capacitors should be incorporated on all power supply pins (V+, V-, V_L).

(b) They should be mounted as close as possible to the device pins.

(c) Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable.

Recommended decoupling capacitors are 1 to 10 µF tantalum bead, in parallel with 100 nF ceramic or polyester.

(d) Additional high frequency protection may be provided by 51 Ω carbon film resistors connected in series with the power supply pins (see Figure 18).

Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG534/538. Some tips for minimizing stray effects are:

i) Use extensive ground planes on double sided PCB separating adjacent signal paths. Multilayer PCB is even better.

ii) Keep signal paths as short as practically possible with all channel paths of near equal length.

iii) Use strip-line layout techniques.

Slight improvements in performance can be obtained by using PLCC parts in preference to DIPs. The stray effects of the quad PLCC package are lower than those of the dual-in-line packages.

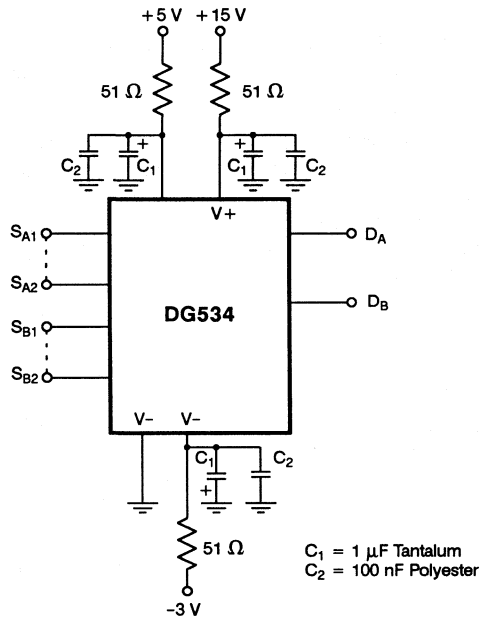


Figure 18. DG534 Power Supply Decoupling

Interfacing

Logic interfacing is easily accomplished. Comprehensive addressing and control functions are incorporated in the design.

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

A typical switching threshold versus V_L is shown in Figure 19.

These devices feature an address readback (Tally) facility, whereby the last address written to the device may be output to the system. This allows improved status monitoring and hand shaking without additional external components.

This function is controlled by the $\overline{I}$/O pin, which directly addresses the tri-state buffers applied to the address inputs (A_0 - A_2). Address inputs can be assigned to accept data (when $\overline{I}$/O = 0; $\overline{WR}$ = 0; $\overline{RS}$ = 1) or output data (when $\overline{I}$/O = 1; $\overline{WR}$ = 1; $\overline{RS}$ = 1) or reflect a high impedance and latched state (when $\overline{I}$/O = 0; $\overline{WR}$ = 1; $\overline{RS}$ = 1).

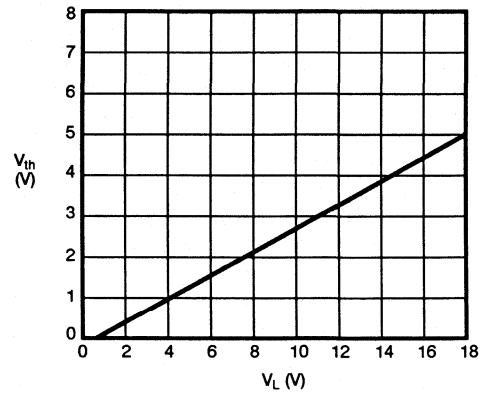


Figure 19. Switching Threshold Voltage vs. V_L

Note: (EN) must have been latched HIGH to allow proper readback, otherwise readback is suppressed.

When the $\overline{I}$/O assigns the address output condition, the address output can sink or source current for logic low and high respectively. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Note: To protect against latchup V_L must not exceed V+ by more than 0.3 V. This is easily achieved by generating V_L from V+ using a Zener or a resistor divider network as shown in Figure 20. When an external V_L is available the alternative simple protection circuit shown in Figure 21 should be used to prevent triggering the parasitic SCR during power up. The DG53XA now in development will not require these protection diodes.

Further control pins facilitate easy microprocessor interface. On chip address, data latches are activated by $\overline{WR}$, which serves as a strobe type function eliminating the need for peripheral latch or memory I/O port devices. Also, for ease of interface, a direct reset function ($\overline{RS}$) allows all latches to be cleared and switches opened. Reset should be used during power up, etc., to avoid spurious switch action. See Figure 22.

APPLICATIONS (Cont'd)

Channel address data can only be entered during $\overline{WR}$ low, when the address latches are transparent and $\overline{I}$/O is low. Similarly, address readback is only operational when $\overline{WR}$ and $\overline{I}$/O are high.

The Siliconix Si582 Video amplifier is recommended as an output buffer to reduce insertion loss and to drive coaxial cables. For low power video routing applications or for unity gain input buffers Siliconix Si581 is recommended.

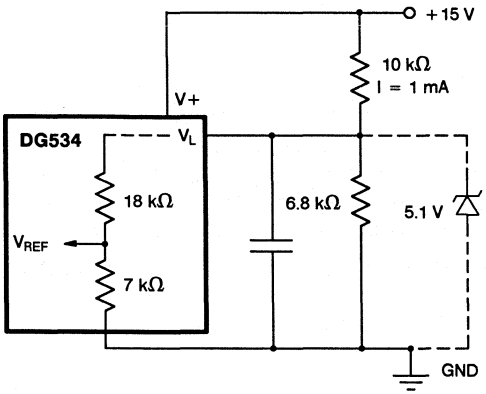


Figure 20. V_L Generated from V+

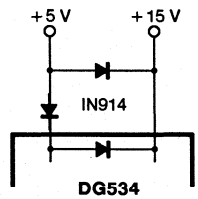


Figure 21. External Diodes Prevent Latchup

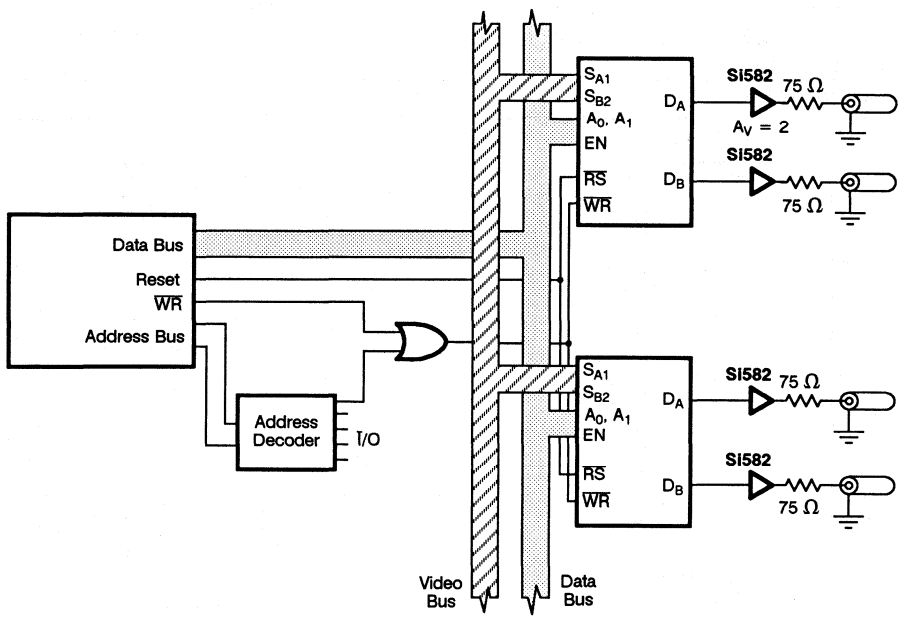


Figure 22. DG534 in a Video Matrix

DG535/536
16-Channel Wideband/Video Multiplexers

Siliconix incorporated

FEATURES

- −100 dB Crosstalk at 5 MHz
- 300 MHz Bandwidth
- 4 pF (max) Input and 12 pF Output Capacitance
- Low Power (75 µW)
- $r_{DS(ON)}$ (90 Ω max)
- µP Interface Latches

BENEFITS

- Improved OFF Isolation
- Reduced Insertion Loss at High Frequencies
- Reduced Input Buffer Requirements
- Minimizes System Power
- Reduced Noise
- Simplifies Bus Interface

APPLICATIONS

- Video Switching/Routing
- High Speed Data Routing
- Wideband Signal Multiplexing
- Precision Data Acquisition
- Crosspoint Arrays
- FLIR Systems

DESCRIPTION

The DG535/536 are 16-channel multiplexers designed for routing one of 16 wideband analog or digital input signals to a single output. They feature low input and output capacitance, low ON resistance, and n-channel DMOS "T" switches, resulting in wide bandwidth, low crosstalk and high "OFF" isolation. In the ON state, the switches pass signals in either direction, allowing the DG535/536 to be used as multiplexers or demultiplexers.

On-chip data latches and decode logic simplify microprocessor interface. Chip Select and Enable inputs simplify addressing in large matrices. Single-supply operation and a low 75 µW power dissipation allows operation in battery powered systems and vastly reduces power supply requirements.

Theses devices are built on a D/CMOS process which creates low-capacitance DMOS FETs on the same substrate with dense, high-speed, low-power CMOS.

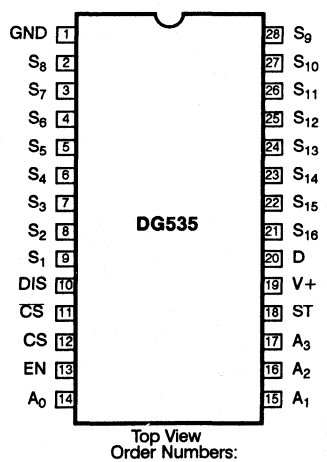
The DG535 is available in the plastic 28-lead DIP for the industrial, D suffix (−40 to 85°C), and the 28-lead side braze DIP for military, A suffix (−55 to 125°C) temperature range operation.

The DG536 is available in surface mount plastic PLCC-44 for industrial, D suffix (−40 to 85°C), and the Cerquad hermetic package for military, A suffix (−55 to 125°C) temperature ranges.

For more information please refer to Siliconix Application Note AN86-1.

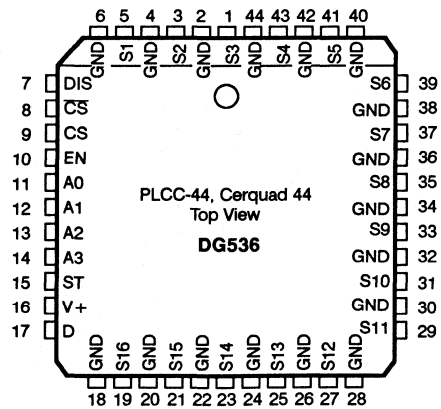
PIN CONFIGURATIONS

Dual-In-Line Package



Top View
Order Numbers:

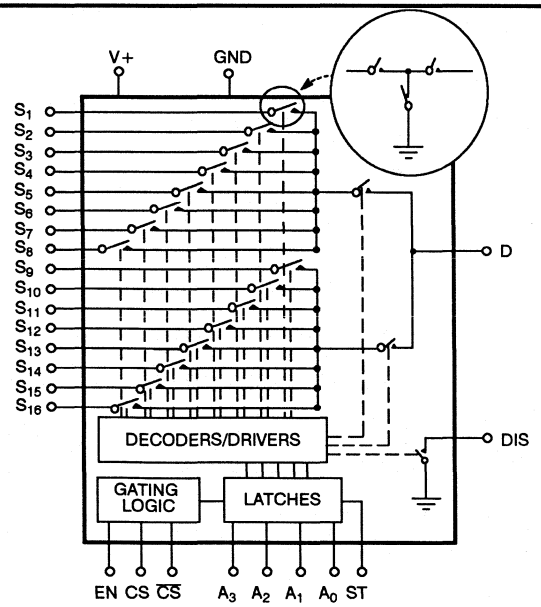
Side Braze: DG535AP, DG535AP/883
Plastic: DG535DJ



Order Numbers:

Plastic: DG536DN
Cerquad: DG536AM/883

FUNCTIONAL BLOCK DIAGRAM AND TRUTH TABLE



EN	CS	$\overline{CS}$	ST	A_3	A_2	A_1	A_0	Channel Selected	Disable
0 X X	X 0 X	X X 1	1	X	X	X	X	NONE	HIGH Z
1	1	0	1	0	0	0	0	S1	LOW Z
				0	0	0	1	S2	
				0	0	1	0	S3	
				0	0	1	1	S4	
				0	1	0	0	S5	
				0	1	0	1	S6	
				0	1	1	0	S7	
				0	1	1	1	S8	
				1	0	0	0	S9	
				1	0	0	1	S10	
				1	0	1	0	S11	
				1	0	1	1	S12	
				1	1	0	0	S13	
				1	1	0	1	S14	
				1	1	1	0	S15	
				1	1	1	1	S16	
X	X	X	0	X	X	X	X	Maintains previous switch condition	HIGH Z or LOW Z

Logic "1": $V_{AH} \geq 10.5$ V
Logic "0" $V_{AL} \leq 4.5$ V

1. LOW Z, HIGH Z = Impedance of Disable Output to GND. Disable output sinks current when any channel is selected.
2. Strobe input (ST) is level triggered.

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3 V to +18 V
Digital Inputs ..... (GND - 0.3 V) to (V+ plus 2 V) or 20 mA, whichever occurs first
V_S, V_D ..... (GND - 0.3 V) to V+ plus 2 V) or 20 mA, whichever occurs first
Current (any terminal) Continuous ..... 20 mA
Current (S or D) Pulsed 1 ms 10% duty cycle ..... 40 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
44-Pin J Lead Cerquad** ..... 825 mW
44-Pin J Lead Plastic*** ..... 450 mW
28-Pin Plastic DIP**** ..... 625 mW
28-Pin Sidebraze DIP***** ..... 1200 mW

*All leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6 mW/°C above 75°C
****Derate 8.6 mW/°C above 75°C
*****Derate 16 mW/°C above 75°C

6

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, ST, CS = 10.5 V $\overline{CS}$ = 4.5 V	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[e]	V_{ANALOG}		Full		0	10	0	10	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -1 mA, V_D = 3 V V_{AL} = 10.5 V, V_{AH} = 4.5 V	Room Full	55		90 120		90 120	Ω
Resistance Match	$\Delta r_{DS(ON)}$	Sequence Each Switch ON EN = 10.5 V	Room			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 3 V, V_D = 0 V EN = 4.5 V	Room Full		-10 -100	10 100	-10 -100	10 100	nA

SPECIFICATIONS[a]

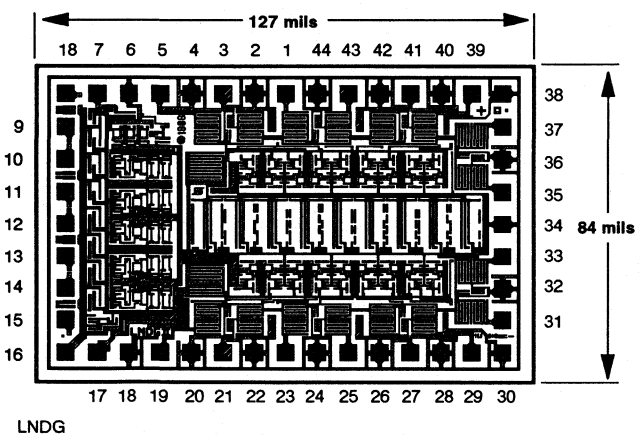
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, ST, CS = 10.5 V, $\overline{CS}$ = 4.5 V		TEMP[f]	TYP[d]	A SUFFIX −55 to 125°C MIN[b]	A SUFFIX −55 to 125°C MAX[b]	D SUFFIX −40 to 85°C MIN[b]	D SUFFIX −40 to 85°C MAX[b]	UNIT
ANALOG SWITCH (Cont'd)										
Total Switch ON Leakage Current	$I_{D(ON)}$	$V_S = V_D = 3$ V, EN = 10.5 V		Room Full		−10 −1000	10 1000	−10 −100	10 100	
Disable Output	$R_{DISABLE}$	$I_{DISABLE}$ = 1 mA, EN = 10.5 V		Room Full	100		200 250		200 250	Ω
DIGITAL CONTROL										
Input Voltage High	V_{AIH}			Full		10.5		10.5		V
Input Voltage Low	V_{AIH}			Full			4.5		4.5	
Address Input Current	I_{AI}	V_A = GND or V+		Room Full	<0.01	−1 −100	1 100	−1 −100	1 100	µA
DYNAMIC CHARACTERISTICS										
ON State Input Capacitance[c]	$C_{S(ON)}$	$V_D = V_S = 3$ V	PLCC Cerquad DIP	Room	32 35 40		45 55		45 55	pF
OFF State Input Capacitance[c]	$C_{S(OFF)}$	$V_S = 3$ V	PLCC Cerquad DIP	Room	2 5 3		8		8	
OFF State Output Capacitance[c]	$C_{D(OFF)}$	$V_D = 3$ V	PLCC Cerquad DIP	Room	8 12 9		20		20	
Multiplexer Switching Time	t_{TRANS}	See Figure 4		Full			300		300	ns
Break-Before-Make Interval	t_{OPEN}			Full		25		25		
EN, CS, $\overline{CS}$, ST, t_{ON}	t_{ON}	See Figure 2 and 3		Full			300		300	
EN, CS, $\overline{CS}$, ST, t_{OFF}	t_{OFF}	See Figure 2		Full			150		150	
Charge Injection	Q	See Figure 5		Room	−35					pC
Single-Channel Crosstalk (See Figure 9)	$X_{TALK(SC)}$	R_{IN} = 75 Ω, R_L = 75 Ω, f = 5 MHz	PLCC Cerquad DIP	Room	−100 −93 −83					dB
Chip Disabled Crosstalk (See Figure 8)	$X_{TALK(CD)}$	$R_{IN} = R_L$ = 75 Ω, f = 5 MHz, EN = 4.5 V	PLCC Cerquad DIP	Room	−85 −85 −60					
Adjacent Input Crosstalk (See Figure 10)	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz	PLCC Cerquad DIP	Room	−92 −72 −72					
All Hostile Crosstalk[c] (See Figure 7)	$X_{TALK(AH)}$		PLCC Cerquad DIP	Room	−74 −74 −60	−60		−60		
Bandwidth	BW	R_L = 50 Ω, See Figure 6		Room	500					MHz
POWER SUPPLIES										
Positive Supply Current	I+	Any One Channgel Selected with Address Inputs at GND or V+		Room Full	5		50 100		50 100	µA
Supply Voltage Range	V+			Full		10	16.5	10	16.5	V

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, ST, CS = 10.5 V, $\overline{CS}$ = 4.5 V	TEMP[f]	TYP[d]	A SUFFIX −55 to 125°C MIN[b]	A SUFFIX −55 to 125°C MAX[b]	D SUFFIX −40 to 85°C MIN[b]	D SUFFIX −40 to 85°C MAX[b]	UNIT
MINIMUM INPUT TIMING REQUIREMENTS									
Strobe Pulse Width	t_{SW}	See Figure 1	Full		200		200		ns
A_0, A_1, A_2, A_3 CS, $\overline{CS}$, EN Data Valid to Strobe	t_{DW}		Full		100		100		
A_0, A_1, A_2, A_3 CS, $\overline{CS}$, EN Data Valid after Strobe	t_{WD}		Full		50		50		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY at 25°C, not guaranteed nor subject to production testing.
e. Analog signal range is measured from the GND pin to the designated Source (Input) pin.
f. Room = 25°C, Full = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



Pad No.	Function	Pad No.	Function
1	S_3	23	S_{14}
2	GND	24	GND
3	S_2	25	S_{13}
4	GND	26	GND
5	S_1	27	S_{12}
6	GND	28	GND
7	DIS	29	S_{11}
8	$\overline{CS}$	30	GND
9	CS	31	S_{10}
10	EN	32	GND
11	A_0	33	S_9
12	A_1	34	GND
13	A_2	35	S_8
14	A_3	36	GND
15	ST	37	S_7
16	V+	38	GND
17	D	39	S_6
18	GND (Substrate)	40	GND
19	S_{16}	41	S_5
20	GND	42	GND
21	S_{15}	43	S_4
22	GND	44	GND

695 Transistors
16 Diodes

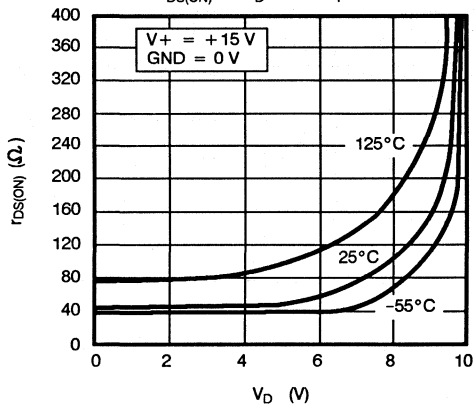
427 n-Channel
268 p-Channel

PIN DESCRIPTION

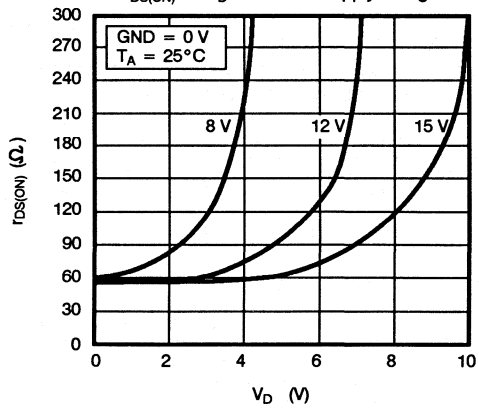
SYMBOL	DESCRIPTION
$S_{1, 2 -- 16}$	Analog inputs/outputs
D	Multiplexer output/demultiplexer input
DIS	Open drain low impedance to analog ground when any channel is selected
$\overline{CS}$, CS, EN	Logic inputs to selected desired multiplexer(s) when using several multiplexers in a system
$A_{0 - 3}$	Binary address inputs to determine which channel is selected
ST	Strobe input that latches A_0, A_1, A_2, A_3, $\overline{CS}$, CS, EN
V+	Positive supply voltage input
GND	Analog signal ground and most negative potential **All ground pins should be connected externally to ensure dynamic performance**

TYPICAL CHARACTERISTICS

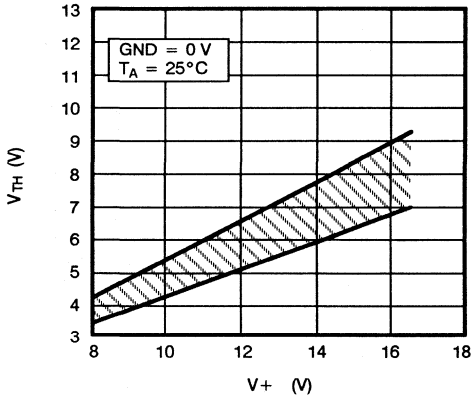
$r_{DS(ON)}$ vs. V_D and Temperature



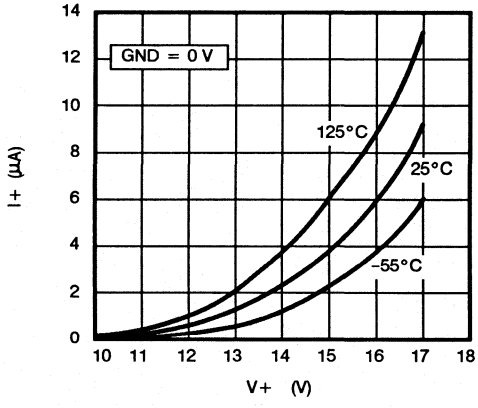
$r_{DS(ON)}$ vs. V_D and Power Supply Voltage



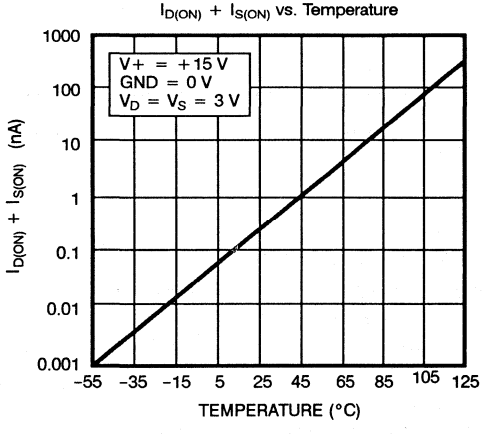
Logic Input Switching Threshold vs. Supply Voltage (V+)



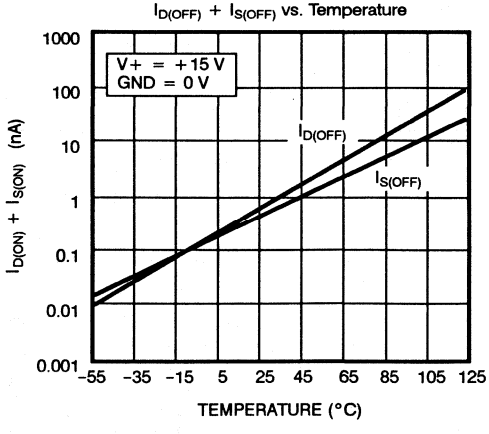
Supply Current vs. Supply Voltage and Temperature



$I_{D(ON)} + I_{S(ON)}$ vs. Temperature

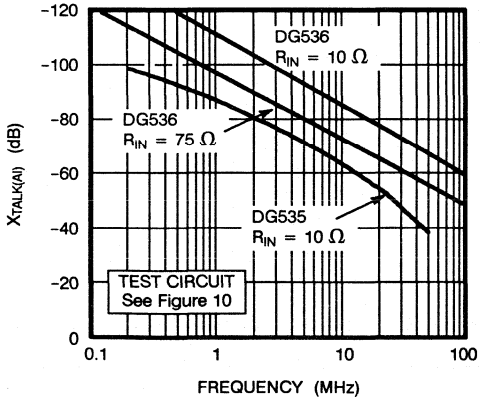


$I_{D(OFF)} + I_{S(OFF)}$ vs. Temperature

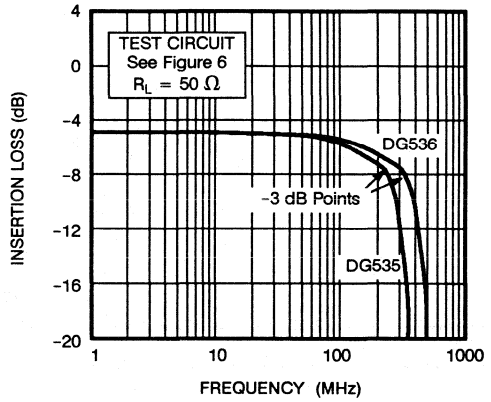


TYPICAL CHARACTERISTICS (Cont'd)

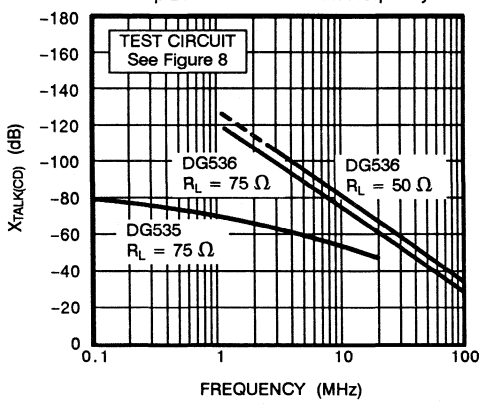
Adjacent Input Crosstalk vs. Frequency



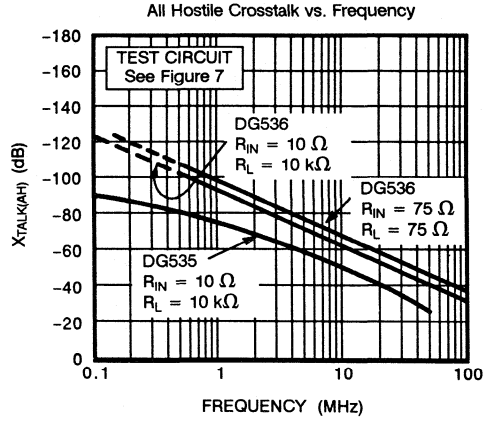
-3 dB Bandwidth
Insertion Loss vs. Frequency



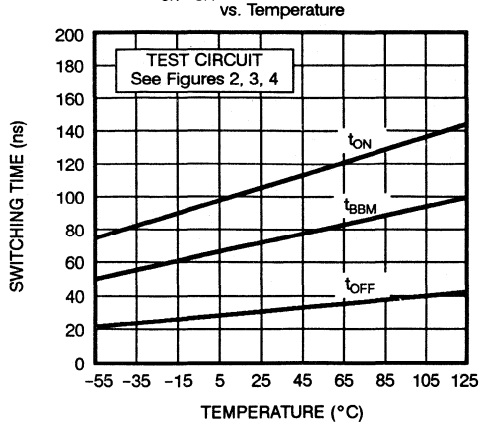
Chip Disabled Crosstalk vs. Frequency



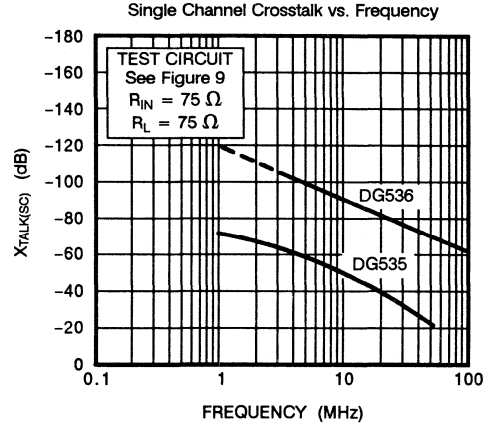
All Hostile Crosstalk vs. Frequency



t_{ON}, t_{OFF} and Break-Before-Make
vs. Temperature



Single Channel Crosstalk vs. Frequency



6

INPUT TIMING REQUIREMENTS

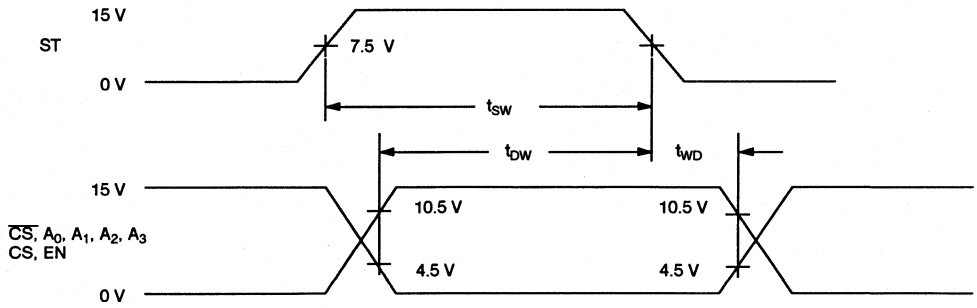


Figure 1.

TEST CIRCUITS

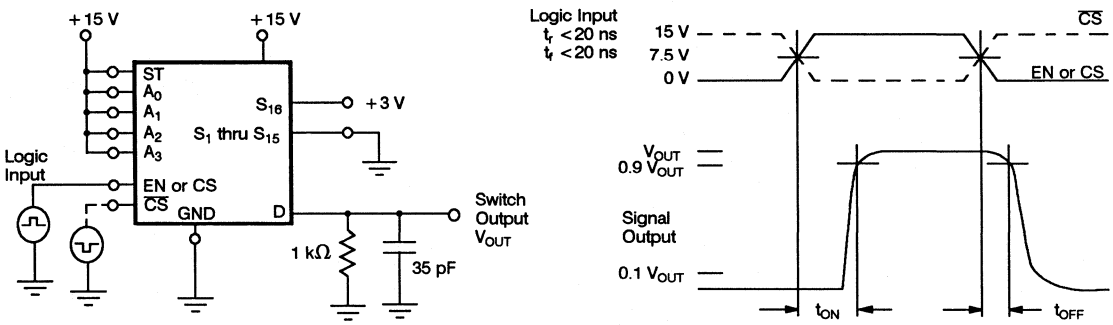


Figure 2. EN, CS, $\overline{CS}$, Turn ON/OFF Time

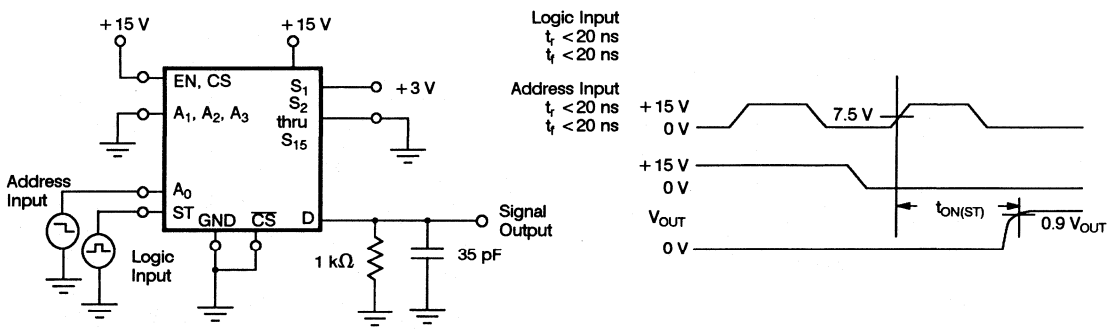


Figure 3. Strobe ST Turn ON Time

TEST CIRCUITS (Cont'd)

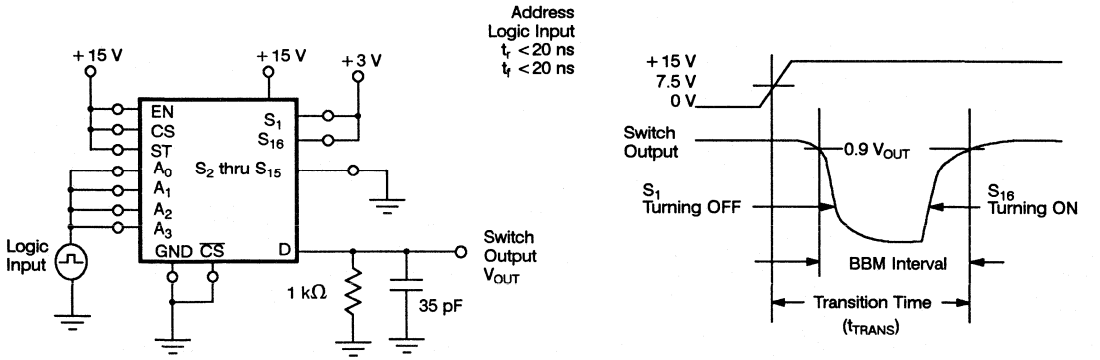


Figure 4. Transition Time and Break-Before-Make Interval

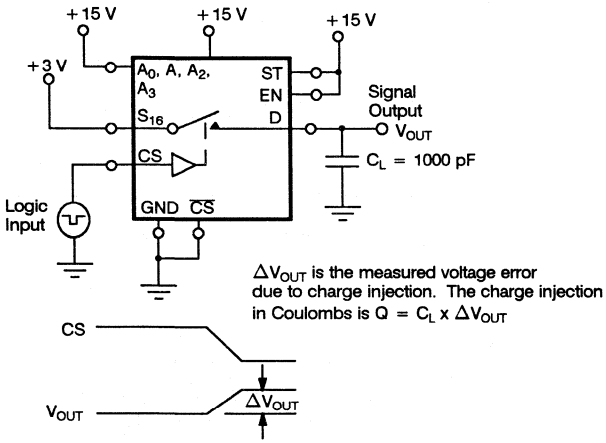


Figure 5. Charge Injection

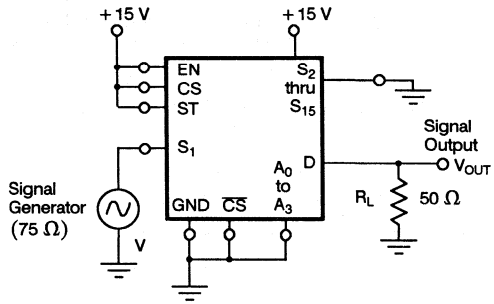


Figure 6. Bandwidth

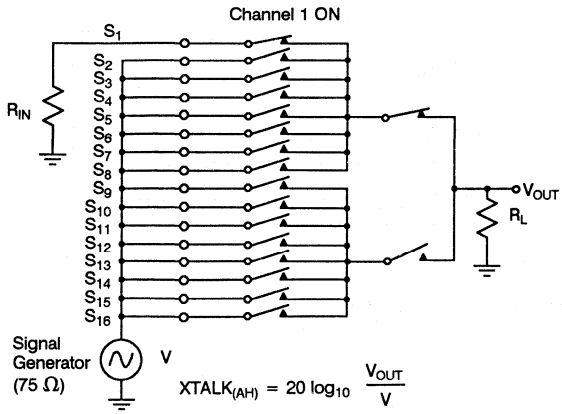


Figure 7. All Hostile Crosstalk - $XTALK_{(AH)}$

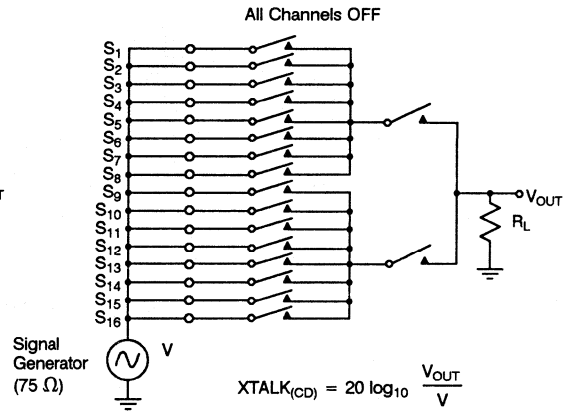
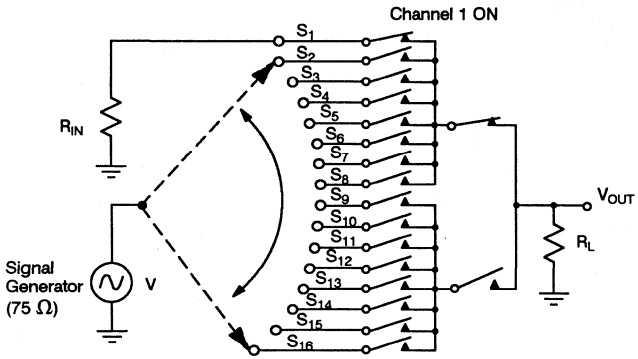


Figure 8. Chip Disabled Crosstalk - $XTALK_{(CD)}$

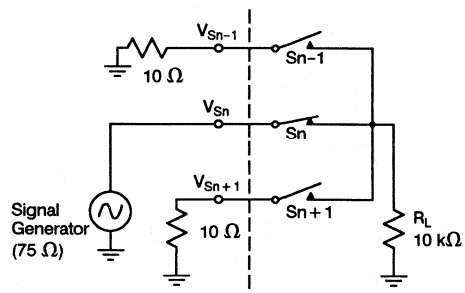
6

TEST CIRCUITS (Cont'd)



NOTES:
1. Any individual channel between S_2 and S_{16} can be selected
2. $XTALK_{(SC)}$ = Average value of $20 \log_{10} \frac{V_{OUT}}{V}$ is scanned sequentially from S_2 to S_{16}

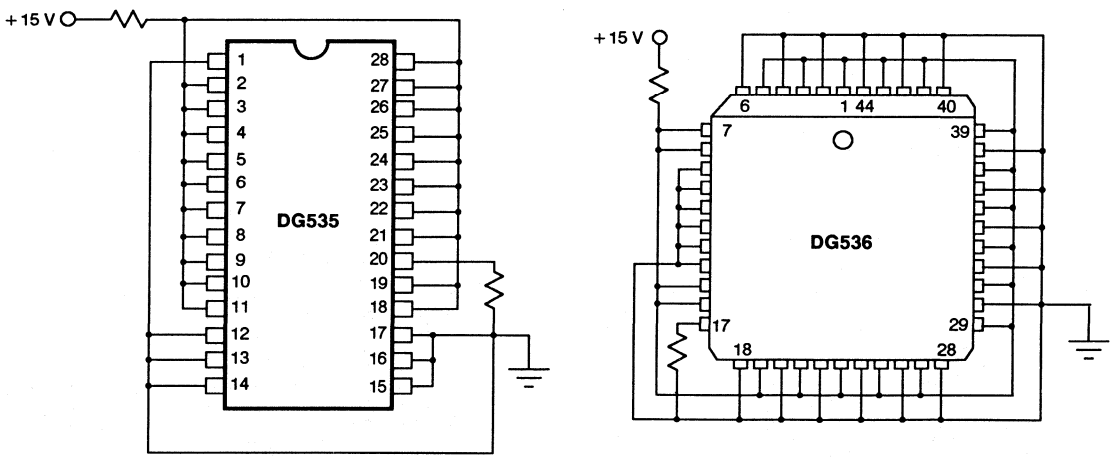
Figure 9. Single Channel Crosstalk - $XTALK_{(SC)}$



$$XTALK_{(AI)} = 20 \log_{10} \frac{V_{Sn-1}}{V} \text{ or } 20 \log_{10} \frac{V_{Sn+1}}{V}$$

Figure 10. Adjacent Input Crosstalk - $XTALK_{(AI)}$

BURN-IN CIRCUITS



Note: All resistors are 10 kΩ unless otherwise specified

Figure 11.

DETAILED DESCRIPTION

The DG535/536 are 16-channel single-ended multiplexers with on-chip address logic and control latches.

The multiplexer connects one of sixteen inputs (S_1, S_2,...S_{16}) to a common output (D) under the control of a 4-bit binary address (A_0 to A_3). The specific input channel selected for each address is given in the Truth Table.

All four address inputs have on-chip data latches which are controlled by the Strobe (ST) input. These latches are transparent when Strobe is high but they maintain the chosen address when Strobe goes low. To facilitate easy microprocessor control in large matrices a choice of three independent logic inputs (EN, CS and $\overline{CS}$) are provided on chip. These inputs are gated together (see Figure 12) and only when EN = CS = 1 and $\overline{CS}$ = 0 is true can an output switch be selected. This necessary logic condition is then latched-in when Strobe (ST) goes low.

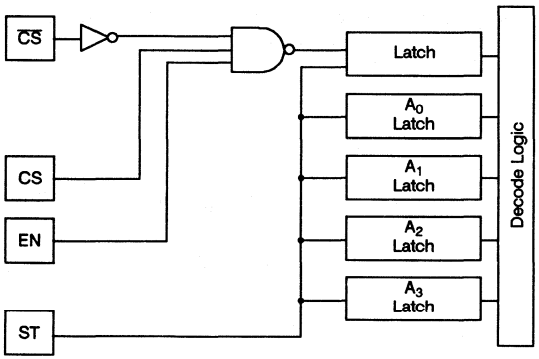


Figure 12. $\overline{CS}$, CS, EN, ST Control Logic

Break-before-make switching prevents momentary shorting when changing from one input to another.

The devices feature a two-level switch arrangement whereby two banks of eight switches (first level) are connected via two series switches (second level) to a common DRAIN output.

In order to improve crosstalk all sixteen first level switches are configured as "T" switches (see Figure 13).

With this method SW2 operates out of phase with SW1 and SW3. In the ON condition SW1 and SW3 are closed with SW2 open whereas in the OFF condition SW1 and SW3 are open and SW2 closed. In the OFF condition the input to SW3 is effectively the isolation leakage of SW1 working into the ON resistance of SW2 (typically 200 Ω).

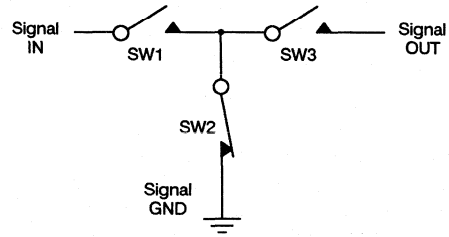


Figure 13. "T" Switch Arrangement

The two second level series switches further improve crosstalk and help to minimize output capacitance.

The DIS output can be used to signal external circuitry. DIS is a high impedance to GND when no channel is selected and a low impedance to GND when any one channel is selected.

The DG535/536 have extensive applications where any high frequency video or digital signals are switched or routed. Exceptional crosstalk and bandwidth performance is achieved by using n-channel DMOS FETs for the "T" and series switches.

A cross section of a switch is shown in Figure 14.

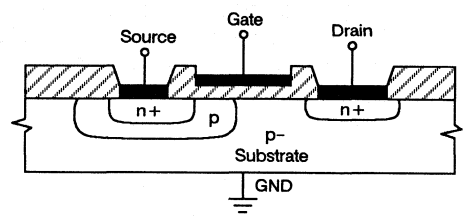


Figure 14. Cross-Section of a Single DMOS Switch

It can clearly be seen from Figure 14 that there exists a PN junction between the substrate and the drain/source terminals.

Should a signal which is negative with respect to the substrate (GND pin) be connected to a source or drain terminal, then the PN junction will become forward biased and current will flow between the signal source and GND. This effective shorting of the signal source to GND will not necessarily cause any damage to the device, provided that the total current flowing is less than the maximum rating, (i.e., 20 mA).

Since no PN junctions exist between the signal path and V+, positive overvoltages are not a problem, unless the breakdown voltage of the DMOS drain terminal (see Figure 14) (+18 V) is exceeded. Positive overvoltage conditions must not exceed +18 V with respect to the GND pin. If this condition is possible (e.g. transients in the signal), then a diode or Zener clamp may be used to prevent breakdown.

The overvoltage conditions described may exist if the supplies are collapsed while a signal is present on the inputs. If this condition is unavoidable, then the necessary steps outlined above should be taken to protect the device

DC BIASING

To avoid negative overvoltage conditions and subsequent distortion of ac analog signals, dc biasing may be necessary. Biasing is not required, however, in applications where signals are always positive with respect to the GND or substrate connection, or in applications involving multiplexing of low level (up to ±200 mV) signals, where forward biasing of the PN substrate-source/drain terminals would not occur.

Biasing can be accomplished in a number of ways, the simplest of which is a resistive potential divider and a few dc blocking capacitors as shown in Figure 15.

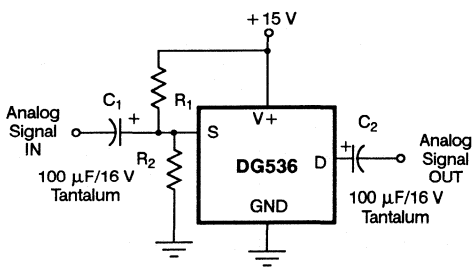


Figure 15. Simple Bias Circuit

R_1 and R_2 are chosen to suit the appropriate biasing requirements. For video applications, approximately 3 V of bias is required for optimal differential gain and phase performance. Capacitor C_1 blocks the dc bias voltage from being coupled back to the analog signal source and C_2 blocks the dc bias from the output signal. Both C_1 and C_2 should be tantalum or ceramic disc type capacitors in order to operate efficiently at high frequencies.

Active bias circuits are recommended if rapid switching time between channels is required.

An alternative method is to offset the supply voltages (see Figure 16).

Decoupling would have to be applied to the negative supply to ensure that the substrate is well referenced to signal ground. Again the capacitors should be of a type offering good high frequency characteristics.

Level shifting of the logic signals may be necessary using this offset supply arrangement.

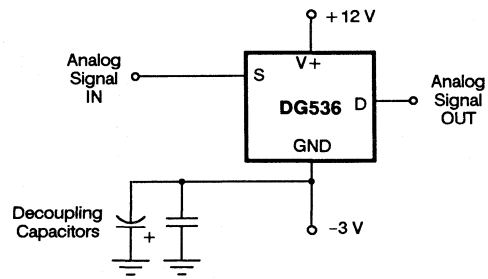


Figure 16. DG536 with Offset Supply

TTL to CMOS level shifting is easily obtained by using a MC14504B.

CIRCUIT LAYOUT

Good circuit board layout and extensive shielding is essential for optimizing the high frequency performance of the DG536. Stray capacitances on the PC board and/or connecting leads will considerably degrade the ac performance. Hence, signal paths must be kept as short as practically possible, with extensive ground planes separating signal tracks.

DG540/541/542
Wideband/Video "T" Switches

FEATURES

- Wide Bandwidth (500 MHz)
- Very Low Crosstalk (-85 dB) and High OFF-Isolation (-80 dB) at 5 MHz
- "T" Switch Configuration
- TTL Compatible
- Fast Switching (t_{ON} <70 ns)
- ESD Protection > ±4000 V
- Low $r_{DS(ON)}$ <75 Ω

BENEFITS

- Improved Data Throughput
- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption

APPLICATIONS

- RF and Video Switching
- RGB Switching
- Local and Wide Area Networks
- Video Routing
- Fast Data Acquisition
- ATE
- Radar/FLIR Systems
- Video Multiplexing

DESCRIPTION

The DG540/541/542 are very high performance monolithic wideband/video switches designed for switching wide bandwidth analog and digital signals. By utilizing a "T" switch configuration techniques on each channel, these devices achieve exceptionally low crosstalk and high OFF-isolation. The crosstalk and OFF-isolation of the DG540 are further improved by the introduction of extra GND pins between signal pins.

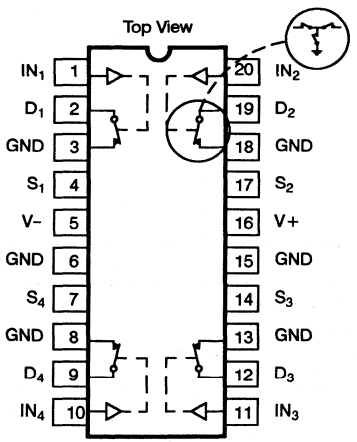
To achieve TTL compatibility, low channel capacitances and fast switching times, the DG540 family is built on the Siliconix proprietary D/CMOS process. Each switch conducts equally well in both directions when ON.

The DG540 is available in 20-pin side braze, plastic, and PLCC packages. Packaging for the DG541 and DG542 includes 16-pin side braze, plastic, and small outline options. Performance grades include military, A suffix (-55 to 125°C) and industrial, D suffix (-40 to 85°C) temperature ranges.

PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES

Dual-In-Line Package

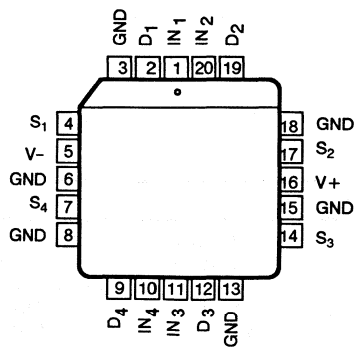
Top View



Order Numbers:

Side Braze: DG540AP, DG540AP/883
Plastic: DG540DJ

PLCC Package



Top View

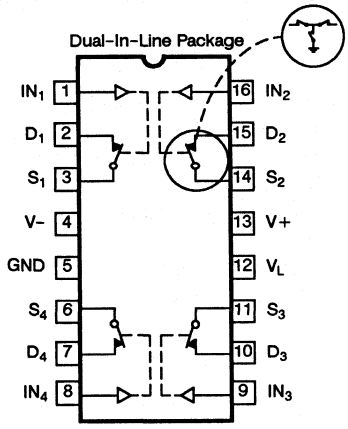
Order Number:
DG540DN

Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.0 V

6

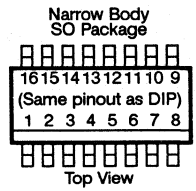
PIN CONFIGURATIONS, FUNCTIONAL BLOCK DIAGRAMS AND TRUTH TABLES (Cont'd)



Top View

Order Numbers:

Side Braze: DG541AP, DG541AP/883
Plastic: DG541DJ

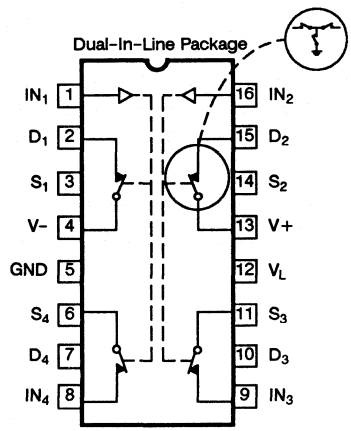


Top View

Order Numbers:
DG541DY

Logic	Switch
0	OFF
1	ON

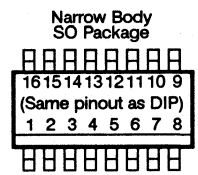
Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V



Top View

Order Numbers:

Side Braze: DG542AP, DG542AP/883
Plastic: DG542DJ



Top View

Order Numbers:
DG542DY

Logic	SW1 SW2	SW3 SW4
0	OFF ON	ON OFF
1		

Logic "0" $\leq$ 0.8 V
Logic "1" $\geq$ 2.0 V

* Switches shown for logic "1" input.

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... -0.3 V to 21 V
V+ to GND ..... -0.3 V to 21 V
V- to GND ..... -19 V to +0.3 V
Digital Inputs ..... (V-) -0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
V_S, V_D ..... (V-) -0.3 V to (V-) +14 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 20 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle max) ..... 40 mA
Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C
Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*
16-, 20-Pin Size Braze DIP** ..... 900 mW
20-Pin Plastic DIP*** ..... 800 mW
20-Pin PLCC**** ..... 800 mW
16-Pin Plastic DIP***** ..... 470 mW
16-Pin SO****** ..... 640 mW

* All leads welded or soldered to PC board.
** Derate 12 mW/°C above 75°C.
*** Derate 7 mW/°C above 25°C.
**** Derate 10 mW/°C above 75°C.
***** Derate 6.5 mW/°C above 25°C.
****** Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V V_{INH} = 2 V, V_{INL} = 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[e]	V_{ANALOG}	V- = -5 V, V+ = 12 V	Full		-5	8	-5	8	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = 0 V	Room Full	30		60 100		60 75	Ω
$r_{DS(ON)}$ Match	$\Delta r_{DS(ON)}$		Room	2		6		6	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 0 V, V_D = 10 V	Room Full	-0.05	-10 -500	10 500	-10 -100	10 100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = 10 V, V_D = 0V	Room Full	-0.05	-10 -500	10 500	-10 -100	10 100	
Channel ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 0 V	Room Full	-0.05	-10 -1000	10 1000	-10 -100	10 100	
DIGITAL CONTROL									
Input Voltage High	V_{INH}		Room Full		2 2		2 2		V
Input Voltage Low	V_{INL}		Room Full			0.8 0.8		0.8 0.8	
Input Current	I_{IN}	V_{IN} = GND or V+	Room Full	0.05	-1 -20	1 20	-1 -20	1 20	µA
DYNAMIC CHARACTERISTICS									
ON State Input Capacitance[c]	$C_{S(ON)}$	V_S = V_D = 0 V	Room	14		20		20	pF
OFF State Input Capacitance[c]	$C_{S(OFF)}$	V_S = 0 V	Room	2		4		4	
OFF State Output Capacitance[c]	$C_{D(OFF)}$	V_D = 0 V	Room	2		4		4	
Bandwidth DG540 DG542	BW	R_L = 50 Ω, See test Circuit	Room	500					MHz
Bandwidth DG541			Room	350					
Turn ON Time DG540 DG541	t_{ON}	R_L = 1 kΩ, C_L = 35 pF 50% to 90%, See Test Circuit	Room Full	45		70 130		70 130	ns
Turn ON Time DG542			Room Full	55		100 160		100 160	
Turn OFF Time DG540 DG541	t_{OFF}		Room Full	20		50 85		50 85	
Turn OFF Time DG542			Room Full	25		60 85		60 85	
Charge Injection	Q	C_L = 1000 pF, V_D = 0 V See Test Circuit	Room	-25					pC
OFF Isolation DG540		R_{IN} = 75 Ω, R_L = 75 Ω f = 5 MHz, See Test Circuit	Room	-80					dB
OFF Isolation DG541			Room	-60					
OFF Isolation DG542			Room	-75					
All Hostile Crosstalk	$XTALK_{(AH)}$	R_{IN} = 10 Ω, R_L = 75 Ω f = 5 MHz, See Test Circuit	Room	-85					

6

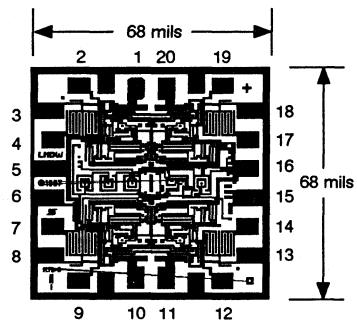
Siliconix incorporated

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V V_{INH} = 2 V, V_{INL} = 0.8 V[e]	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+	All Channels ON or OFF	Room Full	3.5		6 9		6 9	mA
Negative Supply Current	I-		Room Full	-3.2	-6 -9		-6 -9		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. V_{IN} = Input voltage to perform proper function.
f. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

DIE TOPOGRAPHY



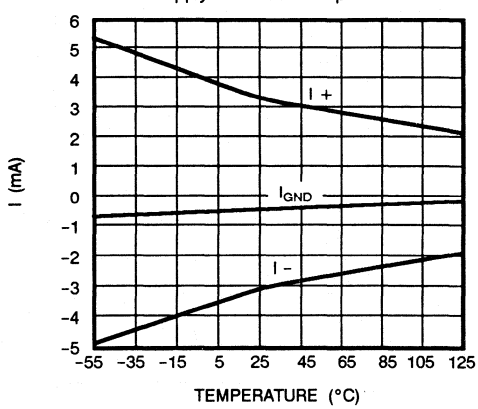
LNDW-A, LNDW-B

32 n-channel Enhancement MOSFETs
28 p-channel Enhancement MOSFETs
4 NPN Bipolar Transistors
8 Diodes
1 Zener Diode
6 Resistors

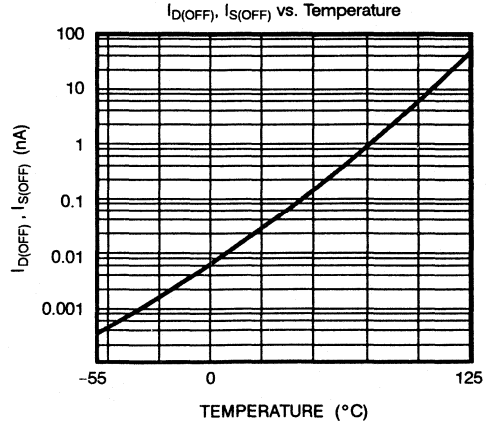
Pad No.	Function DG540	Pad No.	Function DG541	Pad No.	Function DG542
1	IN_1	1	IN_1	1	IN_1
2	D_1	2	D_1	2	D_1
3	GND	3	NC	3	GND
4	S_1	4	S_1	4	S_1
5	V- (Substrate)	5	V- (Substrate)	5	V- (Substrate)
6	GND	6	GND	6	NC
7	S_4	7	S_4	7	S_4
8	GND	8	NC	8	GND
9	D_4	9	D_4	9	D_4
10	IN_4	10	IN_4	10	NC
11	IN_3	11	IN_3	11	NC
12	D_3	12	D_3	12	D_3
13	GND	13	NC	13	GND
14	S_3	14	S_3	14	S_3
15	GND	15	GND	15	NC
16	V+	16	V+	16	V+
17	S_2	17	S_2	17	S_2
18	GND	18	NC	18	GND
19	D_2	19	D_2	19	D_2
20	IN_2	20	IN_2	20	IN_2

TYPICAL CHARACTERISTICS

Supply Current vs. Temperature

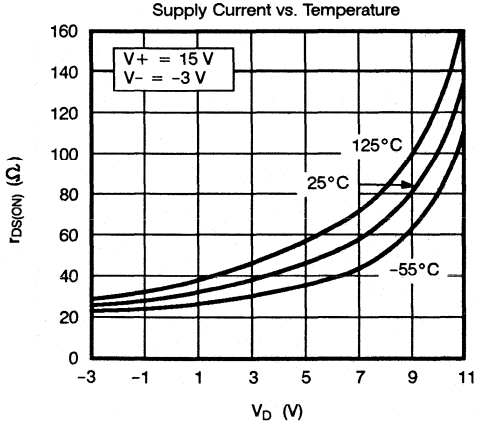


$I_{D(OFF)}$, $I_{S(OFF)}$ vs. Temperature

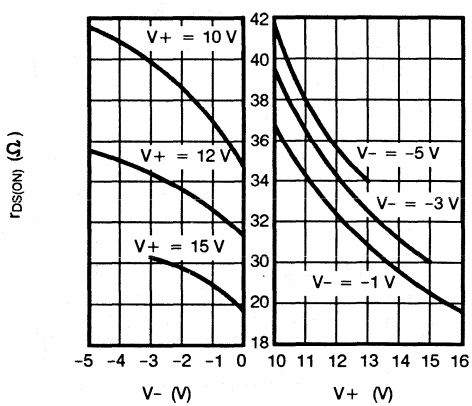


TYPICAL CHARACTERISTICS (Cont'd)

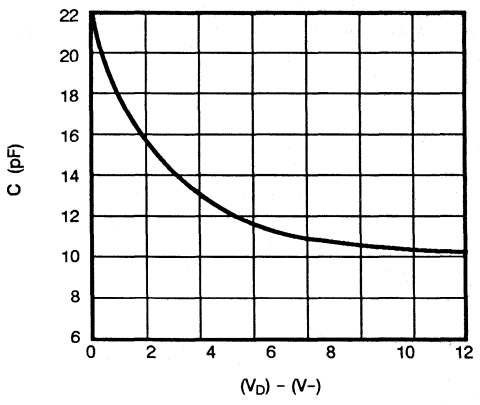
Supply Current vs. Temperature



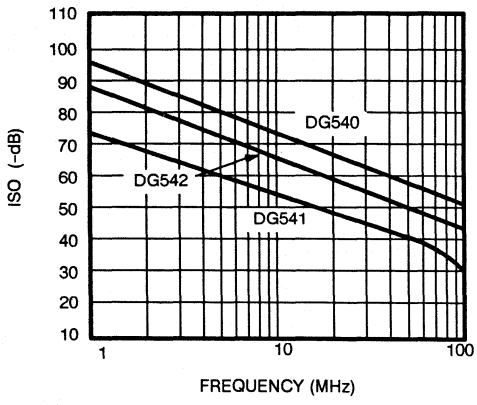
V+ Constant V- Constant



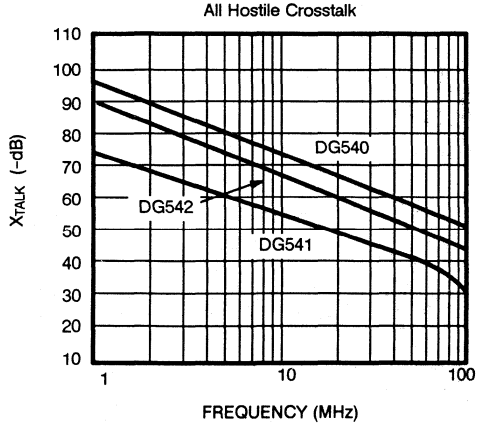
ON Capacitance



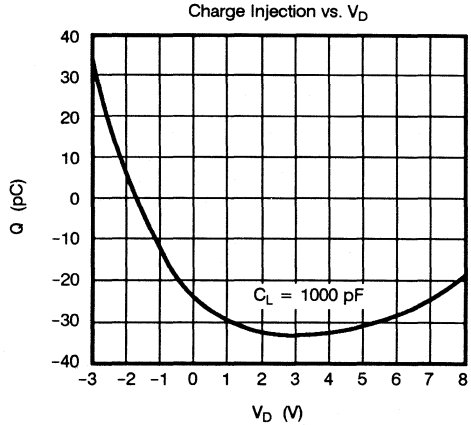
OFF Isolation



All Hostile Crosstalk



Charge Injection vs. V_D



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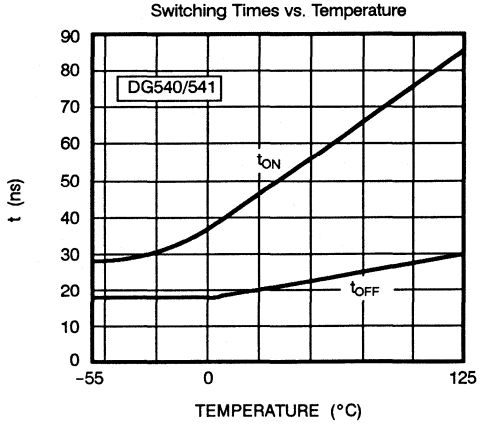
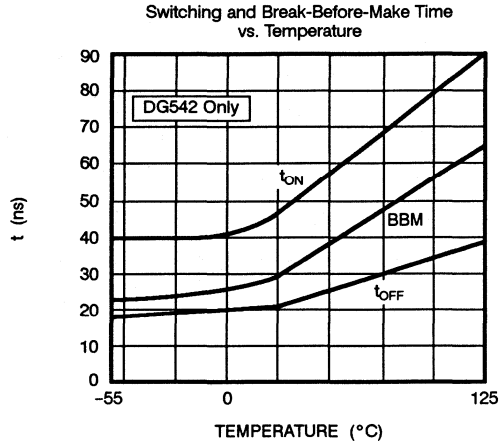
TYPICAL CHARACTERISTICS (Cont'd)





TEST CIRCUITS

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

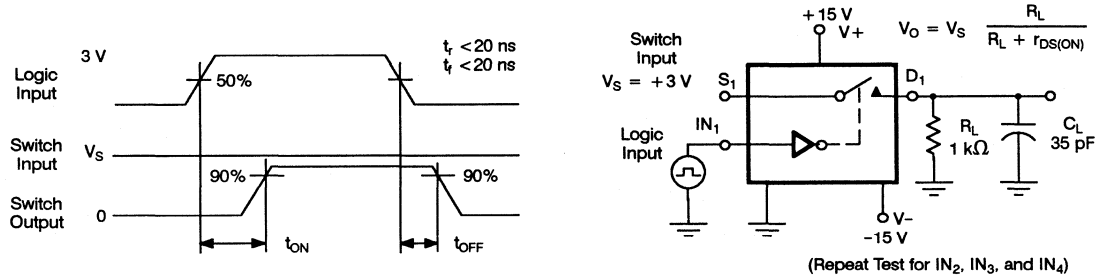


Figure 1. Switching Time

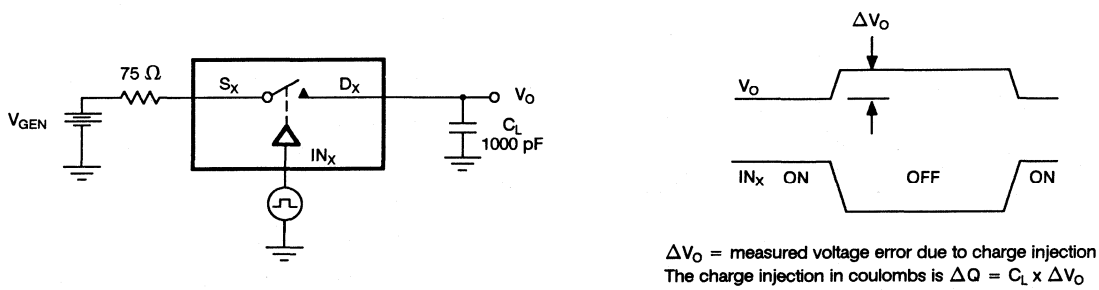


Figure 2. Charge Injection

TEST CIRCUITS (Cont'd)

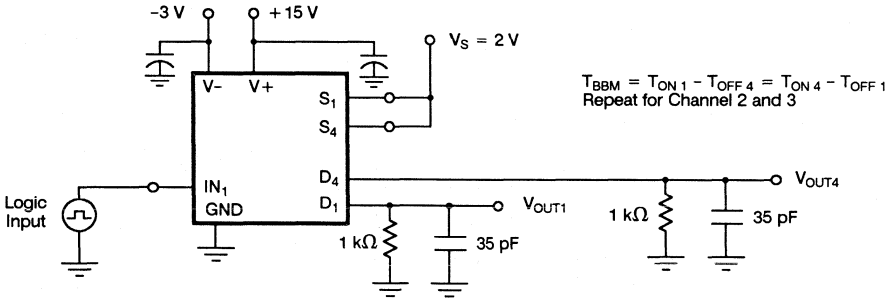


Figure 3. Break-Before-Make (DG542 Only)

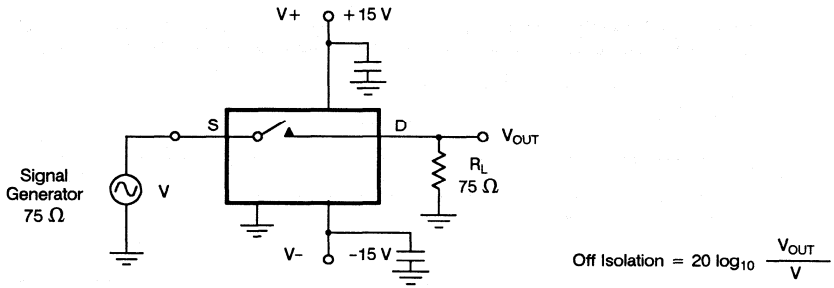


Figure 4. Off Isolation

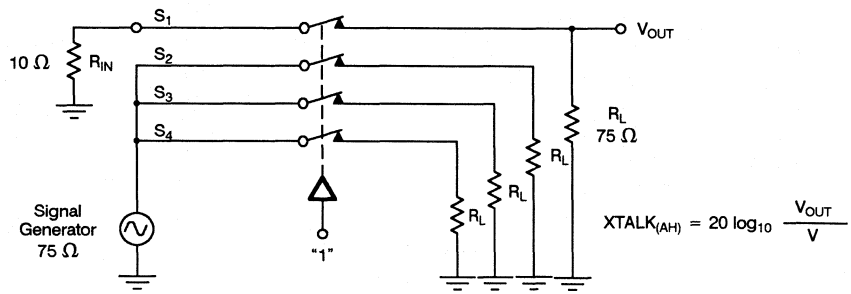


Figure 5. All Hostile Crosstalk - $XTALK_{(AH)}$

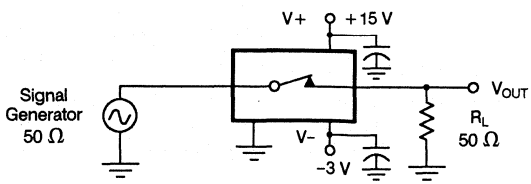
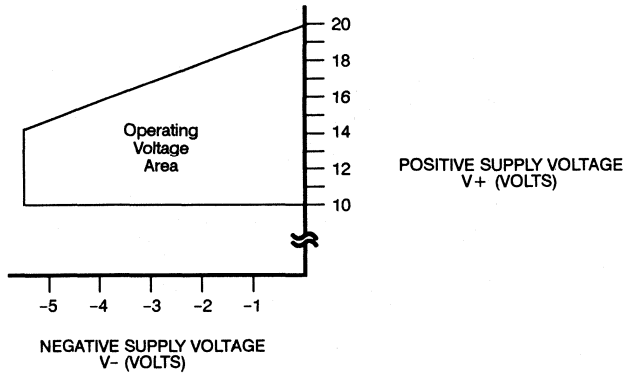


Figure 6. Bandwidth

OPERATING SUPPLY VOLTAGE RANGE



Note:

1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10 µF tantalum bead in parallel with 100 nF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3 V.

Figure 7.

BURN-IN CIRCUITS

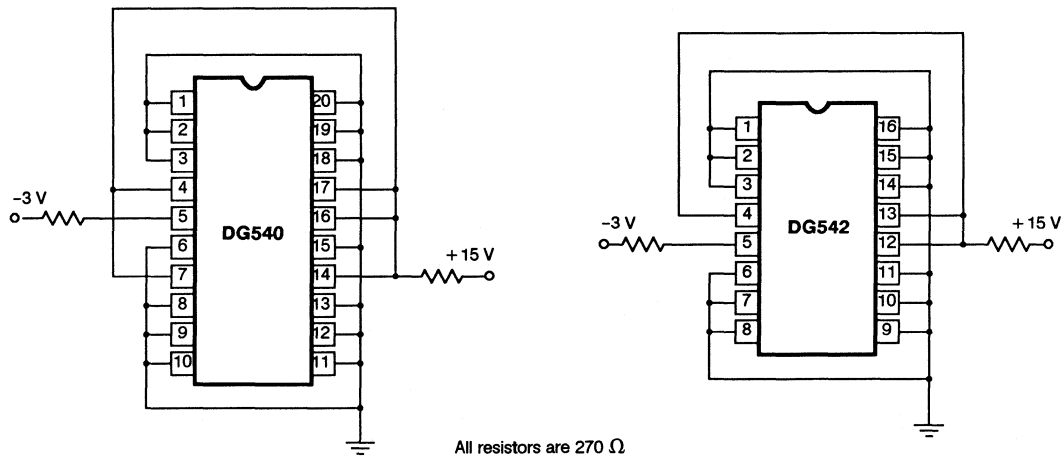


Figure 8.

APPLICATIONS

Device Description

The DG540/541/542 family of wideband switch offers true bidirectional switching of high frequency analog or digital signals with minimum signal crosstalk, low insertion loss, and negligible non-linearity distortion and group delay.

Built on the Siliconix D/CMOS process, these "T" switches provide excellent off-isolation with a bandwidth of around 500 MHz (350 MHz for DG541). Silicon-gate D/CMOS processing also yields fast switching speeds.

An on-chip regulator circuit maintains TTL input compatibility over the whole operating supply voltage range shown, easing control logic interfacing.

Circuit layout is facilitated by the interchangeability of source and drain terminals.

Frequency Response

A single switch on-channel exhibits both resistance [$r_{DS(ON)}$] and capacitance [$C_{S(ON)}$]. This RC combination has an attenuation effect on the analog signal - which is frequency dependent (like an RC low-pass filter). The -3 dB bandwidth of the DG540 is typically. 500 MHz (into 50 Ω). This measured figure of 500 MHz illustrates that the switch channel can not be represented by a two stage RC combination. The ON capacitance of the channel is distributed along the ON-resistance, and hence becomes a more complex multi stage network of R's and C's making up the total $r_{DS(ON)}$ and $C_{S(ON)}$. See Application Note AN88-2 for more details.

Power Supplies

A useful feature of the DG54X family is its power supply flexibility. It can be operated from a single positive supply (V+) if required (V- connected to ground).

Note that the analog signal must not exceed V- by more than -0.3 V to prevent forward biasing the substrate p-n junction. The use of a V- supply has a number of advantages:

1) It allows flexibility in analog signal handling, i.e., with V- = -5 V and V+ = 12 V; up to ± 5 V ac signals can be controlled.

2) The value of ON capacitance [$C_{S(ON)}$] may be reduced. A property known as 'the body-effect' on the DMOS switch devices causes various parametric effects to occur. One of these effects is the reduction in $C_{S(ON)}$ for an increasing V body-source. Note however that to increase V- normally requires V+ to be reduced (since V+ to V- = 21 V max.). Reduction in V+ causes an increase in $r_{DS(ON)}$, hence a compromise has to be achieved. It is also useful to note that tests indicate that optimum video linearity performance (e.g., differential phase and gain) occurs when V- is around -3 V.

3) V- eliminates the need to bias the analog signal using potential dividers and large coupling capacitors.

Decoupling

It is an established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG54X is adversely affected by poor decoupling of power supply pins. Also, of even more significance, since the substrate of the device is connected to the negative supply, adequate decoupling of this pin is essential.

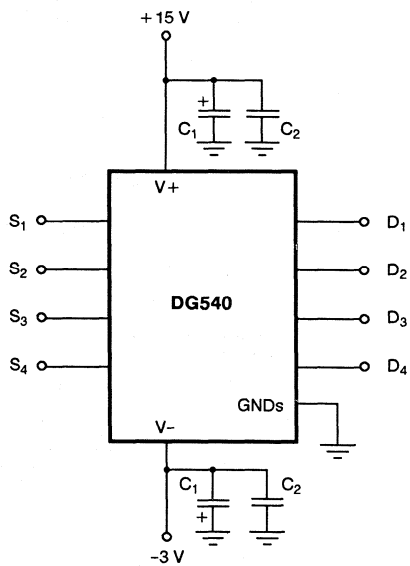
Rules:

a) Decoupling capacitors should be incorporated on all power supply pins (V+, V-). (See Figure 9)

b) They should be mounted as close as possible to the device pins.

c) Capacitors should be of a suitable type with good high frequency characteristics - tantalum bead and/or ceramic disc types are adequate.

Suitable decoupling capacitors are 1 to 10 µF tantalum bead, plus 10 to 100 nF ceramic or polyester.



C_1 = 10 µF Tantalum
C_2 = 0.1 µF Polyester

Figure 9. Supply Decoupling

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Board Layout

PCB layout rules for good high frequency performance must also be observed to achieve the performance boasted by the DG540. Some tips for minimizing stray effects are:

1) Use extensive ground planes on double sided pcb, separating adjacent signal paths. Multilayer pcb is even better.

2) Keep signal paths as short as practically possible, with all channel paths of near equal length.

3) Careful arrangement of ground connections is also very important. Star connected system grounds eliminate signal current, flowing through ground path parasitic resistance, from coupling between channels.

Figure 10 shows a 4-channel video multiplexer using a DG540.

Figure 11 shows a RGB selector switch using two DG542's.

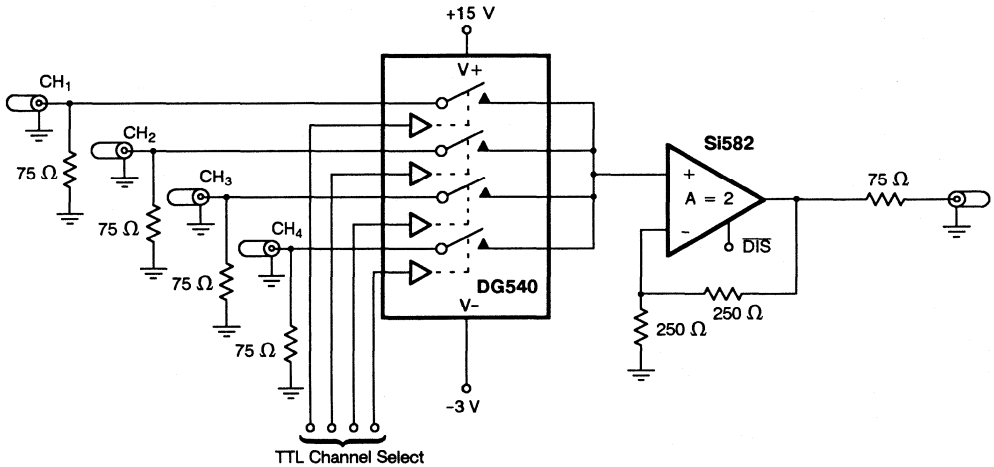


Figure 10. 4 by 1 Video Multiplexing Using the DG540

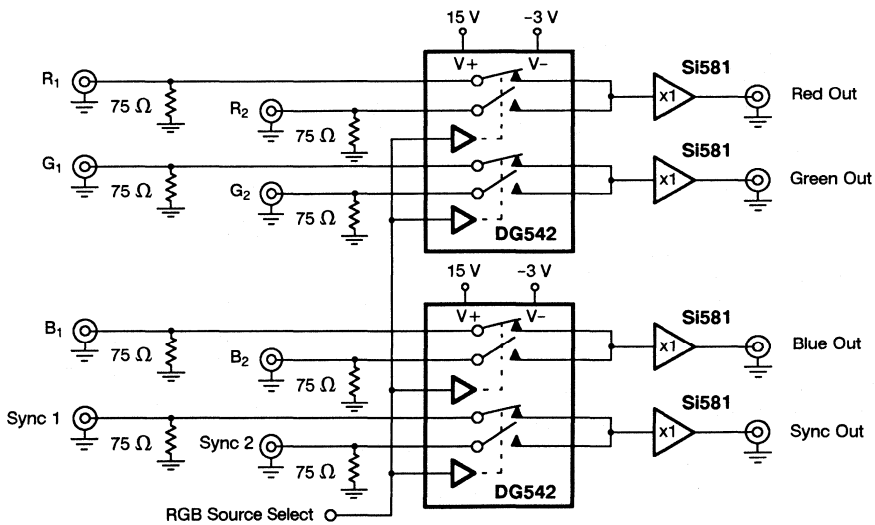


Figure 11. RGB Selector Switch Using Two DG542's

Siliconix incorporated

DG884
8 x 4 Wideband/Video Crosspoint Array

FEATURES

- 8 Inputs, 4 Outputs
- Wide Bandwidth (300 MHz)
- Very Low Crosstalk (−85 dB @ 5 MHz)
- On-board TTL-compatible Latches with Readback
- Optional negative Supply Input
- Low $r_{DS(ON)}$ (90 Ω) max
- ESD Protection > ±4000 V

BENEFITS

- Reduced Board Space
- Improved System Bandwidth
- Improved Channel Off-isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- High Reliability

APPLICATIONS

- Wideband Signal Routing and Multiplexing
- High-end Video Systems
- µP-controlled Systems
- Direct Coupled Systems
- ATE Systems
- Digital Video Routing

DESCRIPTION

The DG884 is a digitally selectable 8 x 4 crosspoint array designed for wideband operation. On-chip TTL-compatible crosspoint selection logic and latches with data readback are included to simplify the interface to a microprocessor data bus. The low ON-resistance and low capacitance of the DG884 make it ideal for wideband data multiplexing and video and audio signal routing in analog and/or digital video systems. An optional negative supply pin allows the handling of bipolar signals without dc biasing.

The DG884 is built on a D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic, drivers and latches. The low-capacitance DMOS FETs are in a "T" configuration to achieve extremely high levels of OFF isolation. Crosstalk is reduced to −85 dB at 5 MHz by including a ground line between adjacent signal input pins.

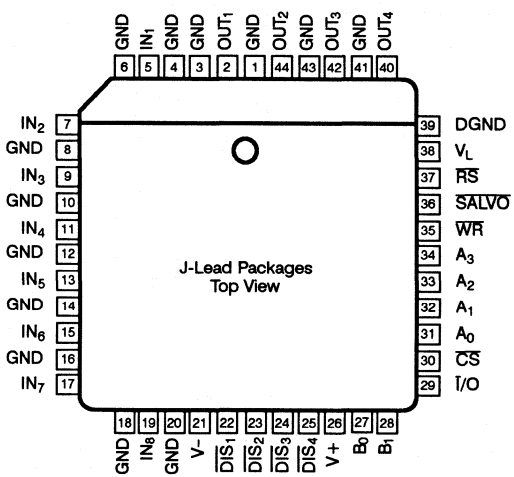
The DG884 is available in the 44-pin plastic and ceramic leaded chip carrier for operation over the industrial, D suffix (−40 to 85°C) temperature range, and for military, A suffix (−55 to 125°C) operation.

For additional information please refer to Applications Note AN90-3.

PIN CONFIGURATIONS

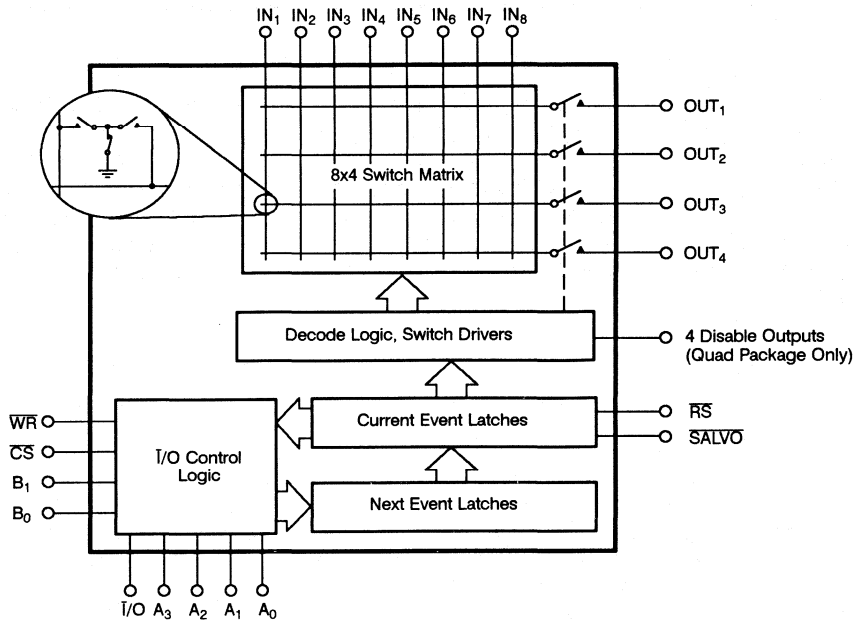
Quad J-Lead Packages

Order Numbers:
PLCC-44: DG884DN
CLCC-44: DG884AM/883



6

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLES

$\overline{RS}$	I/O	$\overline{CS}$	$\overline{WR}$	$\overline{SALVO}$	ACTIONS
1	0	1	↑	1	No Change to next event latches
1	0	0	↑	1	Next event latches loaded as defined in table above
1	0	0	0	1	Next event latches are transparent.
1	0	0	↓	1	Next event data latched
1	0	X	1	↑	Data in all next event latches is simultaneously loaded into the current event latches, i.e., all new crosspoint addresses change simultaneously when $\overline{SALVO}$ goes low.
1	0	X	1	↓	Current event data latched in
1	0	0	X	0	Current event latches are transparent
1	0	0	0	0	Both next and current event latches are transparent
1	1	1	1	1	A_0, A_1, A_2, A_3 – High impedance
1	1	0	1	1	A_0, A_1, A_2, A_3 become outputs and reflect the contents of the current event latches. B_0, B_1 determine which current event latches are being read
0	X	X	1	1	All crosspoints opened (but data in next event latch is preserved)

ALL OTHER STATES ARE NOT RECOMMENDED

NOTE: When $\overline{WR}$ = 0 next event latches are transparent. Each crosspoint is addressed individually, e.g., to connect IN_1 to OUT_1 thru OUT_4 requires A_0, A_1, A_2 = 0 to be latched with each combination of B_0, B_1. When $\overline{RS}$ = 0, all four $\overline{DIS}$ outputs pull low simutaneously.

TRUTH TABLES (Cont'd)

$\overline{WR}$	B_1	B_0	A_3	A_2	A_1	A_0	NEXT EVENT LATCHES
0	0	0	1	0	0	0	IN_1 to OUT_1 Loaded
				0	0	1	IN_2 to OUT_1 Loaded
				0	1	0	IN_3 to OUT_1 Loaded
				0	1	1	IN_4 to OUT_1 Loaded
				1	0	0	IN_5 to OUT_1 Loaded
				1	0	1	IN_6 to OUT_1 Loaded
				1	1	0	IN_7 to OUT_1 Loaded
				1	1	1	IN_8 to OUT_1 Loaded
			0	X	X	X	Turn Off OUT_1 Loaded
	0	1	1	0	0	0	IN_1 to OUT_2 Loaded
				0	0	1	IN_2 to OUT_2 Loaded
				0	1	0	IN_3 to OUT_2 Loaded
				0	1	1	IN_4 to OUT_2 Loaded
				1	0	0	IN_5 to OUT_2 Loaded
				1	0	1	IN_6 to OUT_2 Loaded
				1	1	0	IN_7 to OUT_2 Loaded
				1	1	1	IN_8 to OUT_2 Loaded
			0	X	X	X	Turn Off OUT_2 Loaded
	1	0	1	0	0	0	IN_1 to OUT_3 Loaded
				0	0	1	IN_2 to OUT_3 Loaded
				0	1	0	IN_3 to OUT_3 Loaded
				0	1	1	IN_4 to OUT_3 Loaded
				1	0	0	IN_5 to OUT_3 Loaded
				1	0	1	IN_6 to OUT_3 Loaded
				1	1	0	IN_7 to OUT_3 Loaded
				1	1	1	IN_8 to OUT_3 Loaded
			0	X	X	X	Turn Off OUT_3 Loaded
	1	1	1	0	0	0	IN_1 to OUT_4 Loaded
				0	0	1	IN_2 to OUT_4 Loaded
				0	1	0	IN_3 to OUT_4 Loaded
				0	1	1	IN_4 to OUT_4 Loaded
				1	0	0	IN_5 to OUT_4 Loaded
				1	0	1	IN_6 to OUT_4 Loaded
				1	1	0	IN_7 to OUT_4 Loaded
				1	1	1	IN_8 to OUT_4 Loaded
			0	X	X	X	Turn Off OUT_4 Loaded

ALL OTHER STATES ARE NOT RECOMMENDED

NOTE: When $\overline{WR}$ = 0 next event latches are transparent. Each crosspoint is addressed individually, e.g., to connect IN_1 to OUT_1 thru OUT_4 requires A_0, A_1, A_2 = 0 to be latched with each combination of B_0, B_1. When $\overline{RS}$ = 0, all four $\overline{DIS}$ outputs pull low simutaneously.

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ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... -0.3 V to 21 V

V+ to V- ..... -0.3 V to 21 V

V- to GND ..... -10 V to 0.3 V

Digital Inputs ..... (V-) - 0.3 V to (V+) + 0.3 V
or 20 mA, whichever occurs first

V_S, V_D ..... (V-) - 0.3 V to (V+) + 14 V
or 20 mA, whichever occurs first

CURRENT (any terminal) Continuous ..... 20 mA

CURRENT (S or D) Pulsed 1 ms 10% duty ..... 40 mA

Storage Temperature (A Suffix) ..... -65 to 150°C
(D Suffix) ..... -65 to 125°C

Operating Temperature (A Suffix) ..... -55 to 125°C
(D Suffix) ..... -40 to 85°C

Power Dissipation (Package)*

44-Pin Quad J Lead Plastic *** ..... 450 mW

44-Pin Quad J Lead Hermetic** ..... 1200 mW

*All Leads welded or soldered to PC board

**Derate 16 mW/°C above 75°C

***Derate 6 mW/°C above 75°C

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V V_L = 5 V, $\overline{RS}$ = 2.4 V $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, I/O = 0.8 V	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
ANALOG SWITCH									
Analog Signal Range[e]	V_{ANALOG}	V- = -5 V	Full		-5	8	-5	8	V
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = -10 mA, V_D = 0 V V_{AIH} = 2.4 V, V_{AIL} = 0.8 V	Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(ON)}$	Sequence Each Switch On	Room			9		9	
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 8 V, V_D = 0 V $\overline{RS}$ = 0.8 V	Room Full		-20 -200	20 200	-20 -200	20 200	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_S = 0 V, V_D = 8 V $\overline{RS}$ = 0.8 V	Room Full		-20 -200	20 200	-20 -200	20 200	
Total Switch ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = V_D = 8 V	Room Full		-20 -2000	20 2000	-20 -200	20 200	
DIGITAL INPUT/OUTPUT									
Input Voltage High	V_{AIH}		Full		2		2		V
Input Voltage Low	V_{AIL}		Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V or 2 V or 15 V	Room Full	0.1	-1 -10	1 10	-1 -10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V	Full	-300					
		V_{AO} = 0.4 V	Full	300					
$\overline{DIS}$ Pin Sink Current	I_{DIS}		Room	1.5					mA
DYNAMIC CHARACTERISTICS									
ON State Input Capacitance[c]	$C_{S(ON)}$	1 In, 1 Out, See Figure 11	Room	30				40	pF
		1 In, 4 Out, See Figure 11	Room	120				160	
OFF State Input Capacitance[c]	$C_{S(OFF)}$	See Figure 11	Room	8		20		20	
OFF State Output Capacitance[c]	$C_{D(OFF)}$		Room	10		20		20	
Break-Before-Make Interval	t_{OPEN}	See Figure 5	Full			10		10	ns
$\overline{SALVO}$ Turn ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF 50% Control to 90% Output	Room Full			300 500		300 500	
$\overline{SALVO}$ Turn OFF Time	t_{OFF}	See Figure 3	Room Full			150 300		150 300	
Charge Injection	Q	See Figure 6	Room	-100					pC
Matrix Disabled Crosstalk (See Figure 9)	$XTALK_{(DIS)}$	R_{IN} = R_L = 75 Ω f = 5 MHz	Room	-82					dB
Adjacent Input Crosstalk (See Figure 10)	$XTALK_{(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz	Room	-85					
All Hostile Crosstalk[c] (See Figure 8)	$XTALK_{(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ f = 5 MHz	Room	-66					
Bandwidth	BW	R_L = 50 Ω, See Figure 7	Room	300					MHz

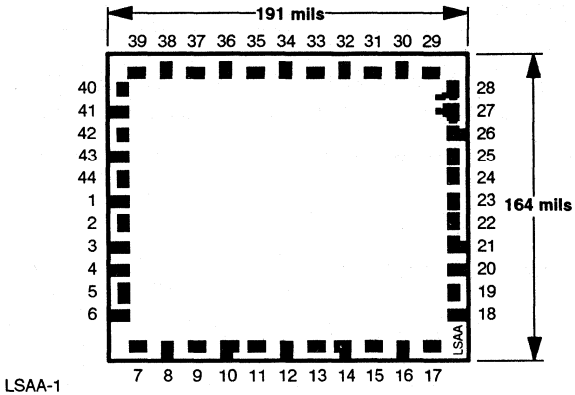
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 15 V, V- = -3 V V_L = 5 V, $\overline{RS}$ = 2.4 V $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, I/O = 0.8 V	TEMP[f]	TYP[d]	A SUFFIX -55 to 125°C MIN[b]	A SUFFIX -55 to 125°C MAX[b]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
POWER SUPPLIES									
Positive Supply Current	I+		Room Full	1.5		3 6		3 6	mA
Negative Supply Current	I-		Room Full	-1.5	-3 -5		-3 -5		
Digital GND Supply Current	I_{DG}	All Channels ON or OFF with address inputs at GND or 2 V	Full	-275	-750		-750		µA
Logic Supply Current	I_L		Full	200		500		500	
Functional Check of Max Operating Supply Voltage Range	V+ to V-	See Figure 12 Functional Test Only	Full		13	18	13	18	V
	V- to GND		Full		-5.5	-3	-5.5	-3	
	V+ to GND		Full		10	15	10	15	
MINIMUM INPUT TIMING REQUIREMENTS									
Write Data Time	t_{WD}	See Figure 1	Full		50				ns
Minimum Pulse Width	t_{MPW}		Full	200					
Data Write Time	t_{DW}		Full		100				
Chip Select Valid Time	t_{CSV}		Full		100				
Chip Select Hold Time	t_{CSH}		Full		100				
Minimum $\overline{SALVO}$ Width	t_{MSW}		Full		200				
SALVO Hold Time	t_{SH}		Full		200		200		
Input Output Time	t_{IO}		Room	200					
Address Output Time	t_{AO}		Room	200					
Reset to $\overline{SALVO}$	t_{RS}		Full		50		50		
Address Tristate Time	t_{AZ}		Room	50					
Address Input Time	t_{AI}		Room	200					

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Analog signal range is measured from the GND pin to the designated Source (input) pin, and indicates the limits of functionality. Performance limits are only guaranteed for stated test conditions.
f. Room = 25°C, Full = as determined by the operating temperature suffix.

6

DIE TOPOGRAPHY

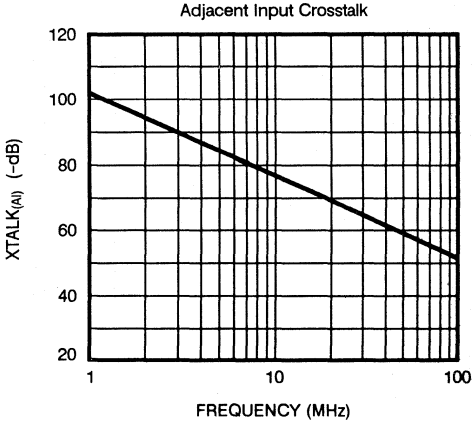


LSAA-1
728 PMOS Transistors
3 p+ resistors
3 NPN Transistors
821 NMOS Transistors
20 diodes

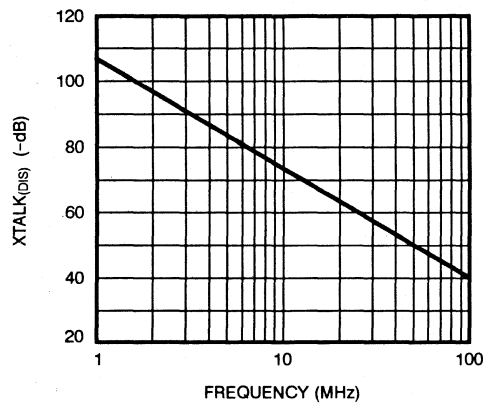
Pad No.	Function	Pad No.	Function
1	GND	23	$\overline{DIS_2}$
2	OUT_1	24	$\overline{DIS_3}$
3	GND	25	$\overline{DIS_4}$
4	GND	26	V+
5	IN_1	27	B_0
6	GND	28	B_1
7	IN_2	29	$\overline{I/O}$
8	GND	30	$\overline{CS}$
9	IN_3	31	A_0
10	GND	32	A_1
11	IN_4	33	A_2
12	GND	34	A_3
13	IN_5	35	$\overline{WR}$
14	GND	36	$\overline{SALVO}$
15	IN_6	37	$\overline{RS}$
16	GND	38	V_L
17	IN_7	39	DGND
18	GND	40	OUT_4
19	IN_8	41	GND
20	GND	42	OUT_3
21	V- (Substrate)	43	GND
22	$\overline{DIS_1}$	44	OUT_2

TYPICAL CHARACTERISTICS

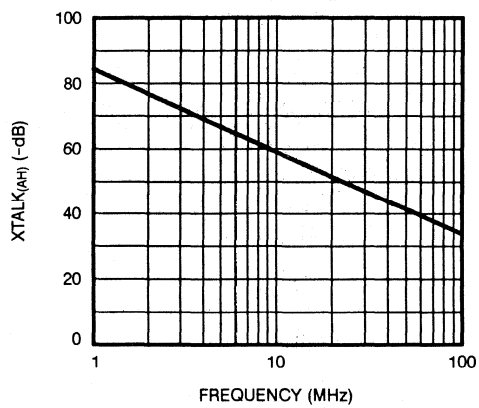
Adjacent Input Crosstalk



Matrix Disabled Crosstalk



All Hostile Crosstalk



TIMING REQUIREMENTS

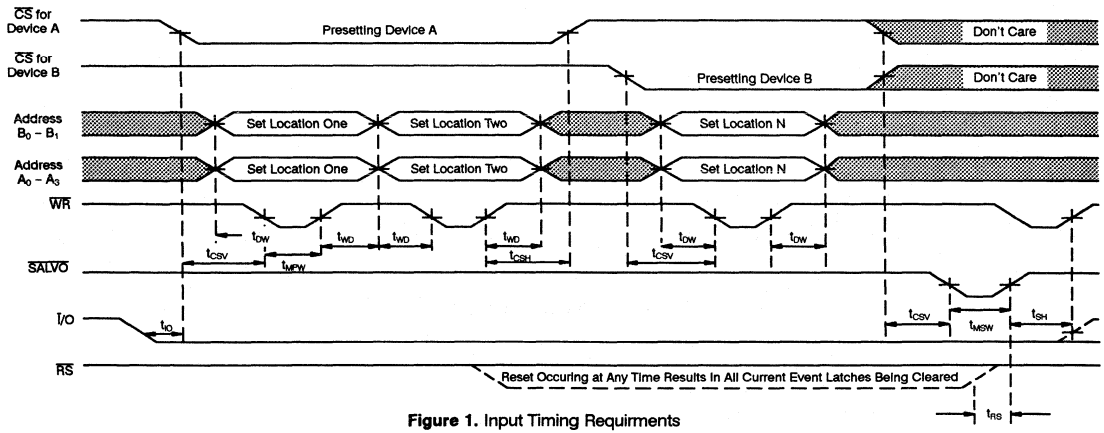


Figure 1. Input Timing Requirments

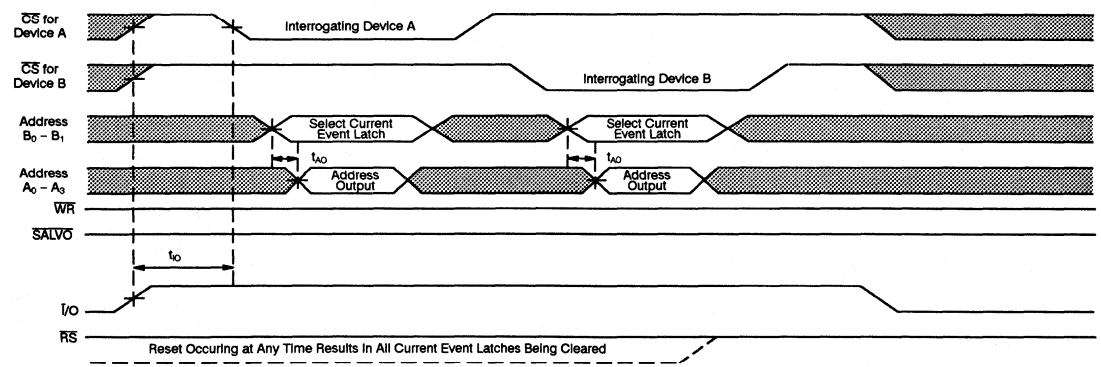


Figure 2. Output Timing Requirments

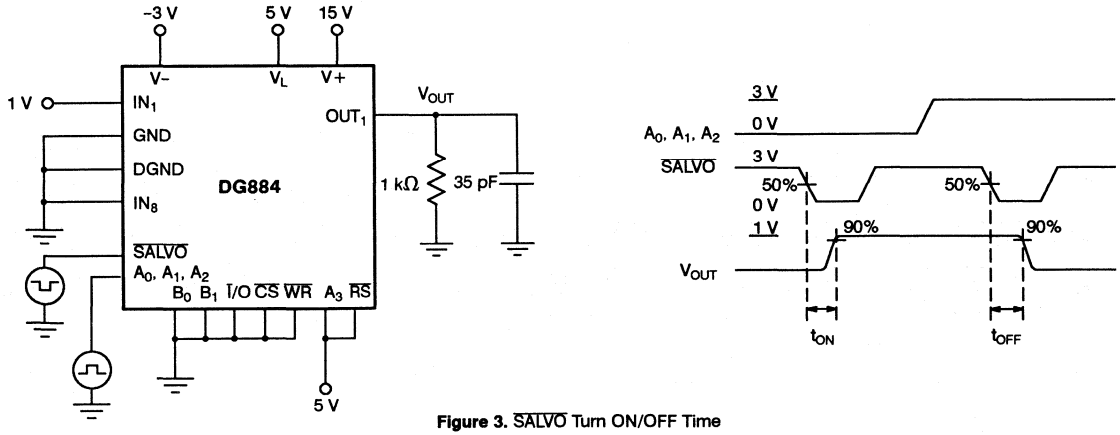


Figure 3. $\overline{\text{SALVO}}$ Turn ON/OFF Time

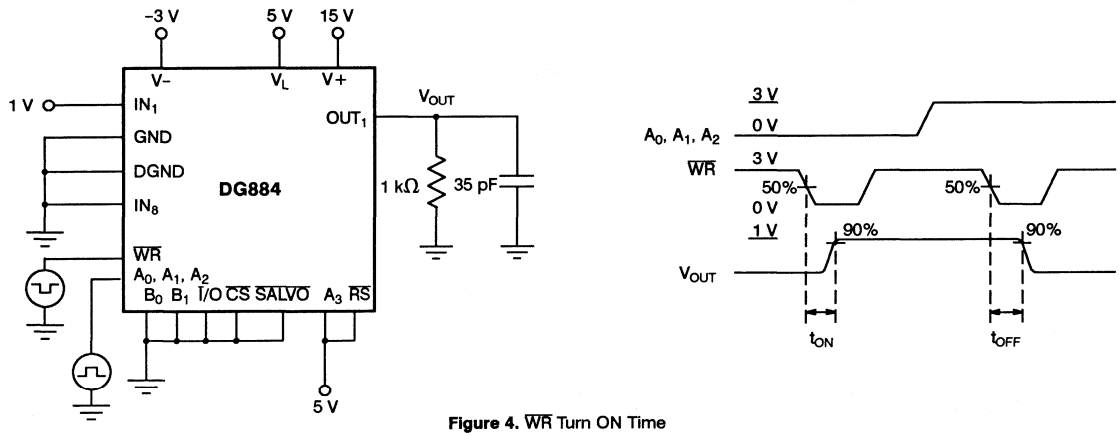


Figure 4. $\overline{\text{WR}}$ Turn ON Time

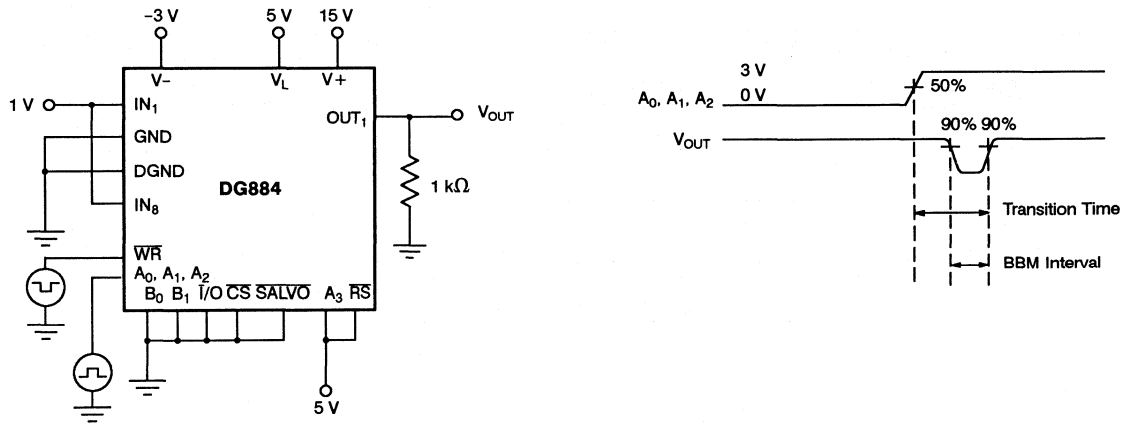


Figure 5. Transition Time and Break-Before-Make Interval

TEST CIRCUITS (Cont'd)

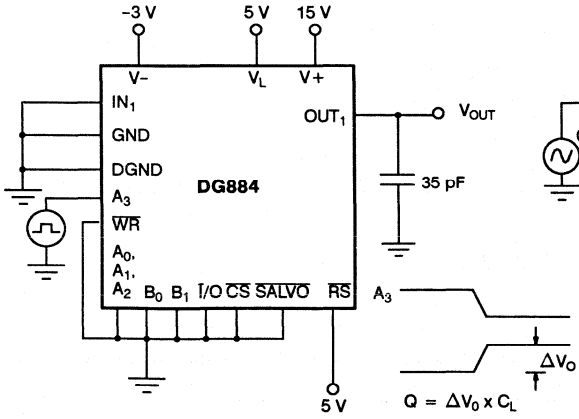


Figure 6. Charge Injection

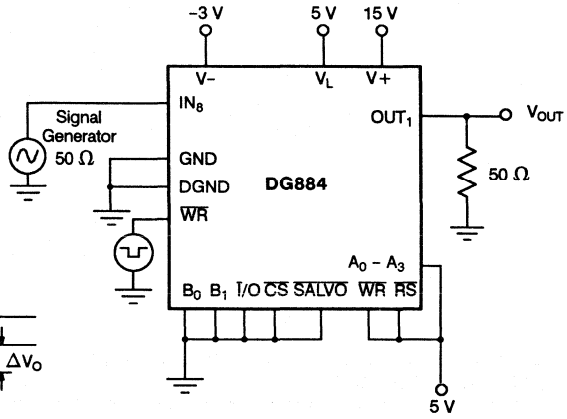


Figure 7. -3 dB Bandwidth

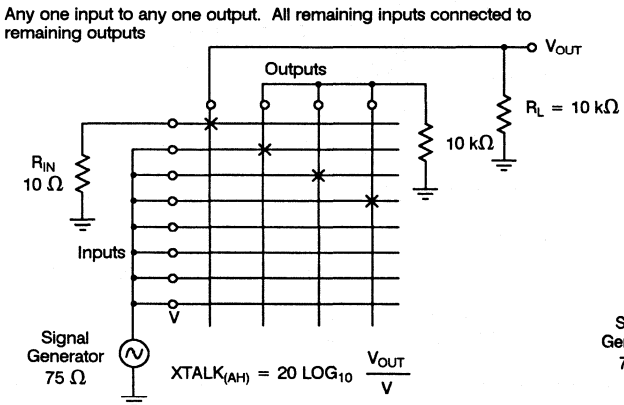


Figure 8. All Hostile Crosstalk - $XTALK_{(AH)}$

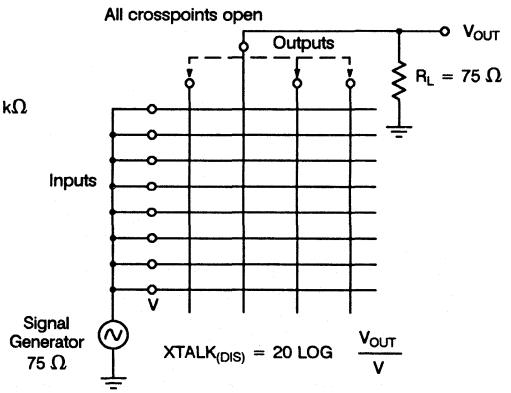


Figure 9. Matrix Disabled Crosstalk - $XTALK_{(DIS)}$

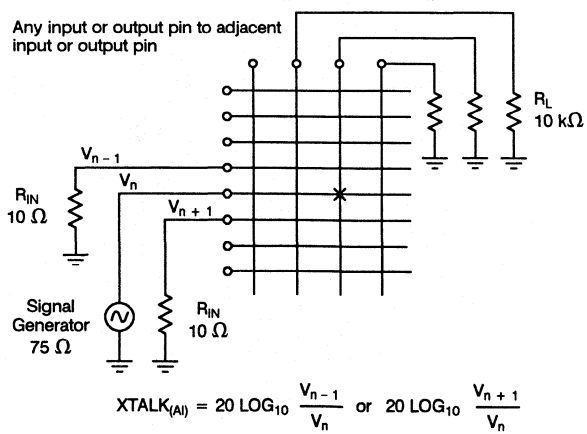


Figure 10. Adjacent Input Crosstalk - $XTALK_{(AI)}$

ON-STATE AND OFF-STATE CAPACITANCES

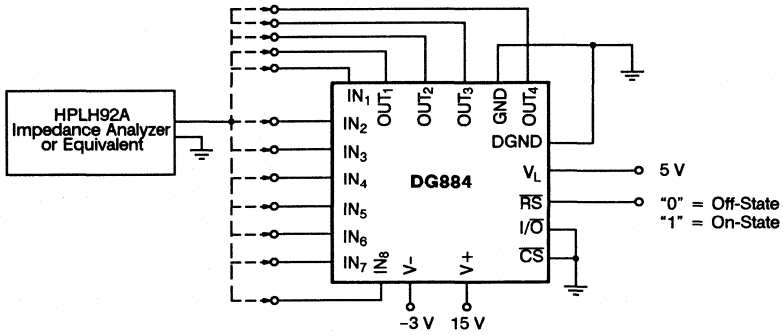
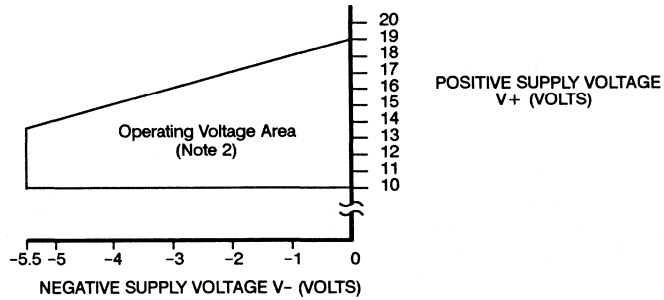


Figure 11.

OPERATING VOLTAGE RANGE



Note:
1. Both V+ and V- must have decoupling capacitors mounted as close as possible to the device pins. Typical decoupling capacitors would be 10 µF tantalum bead in parallel with 0.1 µF ceramic disc.
2. Production tested with V+ = 15 V and V- = -3.0 V. Readback functions for V- $\leq$ -3 V only.
3. At V_L = 5 V ± 10%, 0.8/2.0 V TTL compatibility is maintained over the entire operating voltage range.

Figure 12.

BURN-IN CIRCUIT - 44-LEAD PLCC

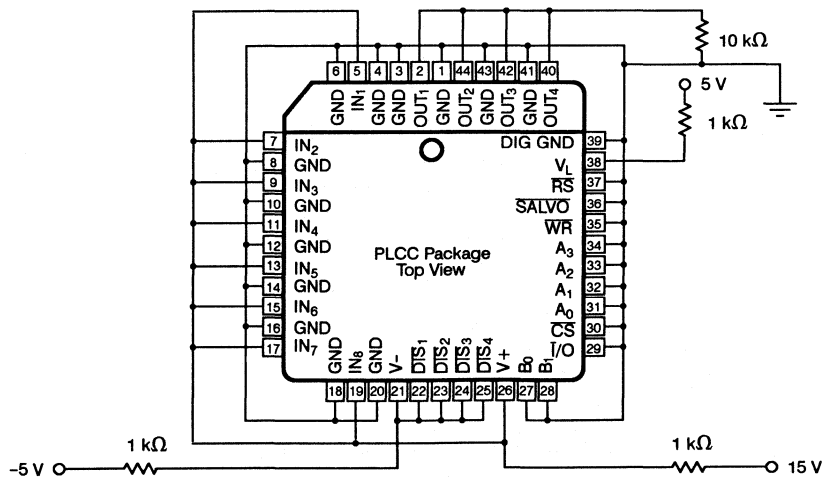


Figure 13.

PIN DESCRIPTION

SYMBOL	DESCRIPTION
GND	Analog Signal Ground
DGND	Digital Ground
V+	Positive Supply Voltage
V-	Negative Supply Voltage
V_L	Logic Supply Voltage
IN_1 to IN_8	8 Analog Input Channels
OUT_1 to OUT_4	4 Analog Output Channels
I/O	Determines whether data is being written into the next event latches or read from the current event latches
$\overline{CS}$	Chip Select
A_0, A_1, A_2, A_3	Input Address Bus
B_0, B_1	Output Address Bus
$\overline{WR}$	Write command that latches A_0, A_1, A_2, A_3 into the next event latches
$\overline{SALVO}$	Master write command, that in one action, transfers all the data from next event latches into current event latches
$\overline{RS}$	Reset
$\overline{DIS_1}$ thru $\overline{DIS_4}$	Open drain disable outputs to power down external video buffers

APPLICATIONS

DEVICE DESCRIPTION

The DG884 is the world's first monolithic wideband crosspoint array that operates from dc to > 100 MHz. The DG884 offers the ability to route any one of eight input signals to any one of four output pins. Any input can be routed to one, two, three or four outputs simultaneously with no risk of shorting inputs together (guaranteed by design).

Each crosspoint is configured as a "T" switch in which DMOS FETs are used due to their excellent low resistance and low capacitance characteristics. Each output line has a series switch that minimizes the capacitive loading when the output is off.

INTERFACING

The DG884 was designed to allow complex matrices to be developed while maintaining a simple control interface. The status of the I/O pin determines whether the DG884 is being written to or read from (see Figures 1 and 2).

In order to WRITE to an individual device, $\overline{CS}$ and I/O need to be low, while $\overline{RS}$, $\overline{WR}$ and $\overline{SALVO}$ must be high. The input to output path is selected by using address inputs A_0 through A_3 to define the input line and address inputs B_0 and B_1 to define the output line. That is, The input defined by A_0 through A_3 is electrically connected to the output defined by B_0, B_1. This chosen path is loaded into the Next Event latches when $\overline{WR}$ goes low and returns high again. This operation is repeated up to three more times if other crosspoint connections need to be changed.

Upon completing all crosspoint connections that are to be changed in a single device, other DG884s can be similarly preset by taking the $\overline{CS}$ pin low on the appropriate device. When all DG884s are preset, the Current Event latches are simultaneously changed by a single $\overline{SALVO}$ command applied to all devices. In this manner the crosspoint configuration of any number of devices can be simultaneously changed.

DIS OUTPUTS

Four open drain disable outputs are provided to control external line drivers or to provide visual or electrical signaling. For example, any or all of the $\overline{DIS}$ outputs can directly interface with a Siliconix Si582 Video Amplifier to place it into a high impedance, low-power standby mode when the corresponding output is not being used. (See Figure 15).

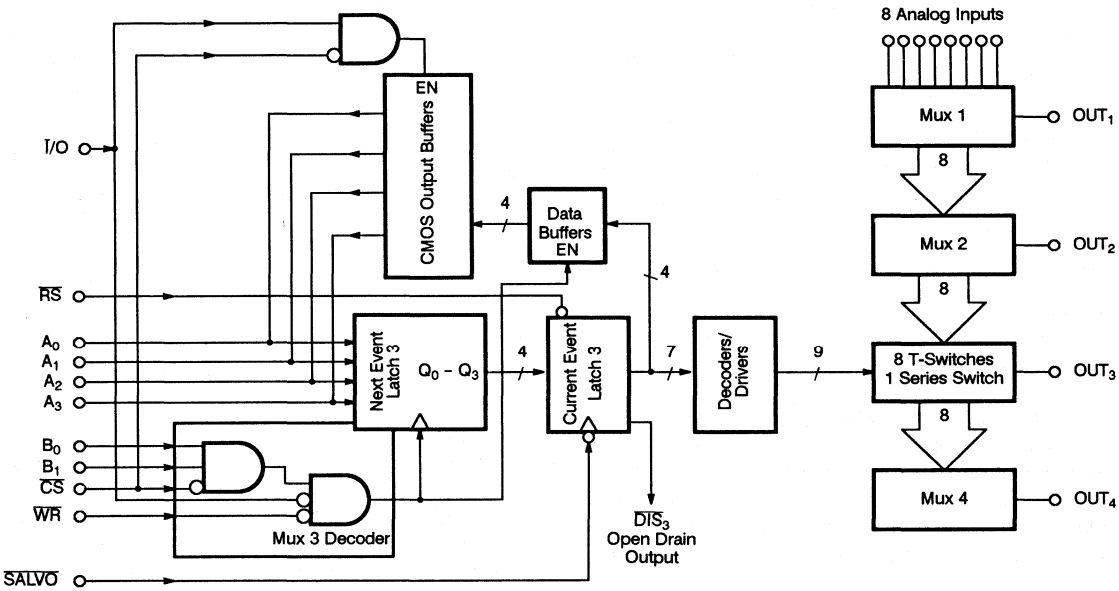
RESET

The reset function ($\overline{RS}$ input) allows the resetting of all crosspoints to a known state (open). At power up, the reset facility may be used to guarantee that all switches are open. It should be noted that $\overline{RS}$ clears the Current Event latches, but the Next Event latches remain unchanged. This useful facility allows the user to return the matrix to its previous state (prior to reset) by simply applying the $\overline{SALVO}$ command. Alternatively, the user can reprogram the Next Event latches, and then apply the $\overline{SALVO}$ command to reconfigure the matrix to a new state.

6

READBACK

The I/O facility enables the user to write data to the next event latches or to read the contents of the current event latches. This feature permits the central controller to periodically monitor the state of the matrix. If a power loss to the controller occurs, the readback feature helps the matrix to recover rapidly. It also offers a means to perform PC board diagnostics both in production and in system operation.



One of Four Blocks of Logic/Latches Shown

Figure 14. Control Circuitry

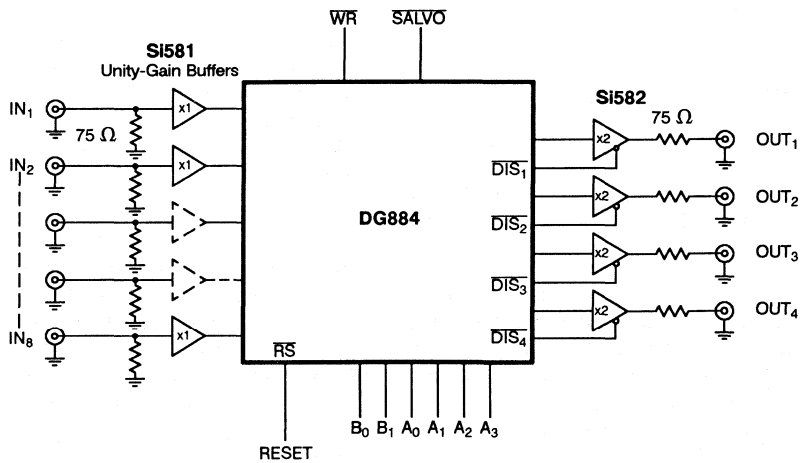


Figure 15. Fully Buffered 8 x 4 Crosspoint. The $\overline{DIS}$ Outputs Are Used to Power Down the Si582 Amplifiers

POWER SUPPLIES AND DECOUPLING

A useful feature of the DG884 is its power supply flexibility. It can be operated from dual supplies, or a single positive supply (V- connected to 0 V) if required. Allowable operating voltage ranges are shown in Figure 12.

Note that the analog signal must not go below V- by more than 0.3 V (see absolute maximum ratings). However, the addition of a V- pin has a number of advantages:

1) It allows flexibility in analog signal handling, i.e. with V- = -5 V and V+ = 15 V, up to ±5 V ac signals can be accepted.

2) The value of ON capacitance ($C_{S(ON)}$) may be reduced by increasing the value of V-. It is useful to note that optimum video differential phase and gain occur when V- is -3 V. Note that V+ has no effect on $C_{S(ON)}$.

3) V- eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established rf design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG884 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

(a) Decoupling capacitors should be incorporated on all power supply pins (V+, V-, V_L).

(b) They should be mounted as close as possible to the device pins.

(c) Capacitors should have good frequency characteristics - tantalum bead and/or ceramic disc types are suitable.

Recommended decoupling capacitors are 1 to 10 µF tantalum bead, in parallel with 100 nF ceramic or polyester.

(d) Additional high frequency protection may be provided by 51 Ω carbon film resistors connected in series with the power supply pins (see Figure 16).

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with +5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

A typical switching threshold versus V_L is shown in Figure 17.

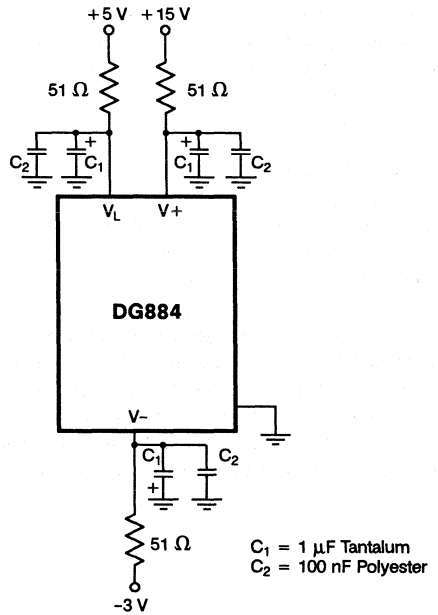


Figure 16. DG884 Power Supply Decoupling

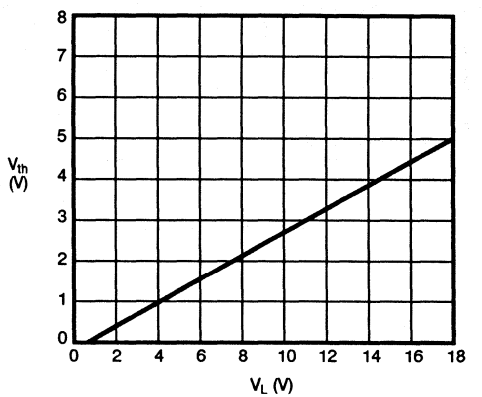


Figure 17. Switching Threshold Voltage vs. V_L

6

These devices feature an address readback (Tally) facility whereby the last address written to the device may be read by the system. This allows improved status monitoring and hand shaking without additional external components.

When the I/O assigns the address output condition, the address output can sink or source current for logic low and high, respectively. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Note: To protect against latchup, V_L must not exceed V+ by more than 0.3 V in operation or during power supply on/off sequencing. This is easily achieved by generating V_L from V+ using a Zener or a resistor divider network as shown in Figure 18. When an external V_L is available, the alternative simple protection circuit shown in Figure 19 should be used.

LAYOUT

The PLCC package pinout is optimized so that large crosspoint arrays can be easily implemented with a minimum number of PCB layers (See Figure 20). Crosstalk is minimized and off-isolation is optimized by having ground pins located adjacent to each input and output signal pins. Optimum off-isolation and low crosstalk performance can only be achieved by the proper use of rf layout techniques: avoid sockets, use ground planes, avoid ground loops, bypass the power supplies with high frequency type capacitors (low ESR, low ESL), use stripelines to maintain transmission line impedance matching.

For additional information please refer to Application Note AN90-3.

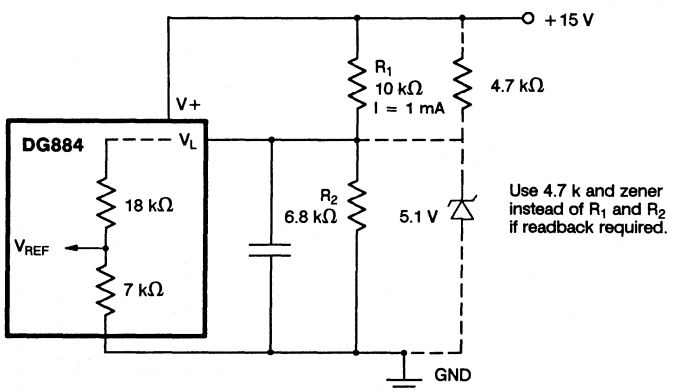


Figure 18. V_L Generated from V+

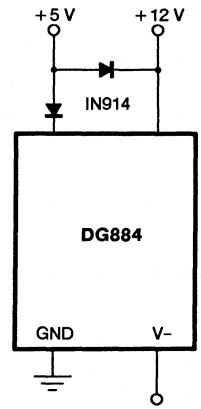


Figure 19. External Diodes Prevent Latchup

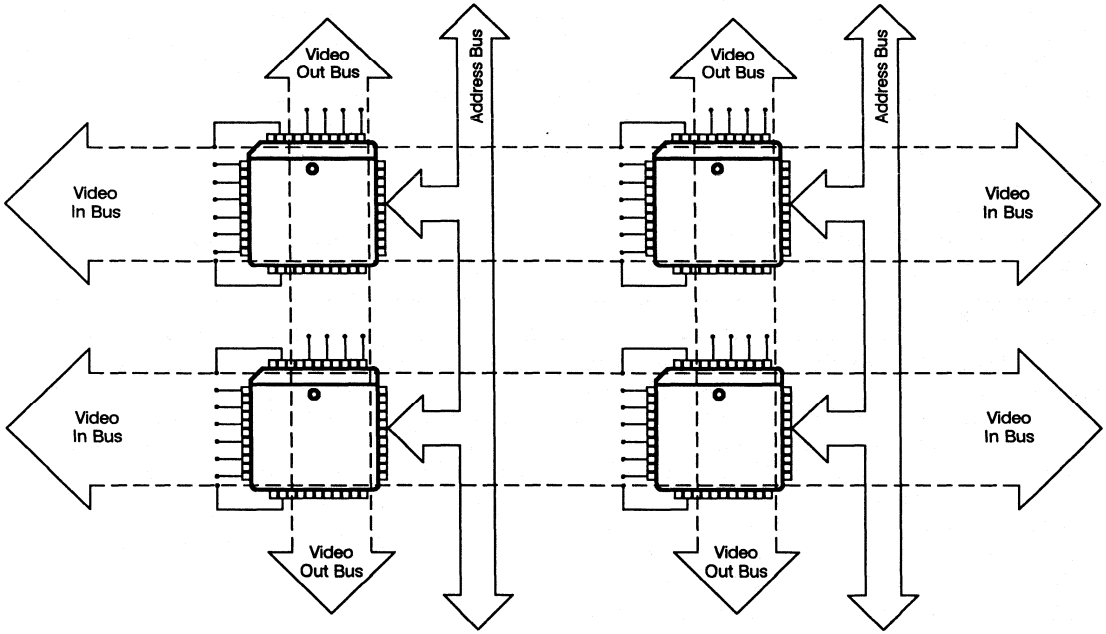


Figure 20. 16 x 8 Expandable Crosspoint Matrix Using DG884

6

DG894
SCART / S-VHS WIDEBAND VIDEO SWITCH

Siliconix incorporated

FEATURES

- Wide Bandwidth (100 MHz)
- Very Low Crosstalk (–70 dB at 5 MHz)
- I²C Bus Interface or dc Switching Permitted
- CMOS Compatible
- Fast Switching (t_{ON} <200 ns)
- Low $r_{DS(ON)}$ <100 Ω
- Single Supply Capability
- ESDS Protected > ±4000 V

BENEFITS

- Low Insertion Loss
- Improved System Performance
- Reduced Board Space
- Reduced Power Consumption
- Easily Interfaced
- Future System Expansion (via I²C Bus)

APPLICATIONS

- Component Video Switching
- High Frequency Crosspoints
- Video Routing
- Digital TV
- ATE

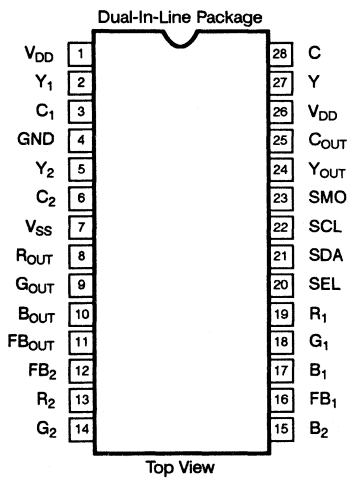
DESCRIPTION

The DG894 is a high performance monolithic switch array designed for switching wide bandwidth analog and digital signals. On-chip address decoding is included to simplify signal source selection. The low ON resistance and low capacitance of the DG894 make it ideal for wideband data and video/audio signal routing. An optional negative supply allows the handling of bipolar signals without dc biasing. Switch control can be through the two-wire I²C bus or through direct addressing.

The DG894 is built on the Siliconix proprietary D/CMOS process that combines n-channel DMOS switching FETs with low-power CMOS control logic and drivers. Low-capacitance DMOS FETs are used to achieve high levels of OFF isolation at moderate cost. Crosstalk is reduced to –70 dB at 5 MHz on the DG894.

The DG894 is available in 28-pin plastic DIP package for operation over the industrial (–40 to 85°C) temperature range.

PIN CONFIGURATION



Order Number:

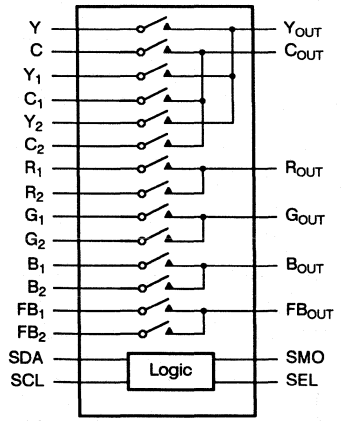
Plastic: DG894DJ

NOTE: The Y and C inputs (or outputs) may be interchanged, or used for other signals as desired. Similarly, the R, G, B, and FB inputs (or outputs) may be used for Y, U, V signals etc., as appropriate.

Purchase of Siliconix I²C components conveys a license under the Philips I²C patent to use the components in the I²C system provided the system conforms to the I²C specifications defined by Philips.

Preliminary

FUNCTIONAL BLOCK DIAGRAM



SCART is an acronym for the French Syndicat des Constructeurs d'Appareils Radio recepteur et Television (Syndicate of Radio and Television Equipment Manufacturers).

TRUTH TABLE

TRUTH TABLE				
SMO	SEL	SDA	SCL	FUNCTION
0	0	I^2C	Bus Operation, Address A0 = "1"	
0	1	I^2C	Bus Operation, Address A0 = "0"	
1	0	0	0	All Switches OFF
1	0	0	1	Y, C
1	0	1	0	Y_1 , C_1
1	0	1	1	Y_2, C_2
1	1	0	0	$SCART_1$
1	1	0	1	$SCART_2$
1	1	1	0	$SCART_1$, Y_1, C_1
1	1	1	1	$SCART_2$, Y_2, C_2
NOTE: $SCART_1$ indicates R_1, G_1, B_1, FB_1				

ABSOLUTE MAXIMUM RATINGS

V+ to GND ..... −0.3 V to +19 V
V+ to V− ..... −0.3 V to +19 V
V− to GND ..... −10 V to +0.3 V
Digital Inputs ..... GND −0.3 V to (V+) +0.3 V
or 20 mA, whichever occurs first
Signal Inputs ..... V_{SS} −0.3 V to +8 V
or 20 mA, whichever occurs first
Continuous Current (Any Terminal) ..... 20 mA
Current (Any Terminal) Pulsed 1 mS,
10% Duty Cycle Max ..... 40 mA
Storage Temperature (D Suffix) ..... −65 to 125°C
Operating Temperature (D Suffix) ..... −40 to 85°C
Power Dissipation (Package)*
28-Pin Plastic DIP ..... 625 mW

*All leads welded or soldered to PC board

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = −5 V, V_{INH} = 3 V, V_{INL} = 1.5 V[f]	TEMP[g]	TYP[d]	D SUFFIX −40 to 85°C MIN[b]	D SUFFIX −40 to 85°C MAX[b]	UNIT
ANALOG SWITCH							
Analog Signal Range[e]	V_{ANALOG}	V_{DD} = 12 V, V_{SS} = GND	Full		0	4	V
		V_{DD} = 12 V, V_{SS} = −5 V	Full		−2	2	
Drain-Source ON-Resistance	$r_{DS(ON)}$	I_S = −10 mA, V_D = 0 V	Room Full			100 150	Ω
Resistance Match Between Channels	$\Delta r_{DS(ON)}$		Room	10			
Source OFF Leakage Current	$I_{S(OFF)}$	V_S = 4 V, V_D = 0 V	Room Full	−0.05	−10 −100	10 100	nA
Drain OFF Leakage Current	$I_{D(OFF)}$	V_D = 4 V, V_S = 0 V	Room Full	−0.05	−10 −100	10 100	
Total Switch ON Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = V_S = 4 V	Room Full	−0.07	−10 −100	10 100	

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SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V_{DD} = 12 V, V_{SS} = -5 V V_{INH} = 3 V, V_{INL} = 1.5 V[f]	TEMP[g]	TYP[d]	D SUFFIX -40 to 85°C MIN[b]	D SUFFIX -40 to 85°C MAX[b]	UNIT
INPUT							
Input Voltage High	V_{INH}		Full		3.0		V
Input Voltage Low	V_{INL}		Full			1.5	
Input Current	I_{IN}	V_{IN} = GND or V_{DD}	Room Full	0.05	-1 -20	1 20	µA
Output Voltage Low	V_{OL}	Pin 21, During Acknowledge I_{OL} = 3 mA	Room			0.4	V
DYNAMIC							
Input Capacitance	C_{in}	Pin 21, 22	Room			10	pF
ON State Input Capacitance[c]	$C_{S(ON)}$	V_S = V_D = 0 V	Room	14		20	
OFF State Input Capacitance[c]	$C_{S(OFF)}$	V_S = 0 V	Room	6		10	
OFF State Output Capacitance[c]	$C_{D(OFF)}$	V_D = 0 V	Room	4		8	
Bandwidth	BW	R_L = 50 Ω, See Test Circuit	Room		100		MHz
Turn ON Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, 50% to 90%	Room			200	ns
Turn OFF Time	t_{OFF}	See Switching Time Test Circuit	Room			180	
SCL Max Clock Frequency	$F_{SCL(MAX)}$		Full		100		kHz
Component Crosstalk	$XTALK_{(CO)}$	R_{IN} = 10 Ω, R_L = 1 kΩ	Room	-70			dB
Channel Crosstalk	$XTALK_{(CH)}$	f = 5 MHz, See Test Circuit	Room	-70			
SUPPLY							
Positive Supply Current	I+	All Control Inputs High or Low	Room Full			8 10	mA
Negative Supply Current	I-		Room Full		-8 -10		

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Analog signal range is measured from the GND pin to the designated Source (input) pin.
f. V_{IN} = Input voltage to perform proper function.
g. Room = 25°C, Full = as determined by the operating temperature suffix.

TEST CIRCUITS

Switching output waveform shown for V_S = Constant with logic input waveform as shown.
V_O is the steady state output with switch ON.
Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

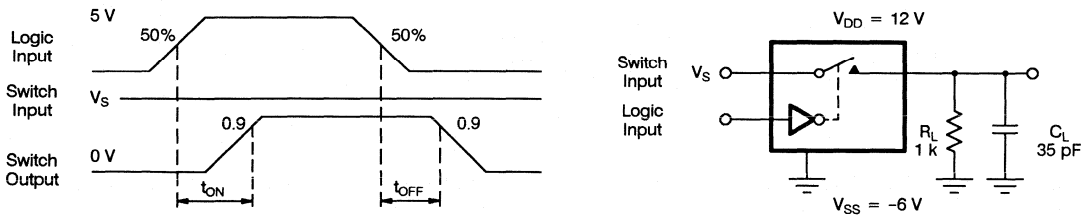

Figure 1. Switching Time

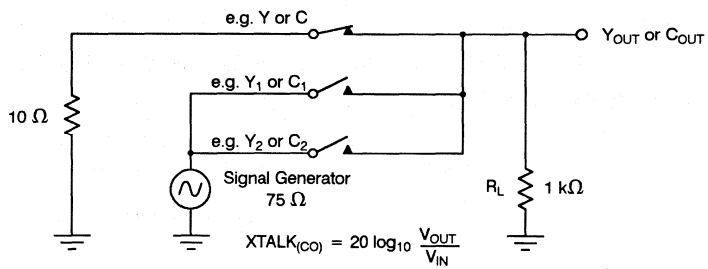

Figure 2. Component Crosstalk - $XTALK_{(CO)}$

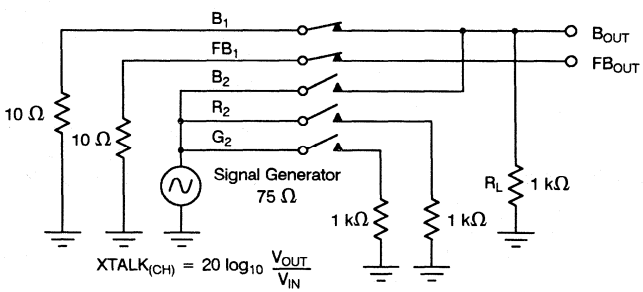

Figure 3. Channel Crosstalk - $XTALK_{(CH)}$

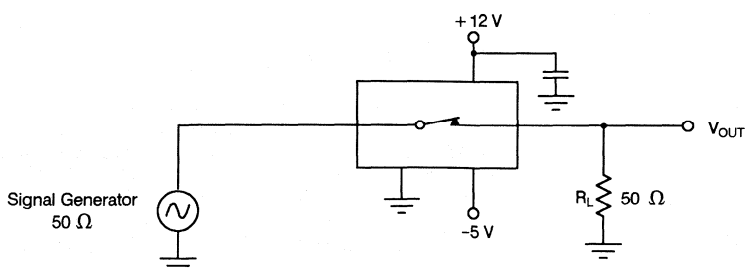

Figure 4. Bandwidth

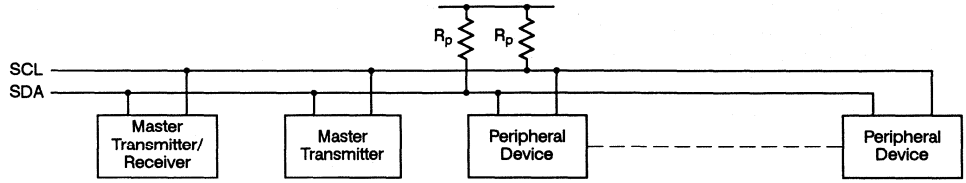

Figure 5.

CHARACTERISTICS OF THE I²C BUS

The I²C Bus interface is ideally suited for communication between different ICs or modules. Its salient features are:

- Two wire bidirectional serial bus
  - Serial data (SDA) and serial clock (SCL) lines
- Any number of interfaces may be connected to the bus
  - Limited only by total capacitance of 400 pF
  - Each pin on bus limited to 10 pF capacitance
  - Input levels:
    V_{IL} max = 1.5 V (fixed supply operation)
    V_{IH} min = 3 V (fixed supply operation)
    V_{IL} max = 0.3 V_{DD} (wide range supply operation)
    V_{IH} min = 0.7 V_{DD} (wide range supply operation)
- Multi-master system (built-in arbitration for multi-master systems)
- Devices have independent clocks
- Master and slave devices can be receivers and/or transmitters.
- Each device has a unique address.
- Maximum bus clock rate of 100 kHz.

SYSTEM CONFIGURATION

R_p value depends on (1) number of devices on bus, (2) total bus capacitance, (3) supply voltage (Figure 5).

DATA TRANSFER ON THE I²C BUS

If the bus is not being used, both SDA and SCL lines must be left high.

One data bit is transferred on each clock pulse. Data on the SDA line must remain stable during the clock high period, except during START and STOP conditions, which are indicated by the SDA line going high to low (START) or low to high (STOP) during the clock high period.

Every byte put onto the SDA line should be eight bits long (MSB first), followed by an acknowledge bit, which is generated by the receiving device.

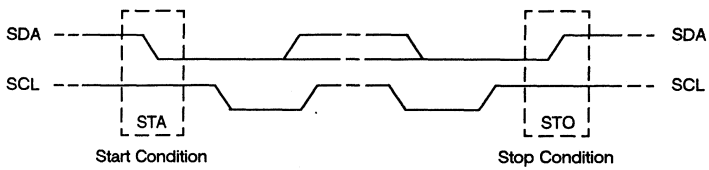

Figure 6. START and STOP Conditions

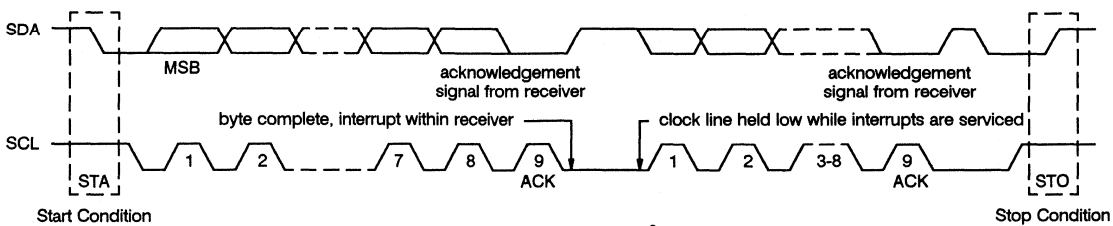

Figure 7. Data Transfer on the I²C Bus

Each data transfer is initiated with a start condition and ended with a stop condition. The first byte after a start condition is always the address byte. If this is the device's own address, the device will generate an acknowledge by pulling the SDA line low during the ninth clock pulse, then accept the data in subsequent bytes until another start or stop condition is detected.

Data bytes are always acknowledged during the ninth clock pulse by the addressed device. Note that during the acknowledge period the transmitting device must leave the SDA line high.

The eight bit of the address byte is the read/write bit (high = read from addressed device, low = write to the addressed device) so, for the DG894, the address is only considered valid if the R/W bit is low.

Premature termination of the data transfer is allowed by generating a stop condition at any time. When this happens, the DG894 will remain in the state defined by the last complete data byte transmitted.

TIMING SPECIFICATIONS OF THE I²C BUS

I²C bus load conditions for timing specifications are as follows:

4 kΩ pull-up resistors to +5 V; 200 pF capacitor to ground. All values are referred to V_{IH} = 3 V, V_{IL} = 1.5 V.

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL Clock Frequency	f_{scl}	-	100	kHz
Bus Free Before Start	t_{BUF}	4.7	-	µs
Start Condition Set-up Time	$t_{SU;STA}$	4.7	-	µs
Start Condition Hold Time	$t_{HD;STA}$	4.0	-	µs
SCL and SDA Low Period	t_{LOW}	4.7	-	µs
SCl and SDA High Period	t_{HIGH}	4.0	-	µs
SCL and SDA Rise Time	t_r	-	1.0	µs
SCl and SDA Fall Time	t_f	-	0.3	µs
Data Set-up Time (WRITE)	$t_{SU;DAT}$	0.25	-	µs
Data Hold Time (WRITE)	$t_{HD;DAT}$	0*	-	µs

*A transmitter must internally provide at lease a hold time to bridge the undefined region (max 300 ns) of the falling edge of the SCL.

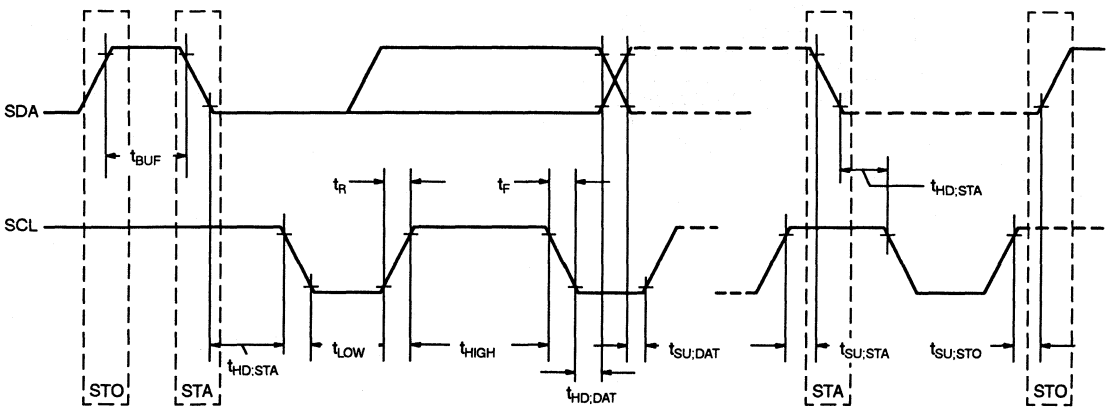

Figure 8. I²C Bus Timing Diagram

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I²C BUS PROTOCOL

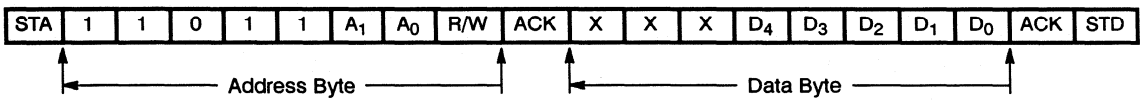
The DG894 is a slave receiver type of I²C interface and has four allocated addresses, two of which are user programmable through the SEL pin. Additional addresses may be obtained by a metal mask option for users requiring more than two DG894s on the same I²C bus. Contact Siliconix marketing for further information.

POWER ON RESET

A power on reset function is provided on the DG894 to turn all switches off following power up if the I²C mode is selected. In the dc mode, the switches are selected according to the state of the control inputs.

After the correct address has been sent, only one data byte is needed to define the switch configuration. Subsequent data put onto the bus will update the switches until a STOP condition (or another START condition) signals that the device is no longer being addressed. The switches will then remain in their last configuration as long as power is maintained to the chip.

MINIMUM BIT STREAM TO SET UP DG894 SWITCHES



STA = START CONDITION
A_1 = 0 (programmable to "1" with metal mask change)
A_0 = $\overline{SEL}$. Address bit set by use (address is inverse of SEL logic level)
R/W = READ/WRITE bit (must be "0"; only WRITE mode allowed for DG894)
ACK = Acknowledge bit ("0") generated by DG894
D_4 = 0 -- R_2, G_2, B_2, and FB_2 switches OFF
D_4 = 1 -- R_2, G_2, B_2, and FB_2 switches ON
D_3 = 0 -- R_1, G_1, B_1, and FB_1 switches OFF
D_3 = 1 -- R_1, G_1, B_1, and FB_1 switches ON
D_2 = 0 -- Y_2, C_2, switches OFF
D_2 = 1 -- Y_2, C_2, switches ON
D_1 = 0 -- Y_1, C_1, switches OFF
D_1 = 1 -- Y_1, C_1, switches ON
D_0 = 0 -- Y and C switches OFF
D_0 = 1 -- Y and C switches ON
STO = STOP CONDITION

PIN DESCRIPTION

SYMBOL	DESCRIPTION
Y, Y_1, Y_2	An analog channel input, typically luminance.
C, C_1, C_2	An analog channel input, typically chrominance.
$R_1, R_2, G_1, G_2, B_1, B_2, FB_1, FB_2$	An analog channel input, typically "red", "green", "blue" or "fast blanking", as appropriate.
GND	Analog and digital ground.
V_{DD}	Positive supply voltage (see note 1)
V_{SS}	Negative supply voltage
Y/C_{OUT}	An analog channel output, typically luminance or chrominance, as appropriate
$R/G/B/FB_{OUT}$	An analog channel output, typically "red", "green", "blue" or "fast blanking", as appropriate.
SMO	Serial mode (I^2C) operation select.
SDA	Serial data line (see note 2).
SCL	Serial clock line (see note 2).
SEL	Dc control line or I^2C address (see note 3)

NOTES:

1. Both V_{DD} pins (pin 1 and pin 26) must be connected for proper operation.
2. SDA and SCL pins become d.c. control inputs when not in I^2C mode.
3. The SEL pin, in I^2C bus operation (i.e., with SMO low), is the least significant bit of the device address. This allows two devices to operate on the same I^2C bus, yet retains independent control.

6

Si581
Wideband Unity-Gain Closed-Loop Buffer

Siliconix incorporated

FEATURES

- 450 MHz –3 dB Bandwidth
- Low Power (P_d = 150 mW)
- Fast Settling (0.2% in 5 ns)
- Low Distortion (–65 dBc at 20 MHz)
- Low Differential Gain (0.1%)
- Low Differential Phase (0.01°)

BENEFITS

- Flat Frequency Response
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transparency
- High Color Fidelity
- Improved Transmission Accuracy

APPLICATIONS

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Transmission Systems

DESCRIPTION

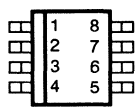
The Si581 is a monolithic closed-loop unity-gain buffer with a very wide –3 dB bandwidth (450 MHz). Its unique design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si581 features wide bandwidth, low power dissipation (typically 150 mW), fast settling (0.2% in 5 ns), without signal degradation. Distortion is typically –65 dBc at 20 MHz, gain flatness is less than 0.4 dB from dc to 50 MHz. These performance specifications allow the designer to improve system bandwidth while reducing system power dissipation, board space and design complexity.

The Si581 uses a complementary bipolar IC process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5 V supplies, reducing power consumption compared with traditional ±15 V designs. It is available in space-saving PDIP-8 (J-suffix) and SO-8 (Y-suffix) packages for operation over the industrial (–40 to 85°C) range.

PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM

SO Package
(Same pinout as DIP)

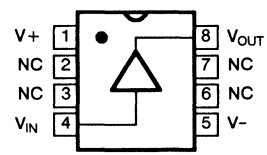


Top View

Order Number:

Si581DY

Dual-In-Line Package



Top View

Order Number:

Plastic: Si581DJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±7 V
Input Voltage Range ..... V– to V+
Output Short Circuit Duration ..... Continuous
I_O (Output is short circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.)

Storage Temperature ..... –65 to 150°C
Operating Temperature ..... –40 to 85°C
Lead Temperature (Soldering 10s) ..... 300°C
Junction Temperature: T_J ..... 175°C
Thermal Resistance: θ_{JA} ..... 175°C/W

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V− = −5 V R_L = 100 Ω, R_S = 50 Ω		TEMP[i]	D SUFFIX −40 to 85 °C TYP[d]	MIN[b]	MAX[b]	UNIT
FREQUENCY DOMAIN[h]								
−3 dB Bandwidth[c]	MSBW	V_{OUT} = <1 V_{p-p}		Room Full	450	275 250		MHz
	LSBW	V_{OUT} = 5 V_{p-p}		Room Full	90	55 60		
Gain Flatness Peaking[e, g]	GFPH	V_{OUT} <1.0 V_{p-p} dc to 50 MHz		Room Full	0		0.4 0.5	dB
Gain Flatness Roll Off[e]	GFRH			Room Full	0		0.5 0.6	
Linear Phase Deviation[e]	LPD	dc to 50 MHz		Room Full	0.5		1.0 1.5	
Differential Phase	DP	R_L = 150 Ω	f = 3.58 MHz	Room	0.01			deg
		$V_{Carrier}$ = 280 mV	f = 4.43 MHz	Room	0.01			
Differential Gain	DG	f = 4.43 MHz	R_L = 150 Ω	Room	0.1			%
		$V_{Carrier}$ = 280 mV	R_L = 1 kΩ	Room	0.07			
TIME DOMAIN[h]								
Rise and Fall Time[c]	t_{RS}	V_{IN} = 0.5 V Step Input Rise/Fall time = 300 ps		Room Full	0.4		1.0 1.4	ns
	t_{RL}	V_{IN} = 5 V Step Input Rise/Fall time ≤ 300 ps		Room Full	4.5		7.5 8.5	
Settling Time[c]	t_{SP}	To ±0.2 %, V_{IN} = 2 V Step		Full	5		10	
Slew Rate[c]	SR			Room Full	800	500 450		V/µs
DISTORTION AND NOISE								
2nd Harmonic Distortion[g]	HD_2	V_{IN} = 2 V_{p-p} f_{IN} = 20 MHz		Room Full	−65		−55 −48	dBc
3rd Harmonic Distortion[g]	HD_3			Full	−65		−55	
Equivalent Input Noise Floor[c]	SNF	f >100 kHz		Room Full	−158		−155 −154	dBm (1 Hz)
Equivalent Input Integrated Noise[c]	INV	100 kHz < f <200 MHz		Room Full	40		57 63	µV
STATIC, dc								
Small Signal Gain[c]	GA			Room Full	0.97	0.96 0.95		V/V
Integral Non-Linearity[c]	INL	±2 V Full Scale		Room Hot Cold	0.2		0.4 0.3 0.8	%FS
Output Offset Voltage[f]	V_{OS}			Room Hot Cold	2		8 13 16	mV
Output Offset Voltage Temperature Coefficient[c]	TCV_{OS}	Average		Room Hot Cold	20		– 50 100	µV/°C

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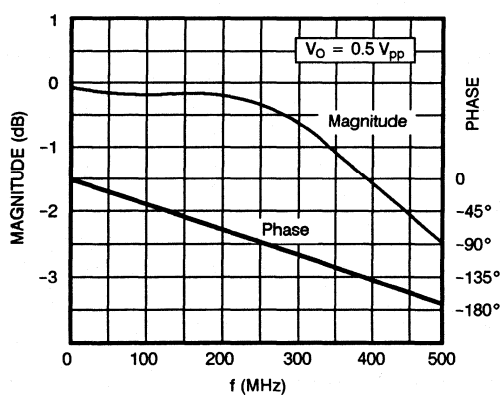
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = -5 V R_L = 100 Ω, R_S = 50 Ω		D SUFFIX -40 to 85 °C			UNIT
			TEMP[i]	TYP[d]	MIN[b]	MAX[b]	
STATIC, dc							
Input Bias Current[f]	I_B		Room Full	20		50 100	µA
Input Bias Current Temperature Coefficient[c]	TCI_B	Average	Room Hot Cold	200		- 300 700	nA/°C
Power Supply Rejection Ratio[g]	PSRR		Full	50	40		dB
Supply Current[f]	I+	No Load	Full	15		20	mA
MISCELLANEOUS							
Input Resistance[c]	R_{IN}		Room Hot Cold	160	100 200 50		kΩ
Input Capacitance[c]	C_{IN}		Room Full	1.6		2.2 2.5	pF
Output Impedance[c]	R_O	At dc	Room Full	2		3 3.5	Ω
Output Voltage Range[c]	V_O		Room Full	±4	-3.2 -3	3.2 3	V
Output Current[c]	I_O		Room Full	±70	-50 -45	50 45	mA

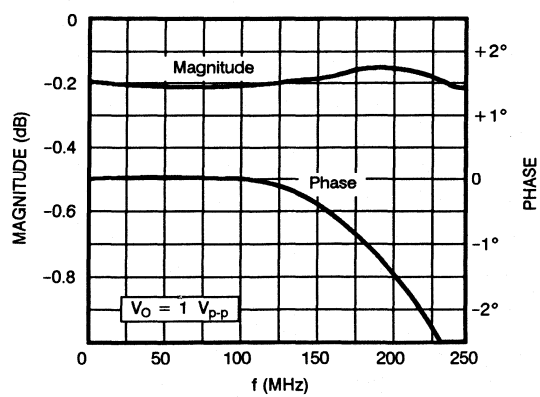
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, and reflect room temperature performance. They are nto guaranteed nor subject to production testing.
e. Gain flatness tests are performed from 0.1 MHz to 50 MHz, and specifications are guaranteed from dc to 50 MHz.
f. Parameter is 100% tested at 25°C and sample tested at -40 and 85°C.
g. Parameter is sample tested at 25°C.
h. Ac performance is very dependent on layout. Specifications apply only in a 50 Ω microstrip environment.
i. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.

TYPICAL CHARACTERISTICS (V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω)

Forward Gain and Phase

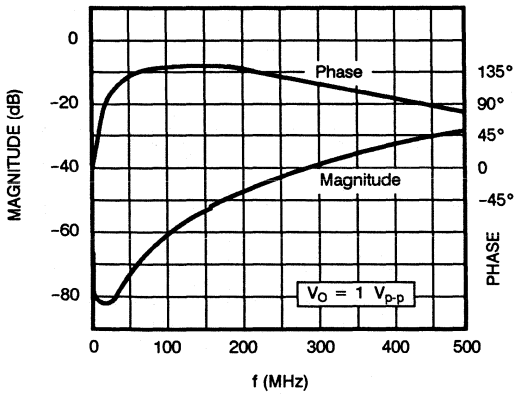


Gain Flatness and Deviation from Linear Phase

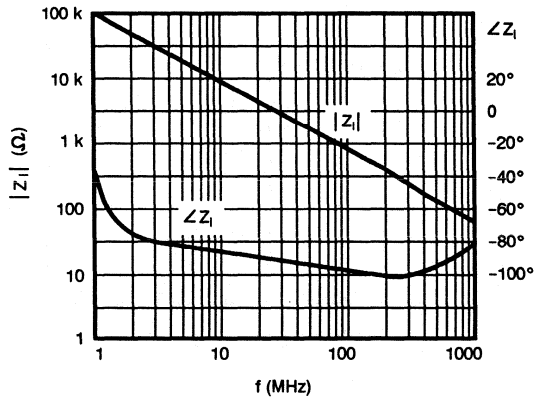


TYPICAL CHARACTERISTICS (V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω)

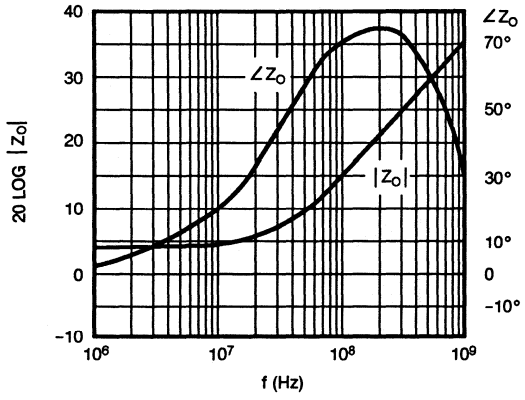
Reverse Gain and Phase



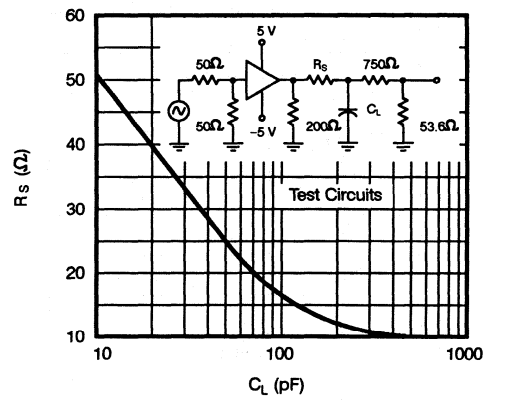
Input Impedance



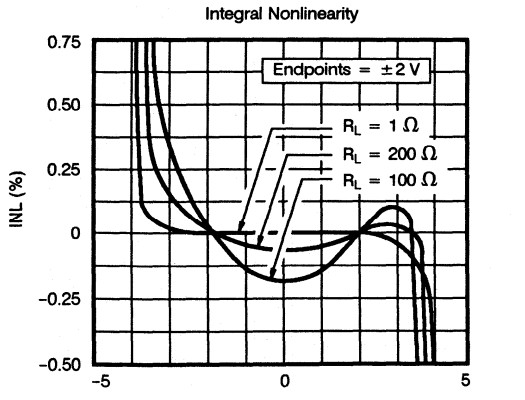
Output Impedance



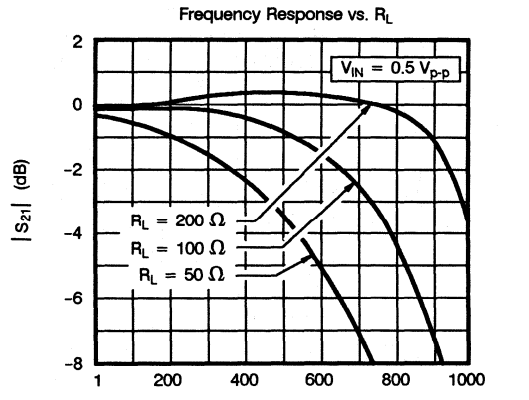
Recommended R_S vs. Load Capacitance



Integral Nonlinearity



Frequency Response vs. R_L



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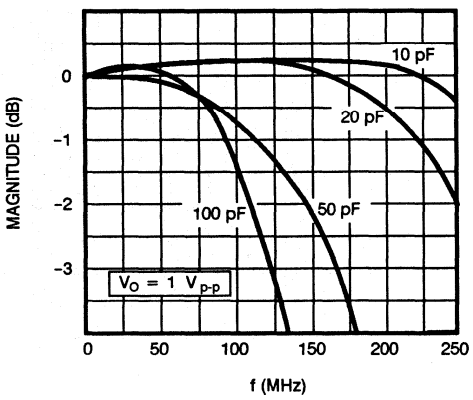
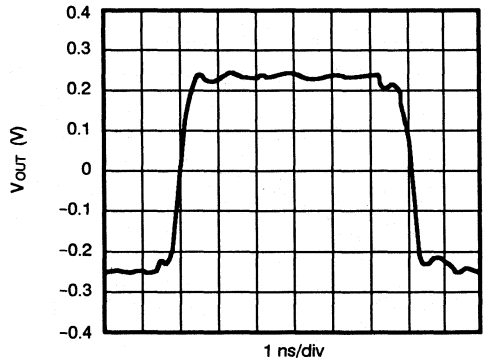
TYPICAL CHARACTERISTICS (V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω)

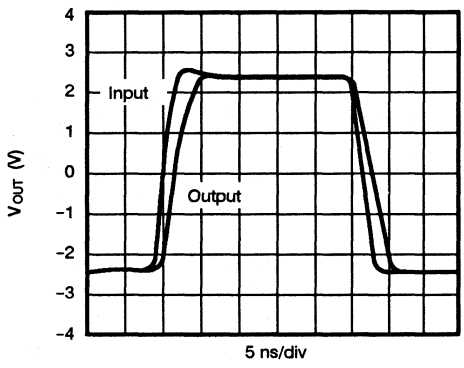
Forward Gain vs. C_{LOAD} With Recommended R_S



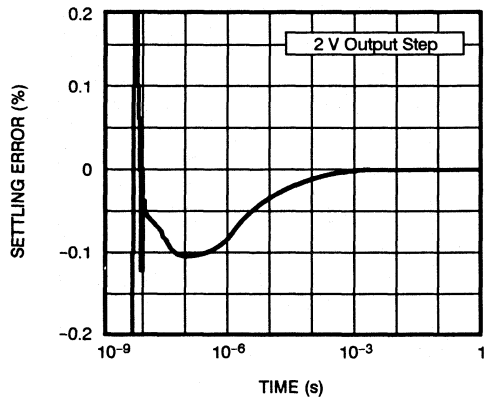
Small Signal Pulse Response



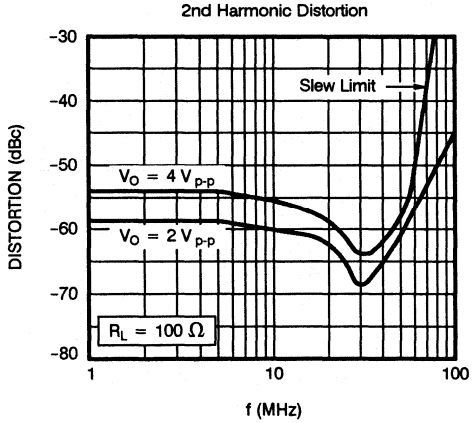
Large Signal Pulse Response



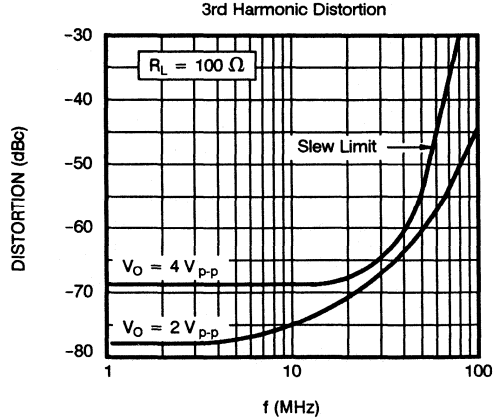
Long-Term Settling Time



2nd Harmonic Distortion

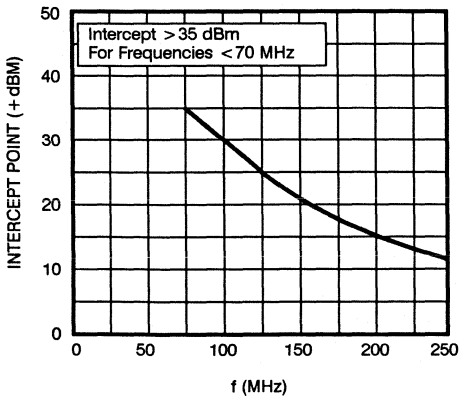


3rd Harmonic Distortion

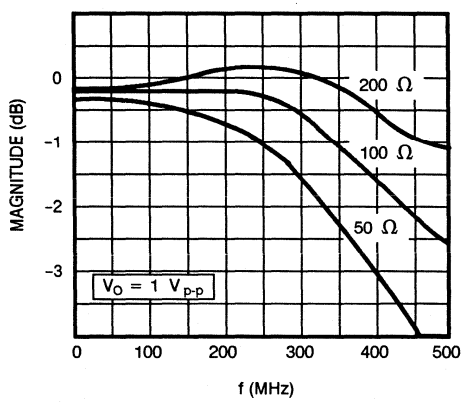


TYPICAL CHARACTERISTICS (V_{SUP} = ±5 V, R_L = 100 Ω, R_S = 50 Ω)

2-Tone, 3rd Order Intermodulation Intercept



Forward Gain vs. R_L



APPLICATIONS

Operation

The Si581 is based upon a unique, patented closed-loop design, which provides the accuracy characteristics of a closed-loop amplifier, yet also has unmatched dynamic performance.

Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the Si581 which has a typical bandwidth of 450 MHz.

To minimize capacitive feedthrough, the pins which are not connected internally (pins 2, 3, 6, and 7) should be connected to the ground plane. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the Si581. On a 0.065 inch epoxy PCB material, a 50 Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing. The ferrite beads are optional and are recommended only where additional isolation from high-frequency (>400 MHz) resonances of the power supply is needed.

Parasitic or load capacitance directly on the output of the Si581 will introduce additional phase shift in the device, which can lead to decreased phase margin and frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The typical characteristic curves illustrate the required resistor value and the resulting performance vs. capacitance.

Precision buffed resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they will cause a degradation of ac performance due to their reactive nature at high frequencies.

Evaluation Board

An evaluation board is available to assist in the evaluation of the Si581. It may also be used as a guide in developing a printed circuit layout. Figure 1 shows the board's schematic; Figures 2 through 4 show the board layout.

Evaluation Board Parts List:

R_{in}	select for desired input impedance
R_{out}	select for desired output impedance
C_1, C_2	0.1 µF ceramic radial lead
C_3, C_4	6.8 µF
L_1, L_2	ferrite beads (optional) (Ferroxcube #VK200 19/4B)

Hardware (optional):

Sockets: Cambion flush-mount connector jacks (#450-2598-01-06-00)

SMA Connectors (female):

Amphenol 901-144 (straight)

Amphenol 901-143 (angled)

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APPLICATIONS (Cont'd)

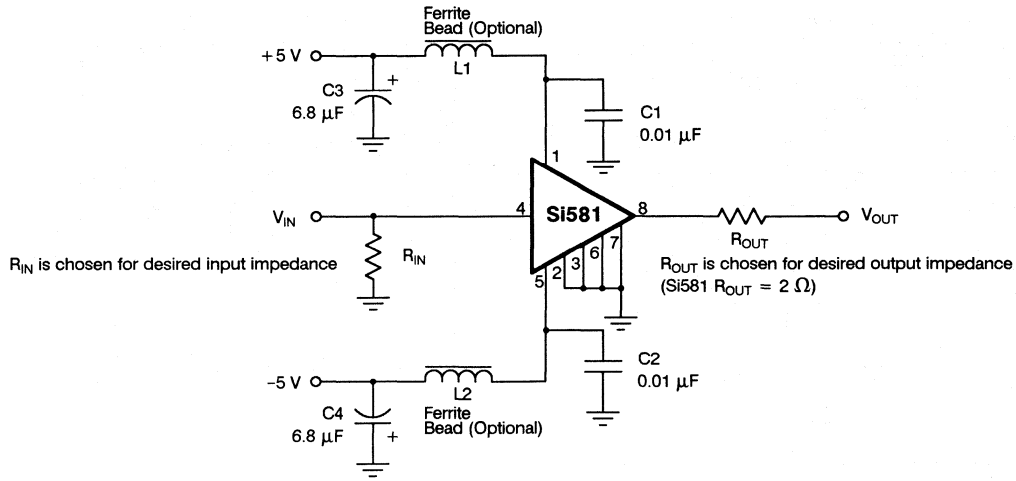


Figure 1. Recommended Circuit and Evaluation Board Schematic

Layouts Not to Scale

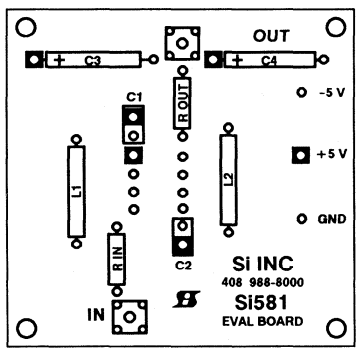


Figure 2. Component Placement Guide

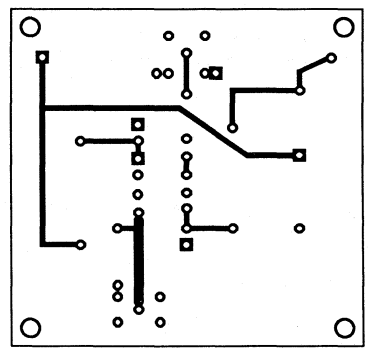


Figure 3. Solder Side (Bottom) as Viewed From Component Side (Top)

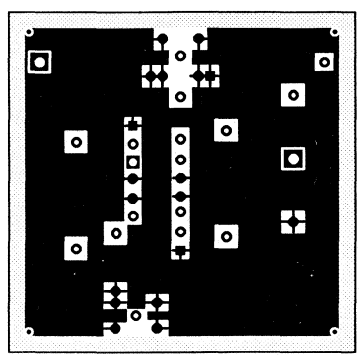


Figure 4. Component Side (Top) Showing Extensive Ground Plane

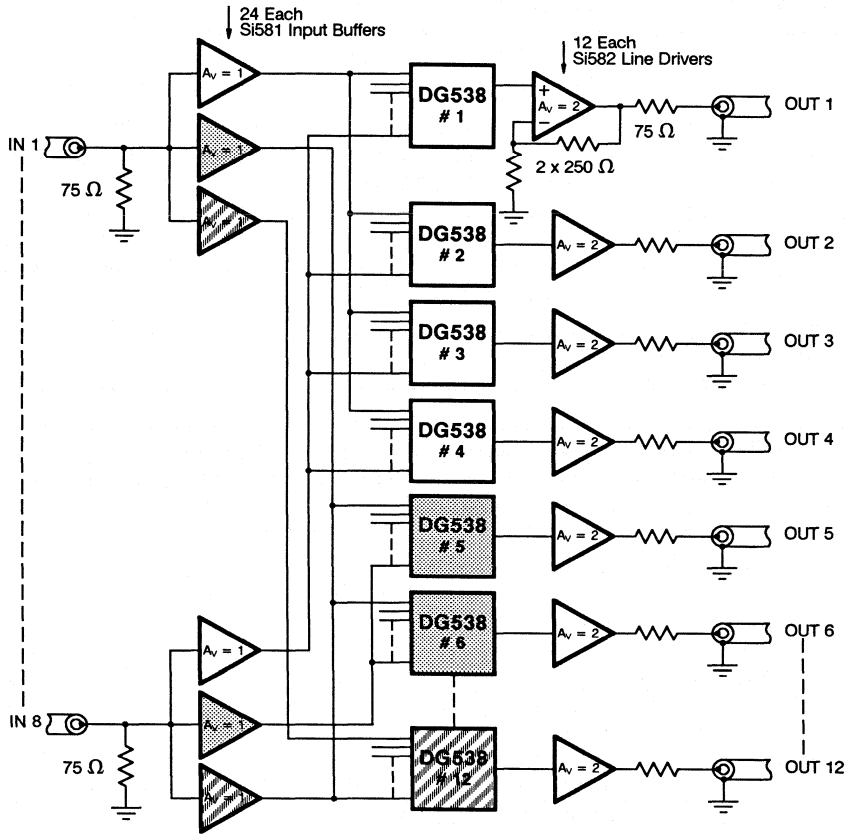


Figure 5. Buffering in a 50 MHz 8 x 12 Video Crosspoint Switch

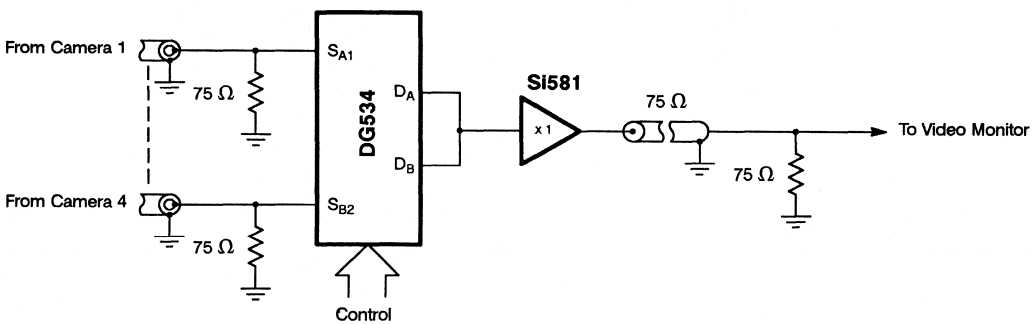


Figure 6. Four Camera High-Definition Closed Circuit TV System

Si582
Monolithic Wideband Low-Gain Amplifier

Siliconix incorporated

FEATURES

- 180 MHz –3 dB Bandwidth
- ±1 to ±8 Closed-Loop Gain Range
- Low Power (P_d = 150 mW)
- Fast Settling (0.05% in 12 ns)
- Low Distortion (–60 dBc at 20 MHz)
- $\overline{\text{DISABLE}}$ Function
- Low Differential Gain (0.1%)
- Low Differential Phase (0.01°)

BENEFITS

- Flat Frequency Response
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- High Color Fidelity
- Improved Transmission Accuracy
- Automatic Power-Down

APPLICATIONS

- Co-Ax Cable Drivers
- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Transmission Systems

DESCRIPTION

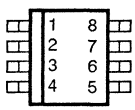
The Si582 is a monolithic low gain operational amplifier with a –3 dB bandwidth of 180 MHz. Its unique current mode feedback design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and other video amplifiers.

The Si582 features wide bandwidth, low power dissipation (typically 150 mW) and fast settling (0.05% in 12 ns). Distortion is typically –60 dBc at 20 MHz, gain flatness is less than 0.4 dB from dc to 50 MHz. These performance specifications allow the designer to improve system bandwidth while reducing power dissipation, board space and design complexity. The wide bandwidth combined with 50 mA output current at a gain of 2 provides an excellent high performance solution for video distribution and line driving applications. In addition, digital transmission systems will benefit from its superior pulse response.

The Si582 uses a complementary bipolar IC process to achieve excellent high frequency performance. All parameters are specified and rated for operation with ±5 V supplies, reducing power consumption compared with traditional ±15 V designs. It is available in space-saving PDIP-8 and SO-8 packages for operation over the industrial, D suffix (–40 to 85°C) range. A military version in the 8-pin side braze package is planned.

PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM

SO Package
(Same pinout as DIP)

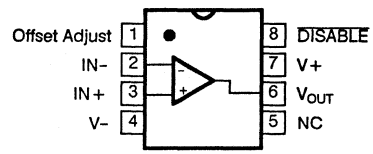


Top View

Order Number:

Si582DY

Dual-In-Line Package



Top View

Order Number:

Plastic: Si582DJ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±7 V
Input Voltage Range ..... V– to V+
Output Short Circuit Duration ..... Continuous
I_O (Output is short circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.)
Common Mode Input Voltage ..... V– to V+
Differential Input Voltage ..... 10 V
Storage Temperature ..... –65 to 150°C
Operating Temperature ..... –40 to 85°C
Lead Temperature (Soldering 10s) ..... 300°C
Junction Temperature: T_J ..... 175°C
Thermal Resistance: θ_{JA} ..... 175°C/W

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = -5 V R_L = 100 Ω, R_F = 250 Ω, A_V = 2		TEMP[h]	D SUFFIX -40 to 85 °C TYP[d]	MIN[b]	MAX[b]	UNIT
FREQUENCY DOMAIN[g]								
-3 dB Bandwidth[c]	MSBW	V_{OUT} = ≤1 V_{p-p}		Room Full	180	140 110		MHz
	LSBW	V_{OUT} = 5 V_{p-p}, A_V = 5		Full	50	35		
Gain Flatness Peaking[e, g]	GFPH	V_{OUT} ≤1.0 V_{p-p} dc to 50 MHz		Room Full	0		0.4 0.5	dB
Gain Flatness Roll Off[e]	GFRH			Room Full	0.05		1.0 1.3	
Linear Phase Deviation[e]	LPD	dc to 50 MHz		Room Full	0.2		1.0 1.2	
Differential Phase	DP	R_L = 150 Ω $V_{Carrier}$ = 280 mV	f = 3.58 MHz f = 4.43 MHz	Room Room	0.01 0.01			deg
Differential Gain	DG	f = 4.43 MHz $V_{Carrier}$ = 280 mV	R_L = 150 Ω R_L = 1 kΩ	Room Room	0.1 0.07			%
TIME DOMAIN[g]								
Rise and Fall Time[c]	t_{RS}	V_{IN} = 1 V Step		Full	2.4		3.5	ns
	t_{RL}	V_{IN} = 5 V Step		Full	6.5		10	
Settling Time[c]	t_{SP}	To ±0.05 %, V_{IN} = 2 V Step		Full	12		15	
Slew Rate[c]	SR	A_V = 2		Full	700	430		V/µs
	SR_1	A_V = -2		Full	1600			
DISTORTION AND NOISE								
2nd Harmonic Distortion[g]	HD_2	V_{IN} = 2 V_{p-p} f_{IN} = 20 MHz		Room Full	-60		-45 -40	dBc
3rd Harmonic Distortion[g]	HD_3			Full	-60		-50	
Equivalent Input Noise Floor[c]	SNF	f >100 kHz 50 Ω on Input		Room Full	-157		-154 -153	dBm (1 Hz)
Equivalent Input Integrated Noise[c]	INV	100 kHz < f <200 MHz		Room Full	40		57 63	µV
SWITCHING ($\overline{\text{DISABLE}}$)								
Turn On Time	t_{ON}			Full			25	ns
Turn Off Time	t_{OFF}			Full			2	µs
Off Isolation[c]	OI	f_{IN} = 10 MHz, $\overline{\text{DISABLE}}$ = "0"		Full	-59	-55		dB
Current to Disable	I_{DIS}			Full			250	µA
Disable Drive Voltage	V_{DISL}	$\overline{\text{DISABLE}}$ = "0", I_{DIS} = 250 µA		Room Full			0.8 0.5	V
Voltage to Enable	V_{DISH}	$\overline{\text{DISABLE}}$ = "1"		Room Full		2.4 3.0		

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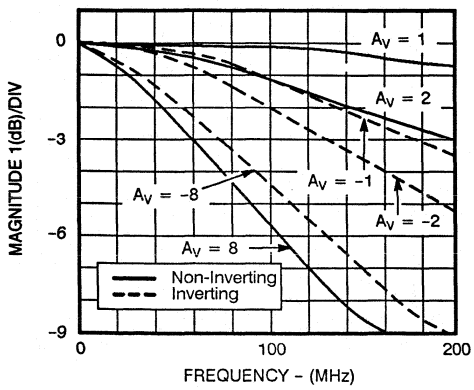
SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = -5 V R_L = 100 Ω, R_F = 250 Ω, A_V = 2			D SUFFIX -40 to 85 °C		UNIT
			TEMP[h]	TYP[d]	MIN[b]	MAX[b]	
STATIC, dc							
Input Offset Voltage[c]	V_{OS}		Room Full	2	-5.5 -9.5	5.5 9.5	mV
Input Offset Voltage Temperature Coefficient[c]	TCV_{OS}		Room Full	20	 -40	 40	µV/°C
Input Bias Current Non-inverting[e]	I_{BN}		Room Full	10	-25 -41	25 41	µA
Input Bias Current Non-inverting Temperature Coefficient[c]	TCI_{BN}		Room Hot Cold	100	 -100 -200	 100 200	nA/°C
Input Bias Current Inverting[e]	I_{BI}		Room Hot Cold	10	-25 -35 -41	25 35 41	µA
Input Bias Current Inverting Temperature Coefficient[c]	TCI_{BI}		Room Hot Cold	50	 -100 -200	 100 200	nA/°C
Power Supply Rejection Ratio[f]	PSRR		Full	50	40		dB
Common Mode Rejection Ratio	CMRR		Full	50	40		
Supply Current[e]	I+	No Load	Full	15		23	mA
		Disabled	Full	4		6	
MISCELLANEOUS							
Non-inverting Input Resistance	R_{IN}		Room Hot Cold	200	100 100 50		kΩ
Non-inverting Input Capacitance	C_{IN}		Full	0.5		2.0	pF
Output Impedance	R_O	At dc	Full	0.1		0.2	Ω
Output Voltage Range	V_O	No Load	Room Full	±3.5	-3.2 -3	3.2 3	V
Common Mode Input Range	CMIR	For Rated Performance	Room Full	±2.1	-2 -1.2	2 1.2	
Output Current[c]	I_O		Room Full	±70	-50 -35	50 35	mA

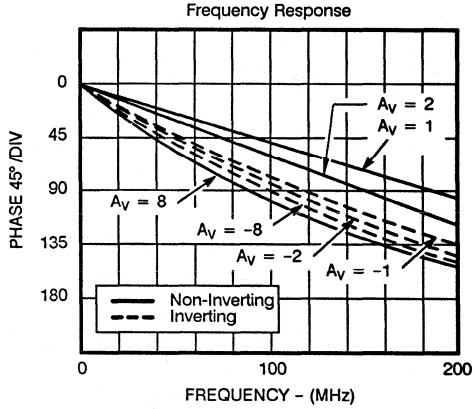
NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, and reflect room temperature performance. They are not guaranteed nor subject to production testing.
e. Parameter is 100% tested at 25°C and sample tested at -40 and 85°C.
f. Parameter is sample tested at 25°C.
g. Ac performance is very dependent on layout. Specifications apply only in a 50 Ω microstrip environment.
h. Room = 25°C, Cold, Hot and Full = as determined by the operating temperature suffix.
j. dBc = dB with respect to carrier.

TYPICAL CHARACTERISTICS (T_A = 25°C, V_{SUP} = ±5 V, R_L = 100 Ω, A_V = +2)

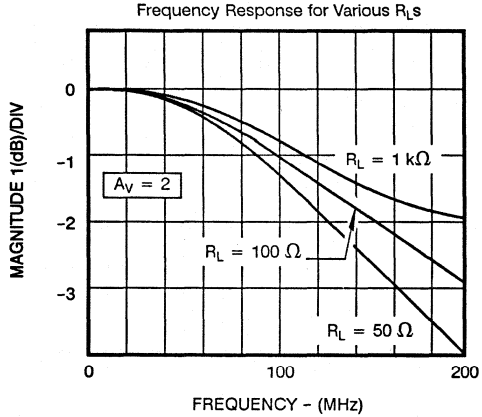
Frequency Response



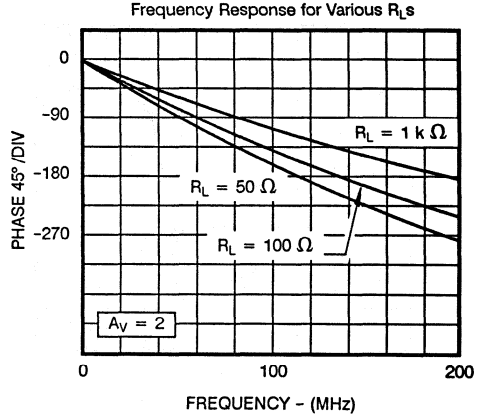
Frequency Response



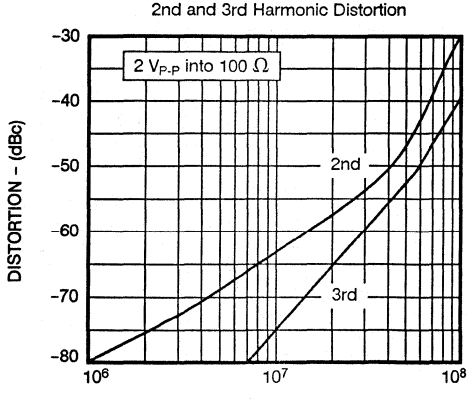
Frequency Response for Various R_Ls



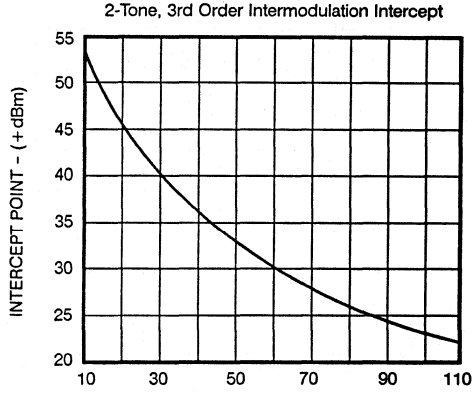
Frequency Response for Various R_Ls



2nd and 3rd Harmonic Distortion



2-Tone, 3rd Order Intermodulation Intercept



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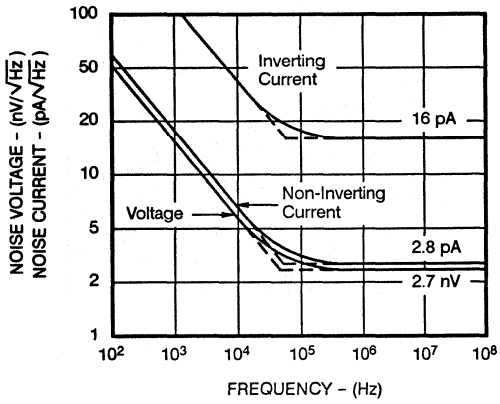
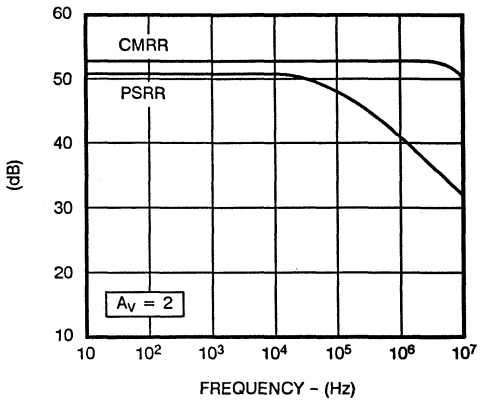
TYPICAL CHARACTERISTICS (T_A = 25°C, V_{SUP} = ±5 V, R_L = 100 Ω, A_V = +2)

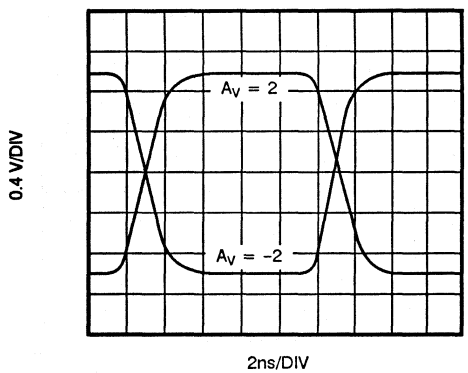
Equivalent Input Noise



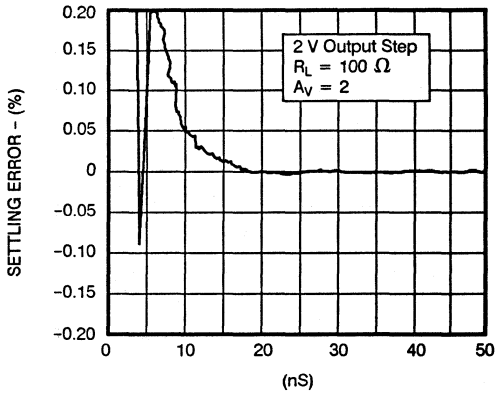
CMRR and PSRR



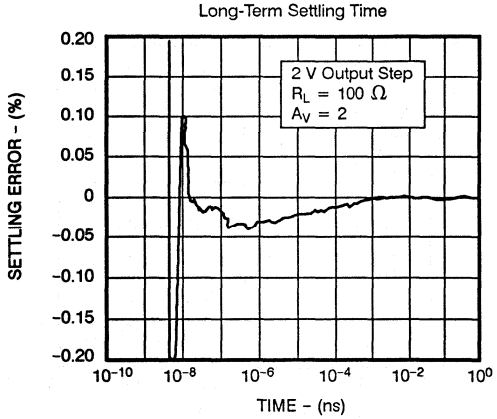
Pulse Response



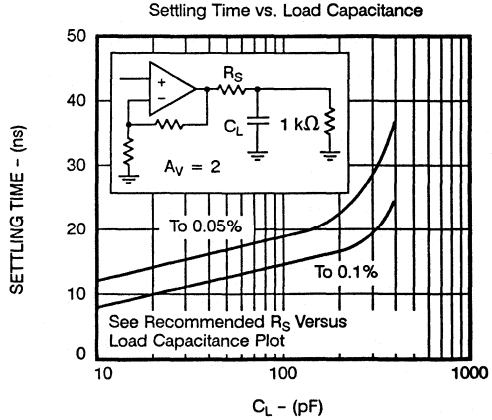
Settling Time



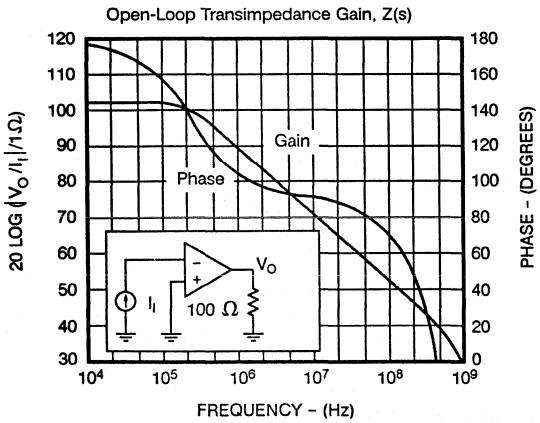
Long-Term Settling Time

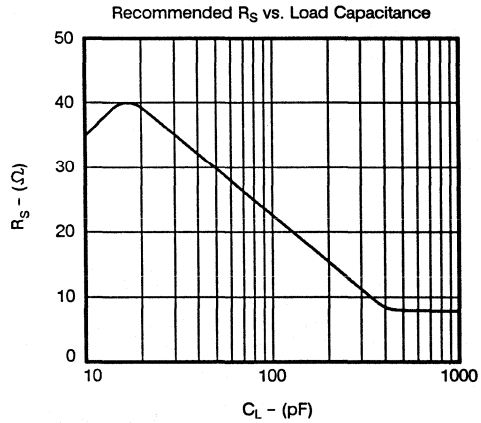


Settling Time vs. Load Capacitance



TYPICAL CHARACTERISTICS (T_A = 25°C, V_{SUP} = ±5 V, R_L = 100 Ω, A_V = +2)





APPLICATIONS

SETTING LOOP GAIN

The Si582 uses a current feedback topology instead of the more common voltage feedback, meaning that the closed loop bandwidth and settling time are relatively independent of closed loop gain.

Optimum bandwidth is achieved with a feedback resistor of 220 to 270 Ω. Closed loop gain is then set by a suitable choice of input resistor value. Figure 1 shows the connections for inverting and non-inverting gains. Feedback resistors greater than 270 Ω may be used, but at the expense of bandwidth. Values lower than 220 Ω will cause amplitude peaking in the passband. For example, a feedback resistor value of 100 Ω will create a peak of approximately 4 dB as roll-off is approached.

Under no circumstances should the output be connected directly to the inverting input in the hope of achieving unity gain. This will cause the device to oscillate and draw significant current from the power supply. Unity gain may be achieved with a 220 to 270 Ω resistor in the feedback path with no input resistor. Similarly, capacitive feedback should not be used with the Si582.

OFFSET CORRECTION

Since the two inputs to the Si582 are quite different internally, the noise and offset performance differs from that of a differential input op-amp. The two input bias currents are unrelated, so that the technique of bias current error cancellation by matching of the inverting and non-inverting input resistances is ineffective.

The equation for output offset is shown in Figure 1, and is the algebraic sum of the equivalent input voltage and current sources which influence dc operation. Pin 1 may be used to correct for the ± 10 mV offset by connecting as shown in Figure 1. When not used, pin 1 should be bypassed to signal ground with a 0.1 µF low inductance capacitor.

DISABLE OPERATION

The disable function of the Si582 is obtained by taking pin 8 to ground. A maximum current of 250 µA and a maximum voltage of 0.5 Volts is required for full disable. When the disable function is not required, pin 8 may be left open or could be tied to the +5 V rail.

PCB LAYOUT AND SUPPLY BYPASSING

The Si582 bandwidth and pulse response are dependent upon good layout and decoupling techniques. Ground plane construction is recommended to preserve as low a ground impedance as possible. Power supply decoupling components should be mounted close to the package and should have good high frequency characteristics to preserve the excellent pulse performance of the device. Figure 2 shows the recommended decoupling circuit. The 10 µF capacitor should be Tantalum or other low ESR/ESL type. For the 0.1 µF capacitor, multi-layer ceramic capacitors are recommended. A low value resistor in series with the 10 µF capacitor's ground lead may be required to reduce output pulse ringing.

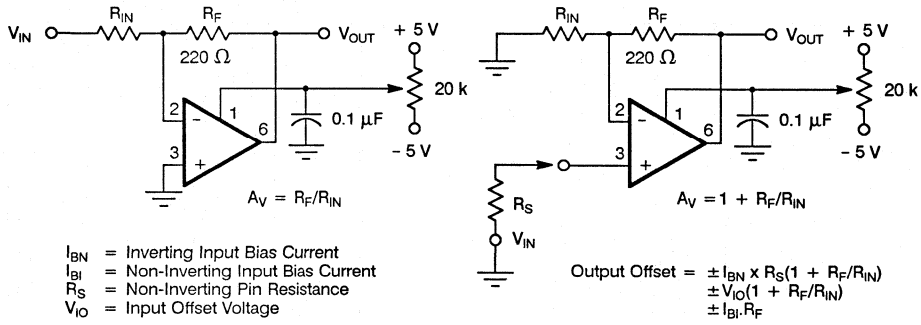


Figure 1. Si582 Inverting and Non-Inverting Gain Circuit

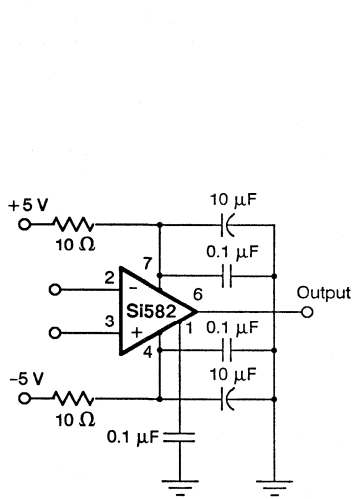


Figure 2. Decoupling the Si582

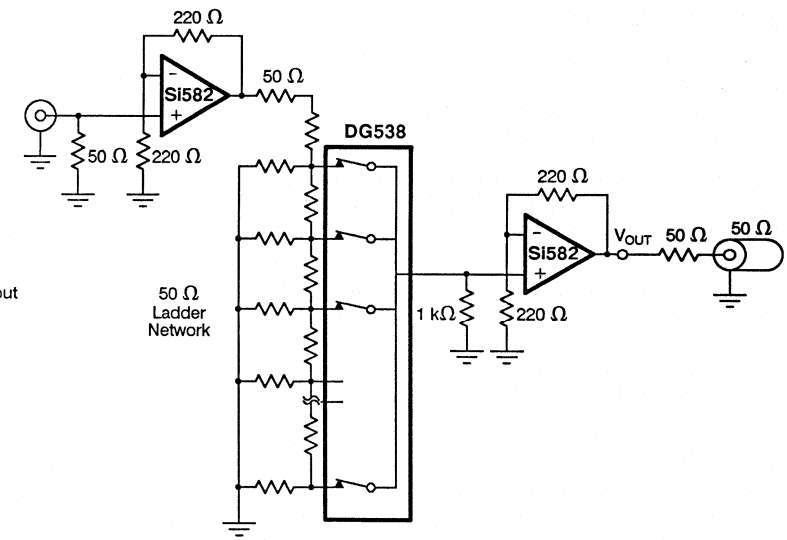


Figure 3. 8-Step Wideband Digitally Controlled Attenuator

DIGITALLY CONTROLLED ATTENUATOR

Figure 3 shows the Si582 in a wideband, digitally controlled attenuator circuit employing the DG538, an 8 to 1 D/CMOS multiplexer. The first Si582 buffers the input and provides a 50 Ω source to drive the 50 Ω ladder attenuator. Taps are chosen to suit the application, i.e., 0.1 dB or 1 dB steps. The second Si582 buffers the multiplexer for good linearity and, at a gain of two, provides "lossless" cable termination at the output.

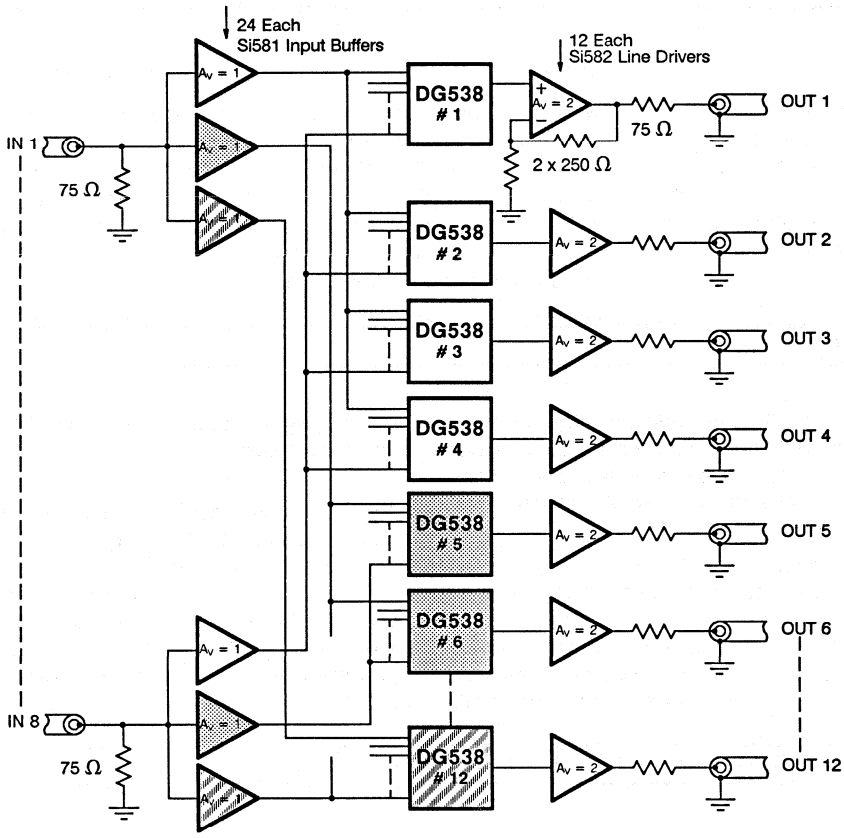


Figure 4. 50 MHz 8 x 12 Video Crosspoint Switch

Si584
Quad Wideband Unity-Gain Closed-Loop Buffer

Siliconix incorporated

FEATURES

- 200 MHz –3 dB Bandwidth
- Low Power (P_d = 120 mW)
- Fast Settling (0.1% in 25 ns)
- Low Distortion (–57 dBc at 20 MHz)
- Low Differential Gain (0.001%)
- Low Differential Phase (0.01°)

BENEFITS

- Flat Frequency Response
- Reduces Power Consumption
- Increases Data Throughput
- Improved Linearity
- Improved Transparency
- High Color Fidelity
- Improved Transmission Accuracy

APPLICATIONS

- Video Signal Routing
- Telecommunications
- Digital Video
- Broadcast Quality Video Systems
- HDTV Transmission Systems

DESCRIPTION

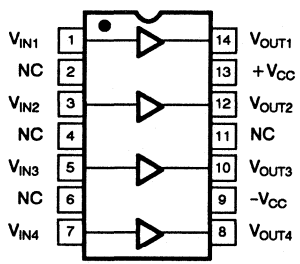
The Si584 is a monolithic closed-loop unity-gain buffer with a very wide –3 dB bandwidth (200 MHz). Its unique design offers a high-transparency, high-performance alternative to conventional discrete, hybrid and open-loop buffers.

The Si584 features wide bandwidth, low power dissipation (typically 120 mW), fast settling (0.1% in 25 ns), without signal degradation. Distortion is typically –57 dBc at 20 MHz, gain flatness is less than 0.35 dB from dc to 30 MHz. These performance specifications allow the designer to improve system bandwidth while reducing system power dissipation, board space and design complexity.

The Si584 uses a complementary bipolar IC process to achieve excellent high frequency performance. All performance is specified and rated for operation with ±5 V supplies, reducing power consumption compared with traditional ±15 V designs. It is available in space-saving PDIP-14 (J-suffix) and SO-14 (Y-suffix) packages for operation over the industrial (–40 to 85°C) range.

PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM

Dual-In-Line Package

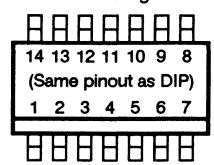


Top View

Order Number:

Plastic: Si584DJ

SO Package



Top View

Order Number:

Si584DY

Advance Information

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, V- = -5 V R_L = 100 Ω, R_S = 50 Ω		TEMP[h]	TYP[d]	D SUFFIX -40 to 85 °C MIN[b]	D SUFFIX -40 to 85 °C MAX[b]	UNIT
FREQUENCY DOMAIN[g]								
-3 dB Bandwidth[c]	MSBW	V_{OUT} = ≤1 V_{p-p}		Room	200	130		MHz
	LSBW	V_{OUT} = 5 V_{p-p}		Full	23			
Gain Flatness Peaking[e, g]	GFPH	V_{OUT} ≤1.0 V_{p-p}, dc to 30 MHz		Room	0.35		0.6	dB
Differential Phase	DP	R_L = 2.5 kΩ $V_{Carrier}$ = 280 mV	f = 3.58 MHz	Room	0.01			deg
			f = 4.43 MHz	Room	0.01			
Differential Gain	DG		f = 3.58 MHz	Room	0.002			%
			f = 4.43 MHz	Room	0.001			
TIME DOMAIN[g]								
Rise and Fall Time[c]	t_{RL}	V_{IN} = 2 V Step		Room	4		7	ns
Overshoot[c]				Room	2.5		13	%
Settling Time[c]	t_{SP}	To ±0.05 %, V_{IN} = 2 V Step		Room	25		42	ns
Slew Rate[c]	SR	V_{IN} = 2 V Step		Room	700	200		V/µs
DISTORTION AND NOISE								
2nd Harmonic Distortion[g]	HD_2	V_{IN} = 2 V_{p-p}		Room	-57			dBc[k]
3rd Harmonic Distortion[g]	HD_3	f_{IN} = 20 MHz		Room	-48			
Equivalent Input Noise Floor[c]	SNF	f >100 kHz 50 Ω on Input		Room Full	-157		-156 -154	dBm (1 Hz)
STATIC, dc								
Small Signal Gain	G_A			Room	0.99			V/V
Integral Endpoint Linearity	I_{LIN}			Room	0.15			%FS
Output Offset Voltage	V_{OS}			Room Full	2.5		4 7	mV
Input Bias Current	I_B			Room Full	2		2.2 3.2	µA
Power Supply Rejection Ratio[f]	PSRR			Full	57	55		dB
Supply Current, per Buffer[e]	I+	No Load		Full	3		4	mA
MISCELLANEOUS								
Input Resistance	R_{IN}			Room	4400			kΩ
Input Capacitance	C_{IN}			Room	0.22			pF
Output Impedance	R_O	At dc		Full	2.2			Ω
Output Voltage Range	V_O			Room	±2			V
Output Current, per Buffer[c]	I_O			Room Full	±20	14 8		mA

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SPECIFICATIONS[a]

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, and reflect room temperature performance. They are not guaranteed nor subject to production testing.
e. Parameter is 100% tested at 25°C and sample tested at -40 and 85°C.
f. Parameter is sample tested at 25°C.
g. Ac performance is very dependent on layout. Specifications apply only in a 50 Ω microstrip environment.
h. Room = 25°C, Full = as determined by the operating temperature suffix.
k. dBc = dB with respect to carrier.

APPLICATIONS

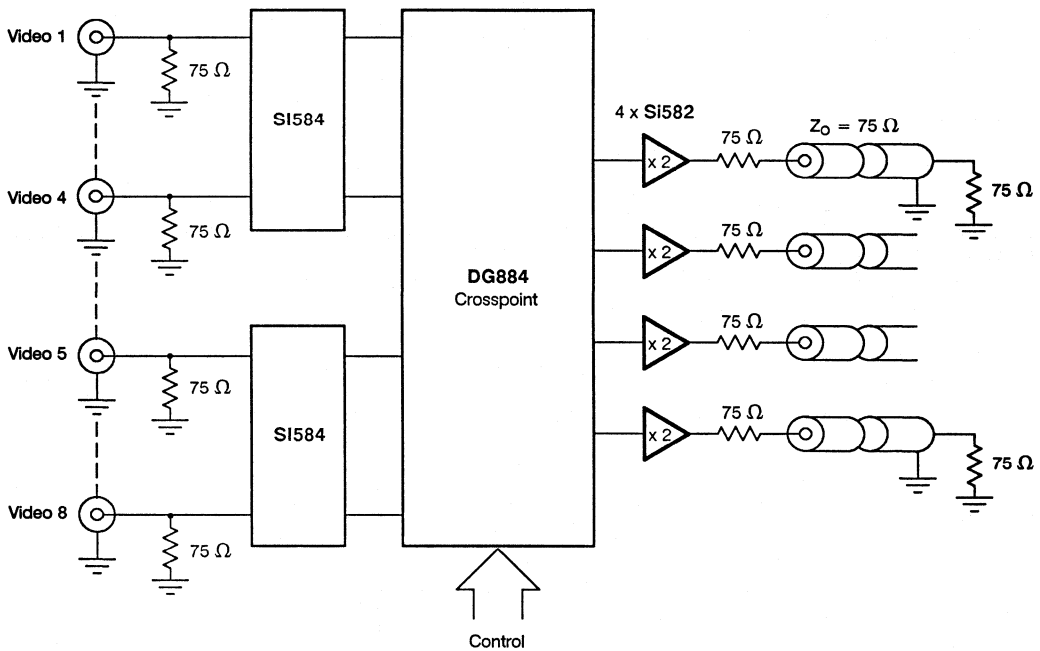


Figure 1. Minimum Parts Count 50 MHz 8 x 4 Video Switching Matrix

TABLE OF CONTENTS

POWER CONVERSION

INTRODUCTION

Virtually every piece of electronic equipment in the world requires a dc power supply. This supply converts power from a battery or an ac line (or sometimes both) into voltages and currents which are useful to the specific piece of electronic equipment it serves. Usually, the outputs must remain constant despite changes in input voltage, output load, and ambient temperature. In addition, the supply should have high conversion efficiency; inject a minimum of noise, ripple or distortion onto its input or output, be small in volume, light in weight, and low in cost.

Siliconix power conversion circuits bring effective solutions to the problems of supplying power to electronic systems, while meeting the above criteria. Siliconix presently supplies three types of power conversion circuits: charge pump voltage converters, high-voltage switchmode regulators and high-voltage switchmode controllers.

Our family of low-cost CMOS charge pump voltage converters are used in applications where a single dc supply is available. These monolithic products feature high conversion efficiency, minimum noise and distortion, and minimum space requirements. They can be configured for voltage inversion or voltage doubling, and require only a few external components (typically two electrolytic capacitors). A typical application would be negative rail generation in a circuit with a battery supply.

The Si7660 is a charge pump converter that inverts or boosts input voltages from the 1.5 Volt to 10 Volt range. It features power conversion efficiencies up to 98%. The Si7661 is a higher-voltage version of the Si7660 intended for input voltages from 7.5 Volts to 20 Volts.

The high-voltage switchmode regulators and controllers made by Siliconix employ high-performance D/CMOS power IC technology to combine CMOS current-mode controllers with high-voltage input regulation and output switching. This design allows Siliconix to build extremely high efficiency switchmode power supply circuits that can run directly from high-voltage inputs such as PBX or ISDN phone lines, or 100 VAC power lines.

The Si9100, Si9101 and Si9102 are switchmode regulators which include an integrated 5 Ω output MOSFET capable of supplying up to 5 Watt loads. They can be configured in single-ended converter topologies, and can be run directly from input voltages as high as 120 V. The major applications for these devices are in telecommunications equipment such as PBX feature phones, ISDN terminals, line-powered modems, and central office electronic equipment.

The Si9110 and Si9111 are switchmode controllers with the same features as the switchmode regulators, except that a push-pull output driver is utilized for driving an external MOSFET switch for higher power applications. These devices are generally used in telecommunications power supply applications greater than 5 Watts, as well as for general purpose dc/dc power converters.

The Si9115 and Si9116 are switchmode controllers designed to run directly from the rectified 110 Volt ac power line. Typical applications are in power supplies for electronic controls in appliances, small computers, and high-voltage avionics systems.

Data sheets for the Si91XX family of switchmode regulators and controllers may be found in the Siliconix Power Products Data Book.

Si7660
Monolithic CMOS Voltage Converter

Siliconix incorporated

FEATURES

- Improved – No External Diode Required
- Conversion of 5 V Logic Supply to ±5 V Supplies
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency
- Operating Voltage Range of 1.5 to 10 V
- Requires Only 2 Capacitors

BENEFITS

- Inexpensive Negative Supply from Positive Supply
- Easy to Use
- Minimum Parts Count
- Small Size
- No Diode Drop at Output

APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized µ-Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies for Analog Switches
- Data Acquisition Systems

DESCRIPTION

The Siliconix Si7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7660 performs a supply voltage conversion from positive to negative for an input range of +1.5 V to +10 V, resulting in a complementary output voltage of −1.5 V to −10 V with the addition of only two capacitors.

Typical applications for the Si7660 are data acquisition and microprocessor based systems where a +5 V supply is available for the digital functions, and an additional −5 V supply is required for the analog functions. The Si7660 is also ideally suited for providing low current, −5 V body bias supply for dynamic RAMs.

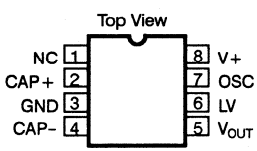
Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output n-channel switch substrates are not forward-biased. The epitaxial layer prevents latch up.

The oscillator, when unloaded, oscillates at a nominal frequency of 12 kHz for an input supply voltage of 1.5 to 10 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

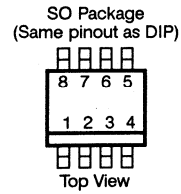
The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+3.5 to +10 V), the "LV" pin should be left disconnected.

Packaging for this device includes the plastic miniDIP, and SO options. Performance grades include industrial, D suffix (−40 to 85°C), and commercial, C suffix (0 to 70°C) temperature ranges. For additional information please refer to Applications Note AN84-2.

PIN CONFIGURATION

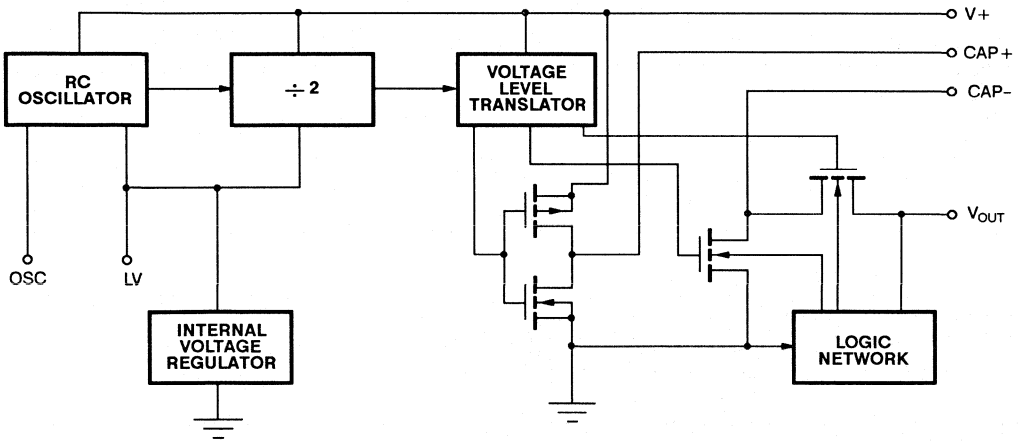


Order Number:
Plastic: Si7660CJ



Order Number:
Si7660DY

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 11 V
Oscillator Input Voltage . -0.3 V to (V+) +0.3 V, for V+ < 5.5 V
(V+) -5.5 V to (V+) +0.3 V, for V+ > 5.5 V
LV ..... No connection for V+ > 3.5 V
Storage Temperature (C & D Suffix) ..... -65 to 125°C
Operating Temperature (C Suffix) ..... 0 to 70°C
(D Suffix) ..... -40 to 85°C

Power Dissipation:*
8-Pin Plastic DIP** ..... 300 mW
SO-8** ..... 300 mW

*All leads welded or soldered to PC board.
**Derate 10 mW/°C above 75°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, C_{OSC} = 0[g]	TEMP[e]	TYP[d]	C, D SUFFIX MIN[b]	C, D SUFFIX MAX[b]	UNIT
INPUT							
Supply Voltage Range LOW	$V+_L$	R_L = 10 kΩ, LV = GND	Full		1.5	3.5	V
Supply Voltage Range HIGH	$V+_H$	R_L = 10 kΩ, LV = NC	Full		3	10	
Supply Current	I+	R_L = ∞, LV = NC	Full	100		250	µA
OUTPUT							
Output Source Resistance	R_{OUT}	V+ = 5 V, LV = OPEN I_O = 20 mA	Room Full	55		100 120	Ω
		V+ = 2 V, LV = GND I_O = 3 mA	Full			300	
Power Conversion Efficiency	PE_1	R_L = 5 kΩ	Room	98	95		%
Voltage Conversion Efficiency	$V_{OUT}E_1$	R_L = ∞	Room	99.9	99		

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SPECIFICATIONS[a]

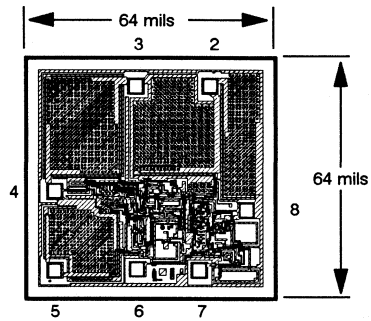
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified V+ = 5 V, C_{OSC} = 0[g]	TEMP[e]	TYP[d]	C, D SUFFIX MIN[b]	C, D SUFFIX MAX[b]	UNIT
DYNAMIC							
Oscillator Frequency[g]	f_{OSC}		Room	12			kHz
Oscillator Impedance	Z_{OSC}	V+ = 2 V, LV = GND	Room	1			MΩ
		V+ = 5 V	Room	100			kΩ

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Room = 25°C, Full = as determined by the operating temperature suffix.
g. For C_{OSC} > 1000 pF, C_1 and C_2 should be increased to 100 µF. C_1 = Pump Capacitor, C_2 = Reservoir Capacitor.

DIE TOPOGRAPHY

CSABA

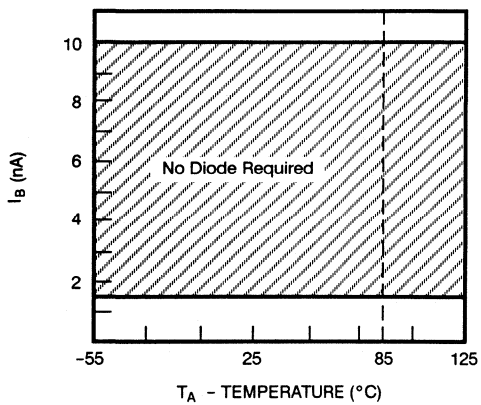
2 Resistors
1 Zener Diode
40 p-channel enhancement MOSFETS
1 Diode
3 Capacitors
48 n-channel enhancement MOSFETs



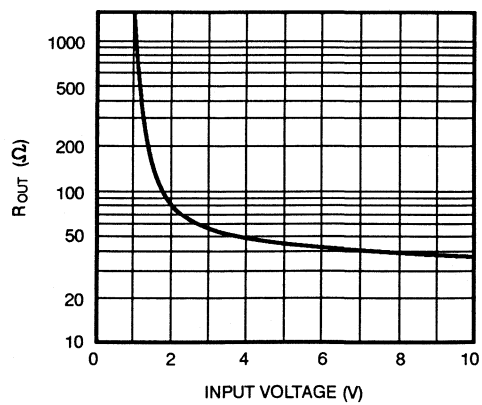
Pad No.	Function
2	CAP+
3	GND
4	CAP–
5	V_{OUT}
6	LV
7	OSC
8	V+

TYPICAL CHARACTERISTICS

Operating Voltage as a Function of Temperature

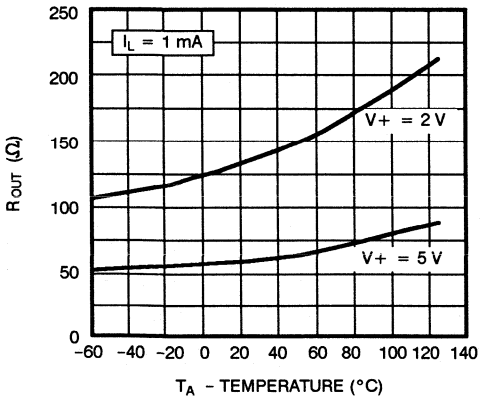


Output Source Resistance as a Function of Supply Voltage

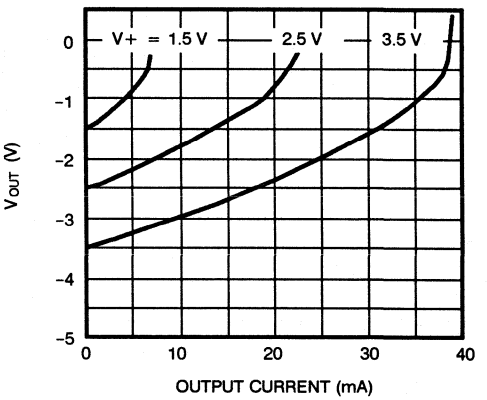


TYPICAL CHARACTERISTICS (Cont'd)

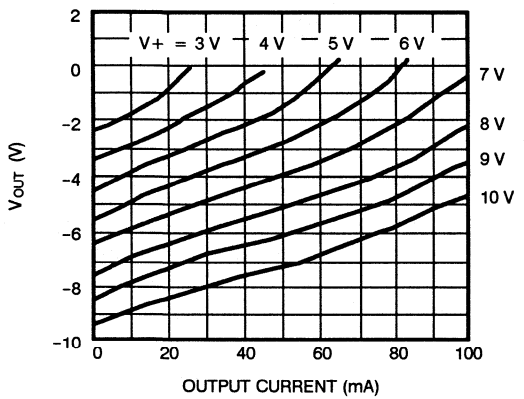
Oultput Source Resistance vs. Temperature



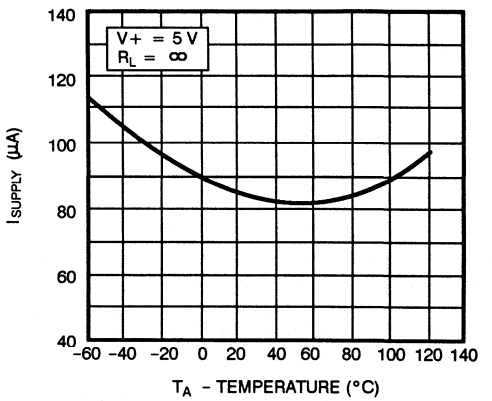
Typical Si7660 Output (LV = GND)



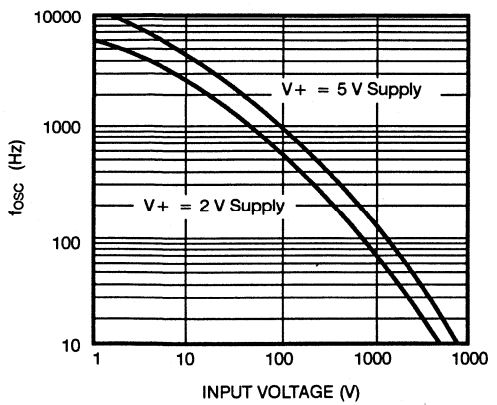
Typical Si7660 Output (LV = OPEN)



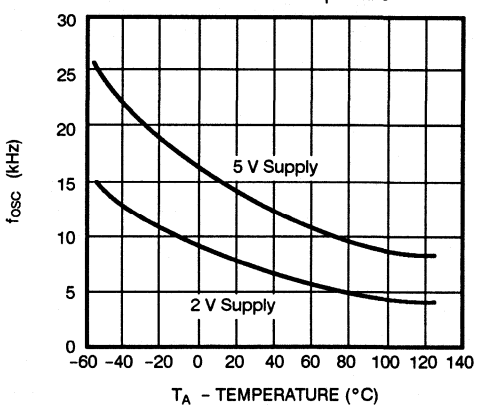
Typical Supply Current vs. Temperature



Oscillation Frequency as a Function of External OSC Capacitance



Unloaded Oscillator Frequency as a Function of Temperature



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TEST CIRCUIT

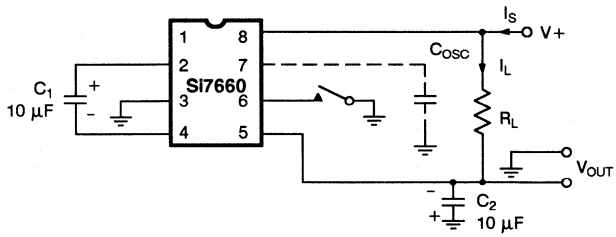
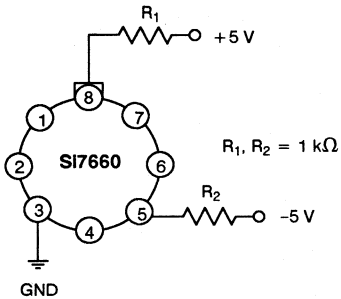


Figure 1.

BURN-IN CIRCUITS



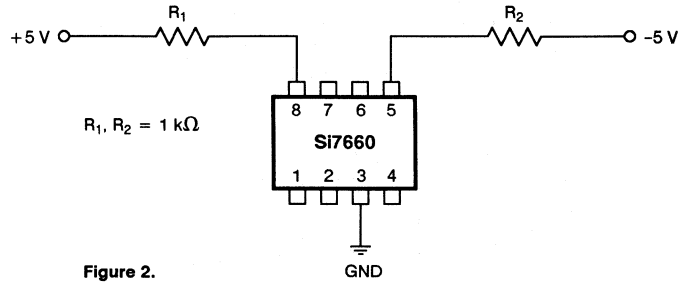


Figure 2.

APPLICATIONS

The Siliconix Si7660 is a VOLTAGE source, not a CURRENT source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or cause the device to go into power shutdown. To avoid problems, keep the VOLTAGE conversion concept in mind.

The Si7660 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7660 would do just as well as a full conventional negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

If the output ripple of the Si7660 is too great for a particular application, the value of the pump (C_1, Figure 3) and reservoir (C_2, Figure 3) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 µF.

The previous version of the Si7660 required a diode in series with pin 5 when operating above 6.5 V. The improved Si7660 does not require this diode. The improved version will work in existing circuits which have the diode.

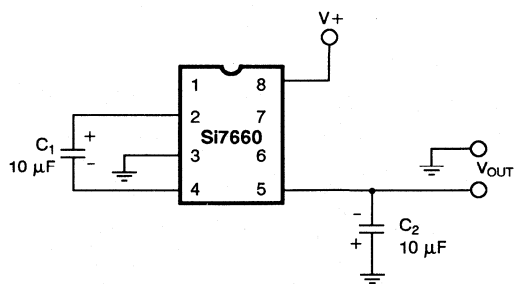


Figure 3. Basic Voltage Inverter Circuit

APPLICATIONS (Cont'd)

Figure 4 shows a circuit that will produce two output voltages utilizing both of the Si7660 features (i.e. inversion and doubling). The combined output current must be limited so the maximum device dissipation is not exceeded.

Two Si7660's can be paralleled to reduce the effective output resistance of the converter. The output voltage at a given current is increased since the voltage drop is halved when the devices are connected as shown in Figure 6.

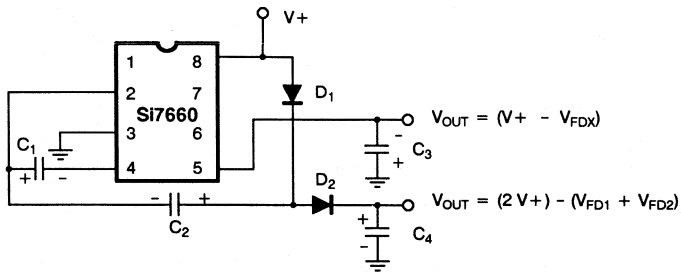


Figure 4. Combination Inverter/Multiplier Circuit

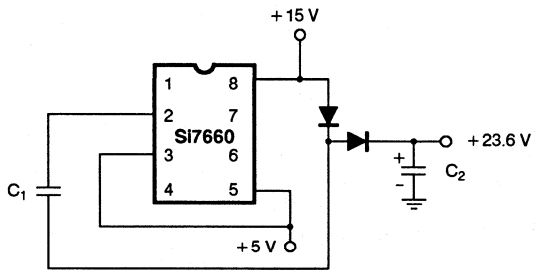


Figure 5. Creating +23.6 V from +15V and +5 V

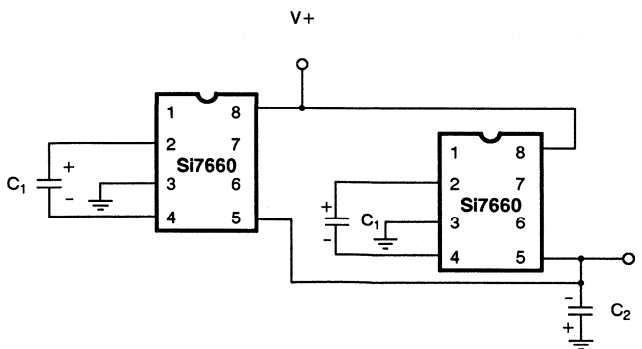


Figure 6. Paralleling Two Si7660s to Reduce the Effective Output Resistance

Si7661
Monolithic CMOS Voltage Converter

Siliconix incorporated

FEATURES

- Conversion of 4.5 V to 20 V to −4.5 to −20 V Supplies
- Voltage Multiplication ($V_{OUT} = (-)nV_{IN}$)
- 99.7% Typical Open Circuit Voltage Conversion Efficiency
- 95% Typical Power Efficiency

BENEFITS

- Inexpensive Negative Supply Generation
- Easy to Use, Requires Only 2 External Capacitors
- Minimum Parts Count
- Small Size

APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized µ-Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies for Analog Switches
- Data Acquisition Systems
- Up to −20 V for Op Amps and Other Linear Circuits

DESCRIPTION

The Siliconix Si7661 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The Si7661 performs a supply voltage conversion from positive to negative for an input range of +4.5 V to +20 V, resulting in a complementary output voltage of −4.5 V to −20 V with the addition of only two capacitors.

Typical applications for the Si7661 are data acquisition and microprocessor based systems, where a +4.5 to +20 V supply is available for the digital functions, and an additional −5 to −20 V supply is required for analog devices, such as op amps. The Si7661 is also ideally suited for providing low current, −5 V body bias supply for dynamic RAMs.

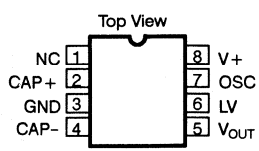
Contained on the chip are a voltage regulator, RC oscillator, voltage level translator, four power MOS switches, and a logic network. This logic network senses the most negative voltage in the device and ensures that the output n-channel switch substrates are not forward-biased. An epitaxial layer prevents latchup.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 4.5 to 20 V. The "OSC" terminal may be connected to an external capacitor to lower the frequency or it may be driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal regulator and improve low voltage (LV) operation. At high voltages (+8 to +20 V), the "LV" pin should be left disconnected.

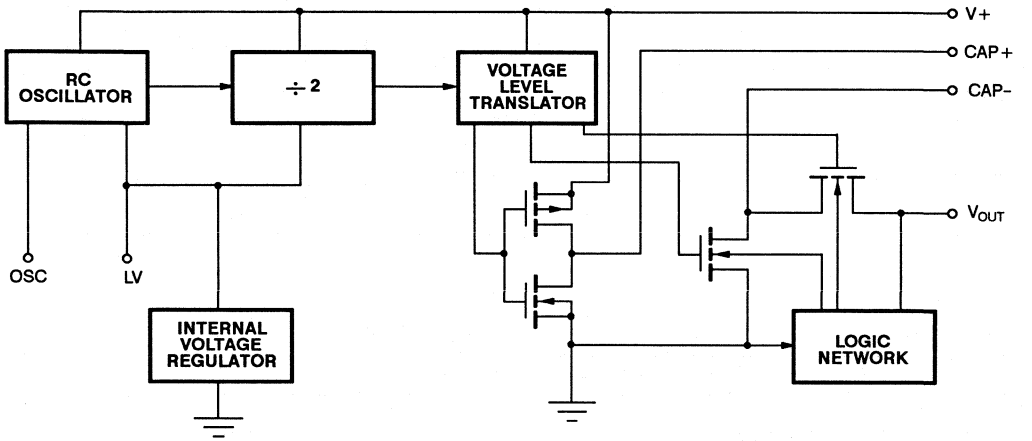
Packaging for this device is the 8-pin MiniDIP. For more information refer to AN84-2.

PIN CONFIGURATION



Order Number:
Plastic: Si7661CJ

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 22 V
Oscillator Input Voltage ... −0.3 V to (V+) +0.3 V, for V+ <8 V
(V+) −8 V to (V+) +0.2 V, for V+ >8 V
LV ..... No connection for V+ >9 V
Storage Temperature (C Suffix) ..... −65 to 125°C
Operating Temperature (C Suffix) ..... 0 to 70°C

Power Dissipation:*
8-Pin Plastic DIP** ..... 500 mW

*All leads welded or soldered to PC board.
**Derate 6.6 mW/°C above 25°C.

SPECIFICATIONS[a]

PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified C_{OSC} = 0[g]	TEMP[e]	TYP[d]	C SUFFIX MIN[b]	C SUFFIX MAX[b]	UNIT
INPUT							
Supply Voltage Range (LV)	$V+_{LV}$	R_L = 10 kΩ, LV = 0 V	Full		4.5	9	V
Supply Voltage Range	V+	R_L = 10 kΩ, LV = OPEN	Full		8	20	
Supply Current	I+	V+ = 4.5 V, R_L = ∞, LV = 0 V	Room	100		500	µA
		V+ = 15 V, R_L = ∞, LV = OPEN	Room	0.7		2	mA
OUTPUT							
Output Source Resistance	R_{OUT}	V+ = 4.5 V, LV = 0 V, I_O = 3 mA	Room	75			Ω
		V+ = 15 V, LV = OPEN, I_O = 20 mA	Room Full	55		100 120	
Power Conversion Efficiency	PE_1	V+ = 15 V, R_L = 2 kΩ	Room	92			%
Voltage Conversion Efficiency	$V_{OUT}E_1$	V+ = 15 V, R_L = ∞	Room	99.7	97		

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Siliconix incorporated

SPECIFICATIONS[a]

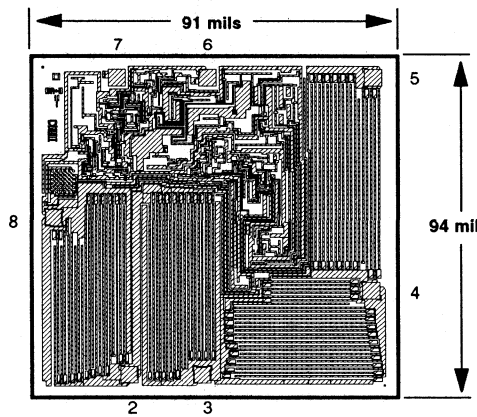
PARAMETER	SYMBOL	TEST CONDITIONS Unless Otherwise Specified C_{OSC} = 0[g]	TEMP[e]	TYP[d]	C SUFFIX MIN[b]	C SUFFIX MAX[b]	UNIT
DYNAMIC							
Oscillator Frequency[g]	f_{OSC}	V+ = 15 V	Room	10			kHz
Oscillator Impedance	Z_{OSC}	V+ = 4.5 V, LV = 0 V	Room	1			MΩ
		V+ = 15 V	Room	100			kΩ

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
g. For C_{OSC} > 1000 pF, C_1 and C_2 should be increased to 100 µF. C_1 = Pump Capacitor, C_2 = Reservoir Capacitor.

DIE TOPOGRAPHY

CSHA

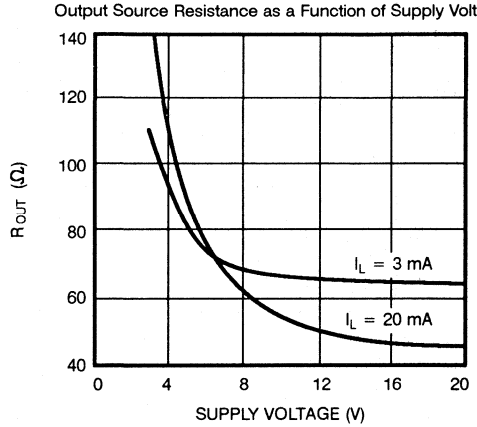
3 Capacitors
1 Resistor
1 Zener Diode
47 n-Channel Enhancement MOSFETs
40 p-Channel Enhancement MOSFETs



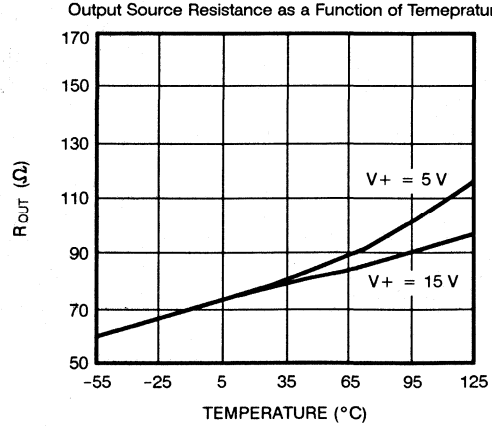
Pad No.	Function
2	CAP+
3	GND
4	CAP-
5	V_{OUT}
6	V_L
7	OSC
8	V+ (Substrate)

TYPICAL CHARACTERISTICS

Output Source Resistance as a Function of Supply Voltage

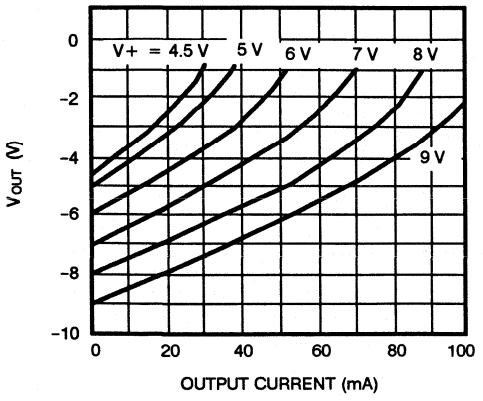


Output Source Resistance as a Function of Temeprature

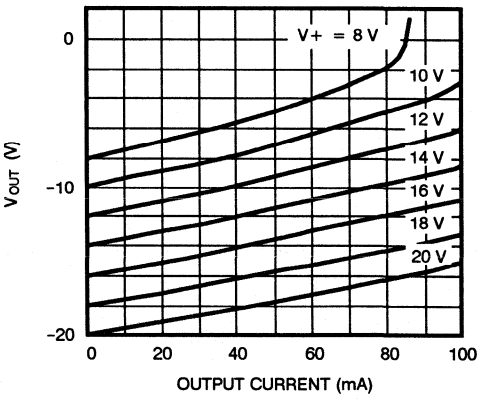


TYPICAL CHARACTERISTICS (Cont'd)

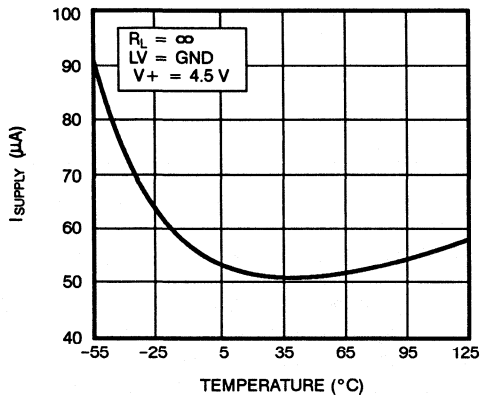
Typical Si7661 Output (LV = GND)



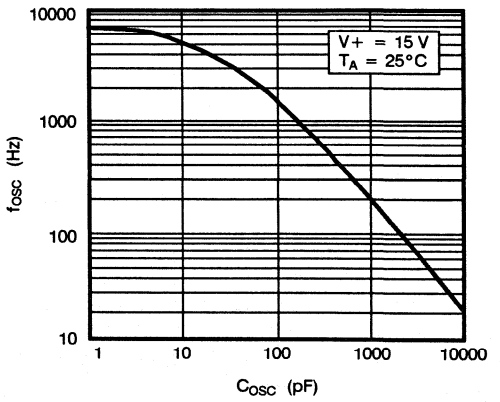
Typical Si7661 Output (LV = OPEN)



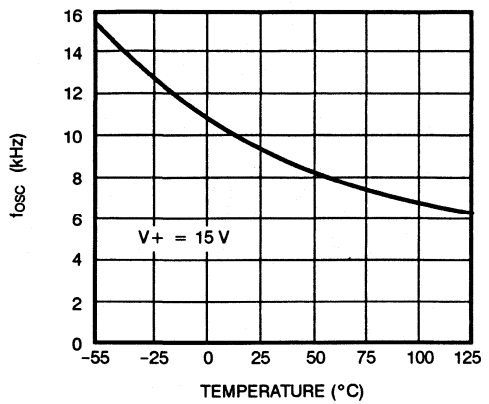
Supply Current vs. Temperature



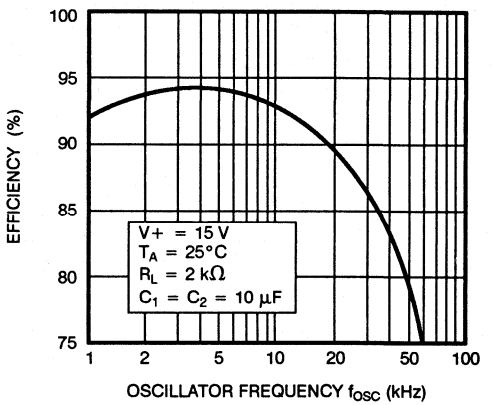
Frequency of Oscillation as a Function of External Oscillator Capacitance



Unloaded Oscillator Frequency as a Function of Temperature



Si7661 Power Efficiency vs. Oscillator Frequency



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TEST CIRCUIT

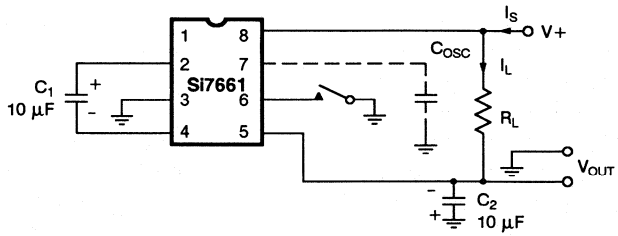


Figure 1.

BURN-IN CIRCUIT

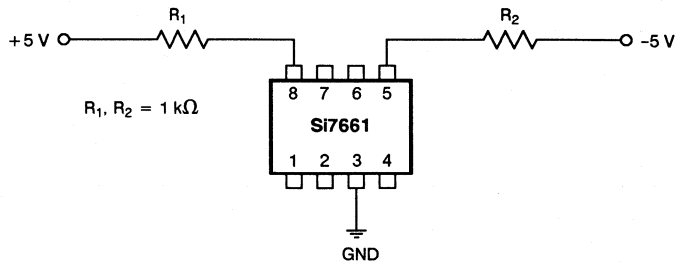


Figure 2.

APPLICATIONS

The Siliconix Si7661 is a VOLTAGE source, not a CURRENT source. Therefore, any heavy load current will either greatly reduce the output voltage (possibly out of the desired range) or will cause the device to go into power shutdown. To avoid problems, keep the VOLTAGE conversion concept in mind.

The Si7661 is intended for use as a voltage inverter. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. Some of the possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication. For more information refer to Application Note AN84-2.

There are many applications where a low current negative supply made with an Si7661 would do just as well as a full conventional negative supply or dc-to-dc converter module. Some examples are negative power supplies for microprocessors, dynamic RAMs, or data acquisition systems.

In addition, the extended input voltage range of the Si7661 lends itself for use as a negative generator for most op-amp applications.

If the output ripple of the Si7661 is too great for a particular application, the value of the pump (C_1, Figure 3) and reservoir (C_2) capacitors can be increased to reduce this effect. However, it is important to note that increasing the capacitor size can lead to surge currents at turn-on. If the current is too great, the power dissipation of the device can be exceeded, causing destruction of the device. The maximum recommended capacitor size is 1000 µF.

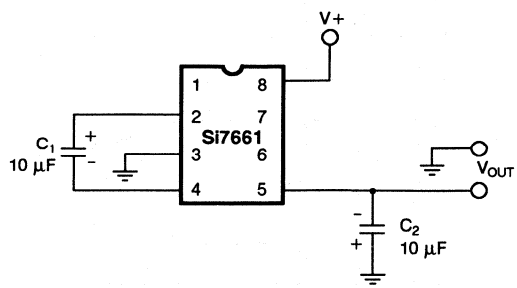


Figure 3. Basic Voltage Inverter Circuit

APPLICATIONS (Cont'd)

When an external clock is used to drive the Si7661 a 1 kΩ resistor should be used between the clock source and the OSC input (Pin 7) as shown in Figure 4.

Figure 5 shows a regulator that will operate with much less than 1 volt drop between V+ and V_{OUT} at large output currents. Most three terminal voltage regulators would exhibit a drop of a volt or more under these conditions.

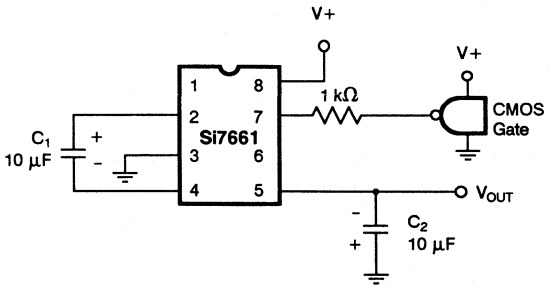
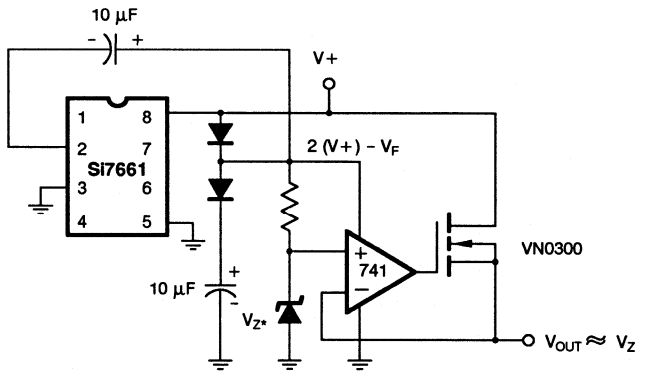


Figure 4. Driving the Si7661 with an External Clock



*The Zener voltage sets the output of the regulator.

Figure 5. Low Loss Regulator Circuit

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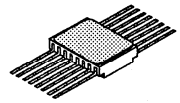
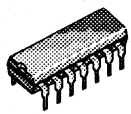
TABLE OF CONTENTS

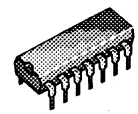
Integrated Circuits Package Overview



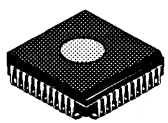
14–16 Pin
Flat Package
(L)



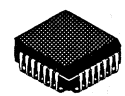
8–28 Pin
Ceramic DIP
(K)



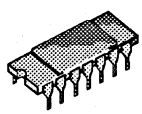
8–40 Pin
Plastic DIP
(J)



28–44 Pin
CerQuad Package
(M)



20–44 Pin
PLCC Package
(N)

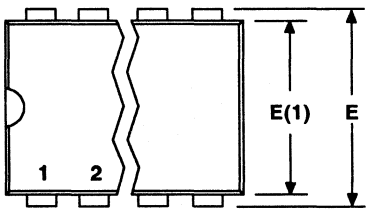


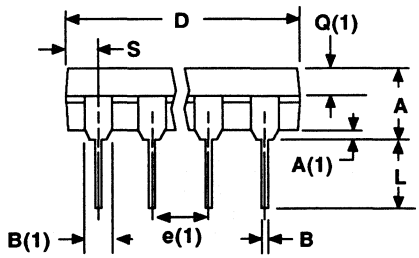
14–40 Pin
Side Braze DIP
(P, R)

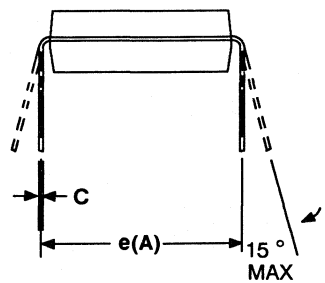
8–16 Pin
SO Package
(Y)

Plastic DIP (J Suffix), 8-20 Leads

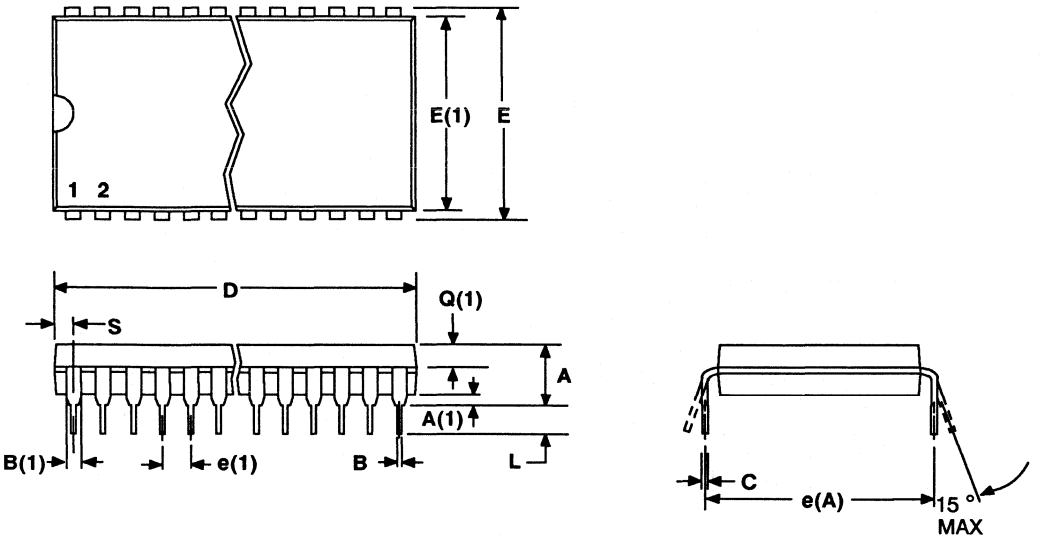
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	0.150	0.200
A(1)	0.38	1.27	0.015	0.050
B	0.38	.51	0.015	0.020
B(1)	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D-8	9.65	11.68	0.380	0.460
D-14	17.27	19.30	0.680	0.760
D-16	18.93	21.33	0.745	0.840
D-18	22.35	24.38	0.880	0.960
D-20	24.89	26.92	0.980	1.060
E	7.62	8.26	0.300	0.325
E(1)	5.59	7.11	0.220	0.280
e(1)	2.29	2.79	0.090	0.110
e(A)	7.37	7.87	0.290	0.310
L	3.175	3.81	0.125	0.150
Q(1)	1.27	2.03	0.050	0.080
S-8	1.02	2.03	0.040	0.080
S-14	1.02	2.03	0.040	0.080
S-16	0.38	1.52	0.015	0.060
S-18	1.02	2.03	0.040	0.080
S-20	1.02	2.03	0.040	0.080





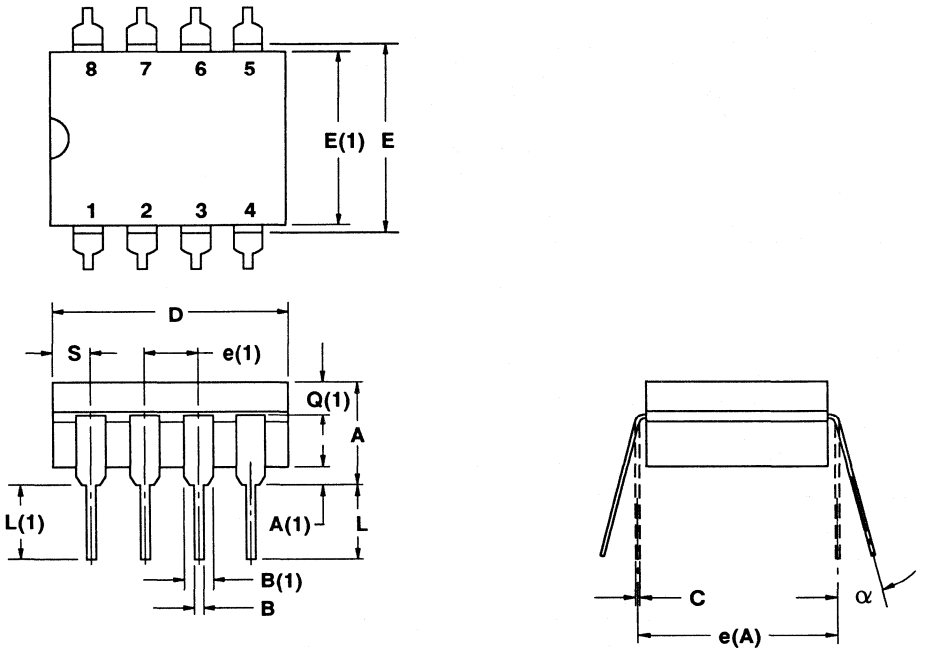


Plastic DIP (J Suffix), 24-40 Leads



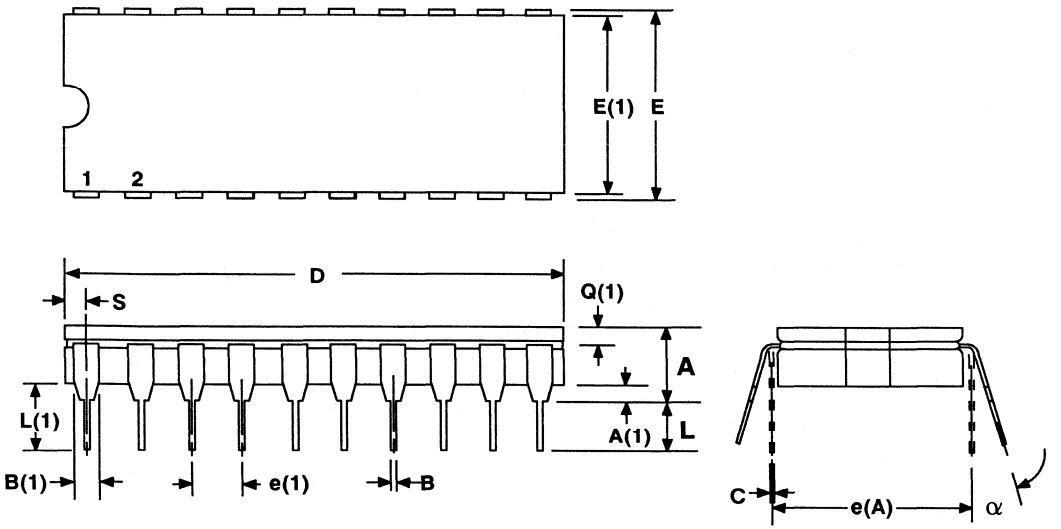
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	3.81	5.08	0.150	0.200
A(1)	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B(1)	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D-24	29.97	33.02	1.180	1.300
D-28	35.05	38.10	1.380	1.500
D-40	50.29	53.34	1.980	2.100
E	15.24	15.88	0.600	0.625
E(1)	13.21	14.73	0.520	0.580
e(1)	2.29	2.79	0.090	0.110
e(A)	14.99	15.49	0.590	0.610
L	3.175	5.08	0.125	0.200
Q(1)	1.27	2.03	0.050	0.080
S	1.02	2.54	0.040	0.100

CerDIP, 8 Lead



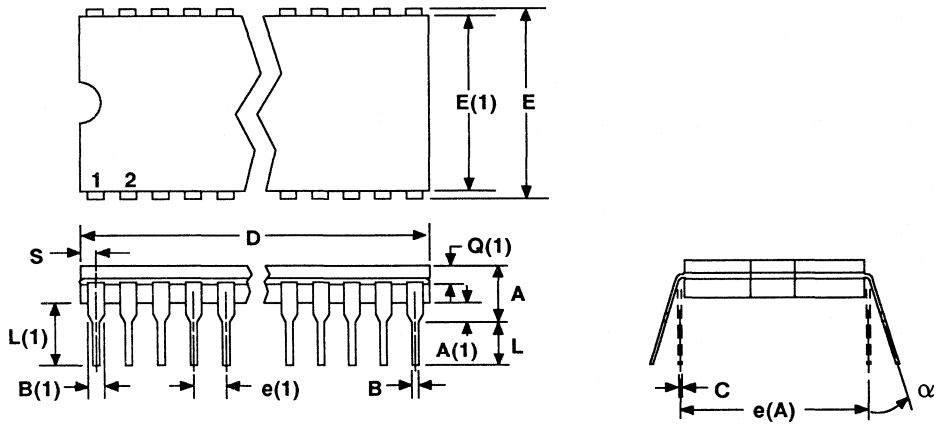
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	0.160	0.200
A(1)	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B(1)	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D	9.40	10.16	0.370	0.400
E	7.62	8.26	0.300	0.325
E(1)	6.60	7.62	0.260	0.300
e(1)	2.54 BSC		0.100 BSC	
e(A)	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L(1)	3.18	5.08	0.150	0.200
Q(1)	1.27	2.16	0.050	0.085
S	0.64	1.52	0.025	0.060
α	0 °	15°	0 °	15°

CerDIP (K Suffix), 14-20 Leads



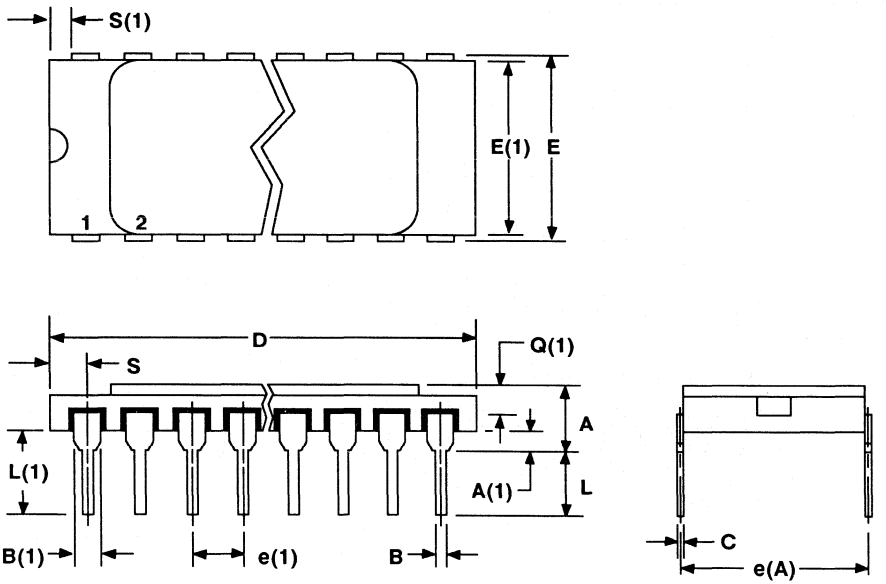
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	0.160	0.200
A(1)	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B(1)	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D-14	19.05	19.56	0.750	0.770
D-16	19.05	19.56	0.750	0.770
D-18	22.35	22.86	0.880	0.900
D-20	23.88	24.38	0.940	0.960
E	7.62	8.26	0.300	0.325
E(1)	6.60	7.62	0.260	0.300
e(1)	2.54 BSC		0.100 BSC	
e(A)	7.62 BSC		0.300 BSC	
L	3.18	3.81	0.125	0.150
L(1)	3.81	5.08	0.150	0.200
Q(1)	1.27	2.16	0.050	0.085
S-14	1.65	2.41	0.065	0.095
S-16	0.38	1.14	0.015	0.045
S-18	0.76	1.52	0.030	0.060
S-20	0.25	1.02	0.010	0.040
α	0 °	15°	0 °	15°

CerDIP (K Suffix), 24-28 Leads, 0.6" Wide Body



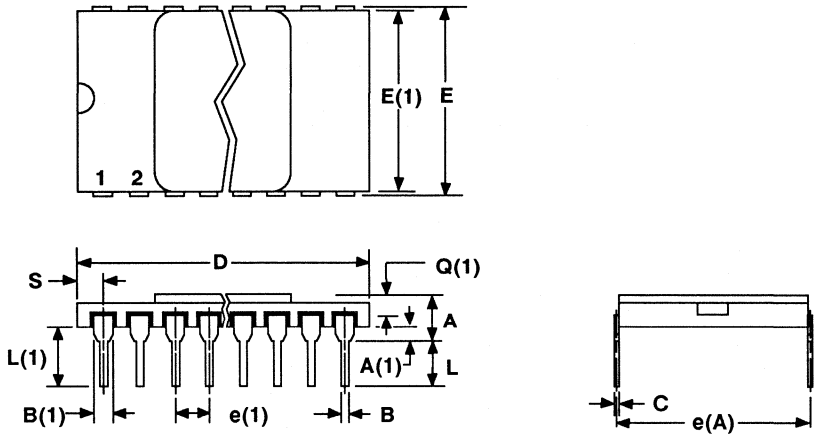
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.06	5.08	0.160	0.200
A(1)	0.51	1.14	0.020	0.045
B	0.38	0.51	0.015	0.020
B(1)	1.14	1.65	0.045	0.065
C	0.20	0.30	0.008	0.012
D-24	31.50	32.00	1.240	1.260
D-28	36.58	37.08	1.440	1.460
e(1)	2.54 BSC		0.100 BSC	
e(A)	15.24 BSC		0.600 BSC	
E	15.24	15.88	0.600	0.625
E1	12.95	13.46	0.510	0.530
L	3.18	3.81	0.125	0.150
L1	3.81	5.08	0.150	0.200
Q1	1.27	2.16	0.050	0.085
S	1.52	2.29	0.060	0.090
α	0 °	15°	0 °	15°

Side Braze DIP (P Suffix), 14-24 Leads



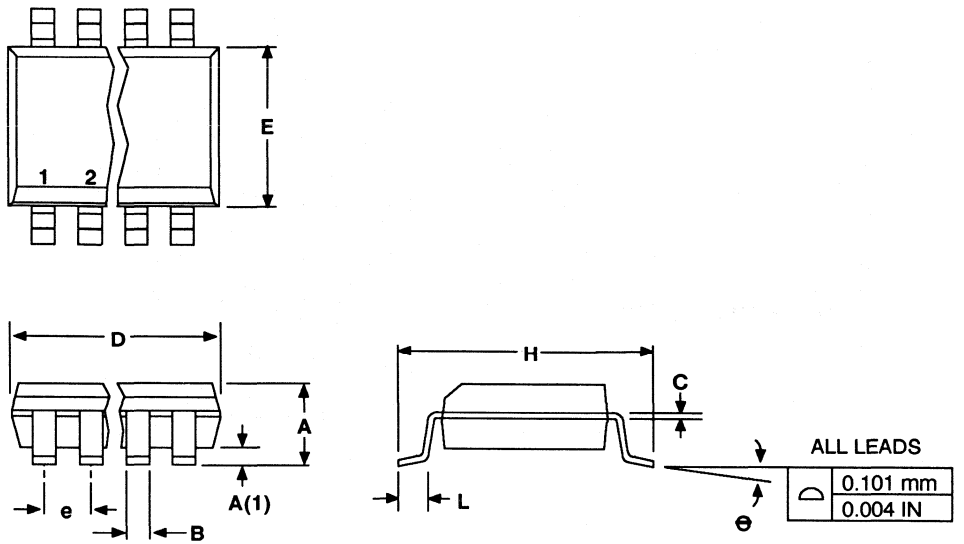
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.67	4.44	0.105	0.175
A(1)	0.64	1.39	0.025	0.055
B	0.38	0.53	0.015	0.021
B(1)	0.97	1.52	0.038	0.060
C	0.20	0.30	0.008	0.012
D-14	17.53	19.55	0.690	0.770
D-16	19.56	21.08	0.770	0.830
D-18	22.36	23.62	0.880	0.930
D-20	24.89	26.16	0.890	1.030
D-24	29.97	31.24	1.180	1.230
E	7.37	8.25	0.290	0.325
E(1)	7.12	7.87	0.280	0.310
e(1)	2.54 BSC		0.100 BSC	
e(A)	7.62 BSC		0.300 BSC	
L	3.18	4.44	0.125	0.175
Q(1)	0.25	–	0.010	–
S-14	0.77	2.41	0.030	0.095
S-16	0.51	1.65	0.020	0.065
S-18	0.77	1.65	0.030	0.065
S-20	0.77	1.65	0.030	0.065
S-24	0.77	2.41	0.030	0.095

Side Braze DIP (P, R Suffix), 24-40 Leads, 0.6" Wide Body



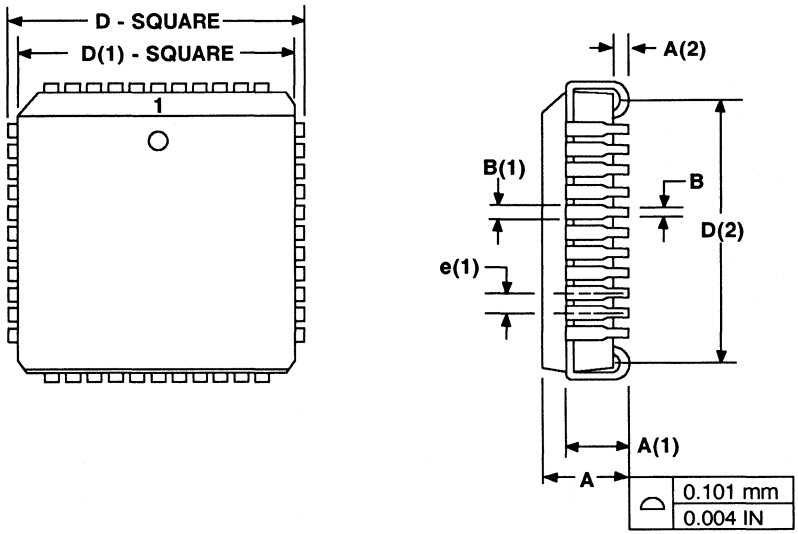
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	4.83	0.085	0.190
A(1)	0.51	1.78	0.020	0.070
B	0.38	0.58	0.015	0.023
B(1)	0.97	1.52	0.038	0.060
C	0.20	0.30	0.008	0.012
D-24	29.98	30.98	1.180	1.220
D-28	35.06	36.22	1.380	1.430
D-40	50.30	51.56	1.980	2.030
E	15.12	15.87	0.595	0.625
E(1)	14.73	15.49	0.580	0.610
e(1)	2.54 BSC		0.100 BSC	
e(A)	15.24 BSC		0.600 BSC	
L	3.18	4.45	0.125	0.175
Q(1)	0.25	–	0.010	–
S	0.76	1.65	0.030	0.065

SO Package (Y Suffix), 8-16 Leads, Narrow Body



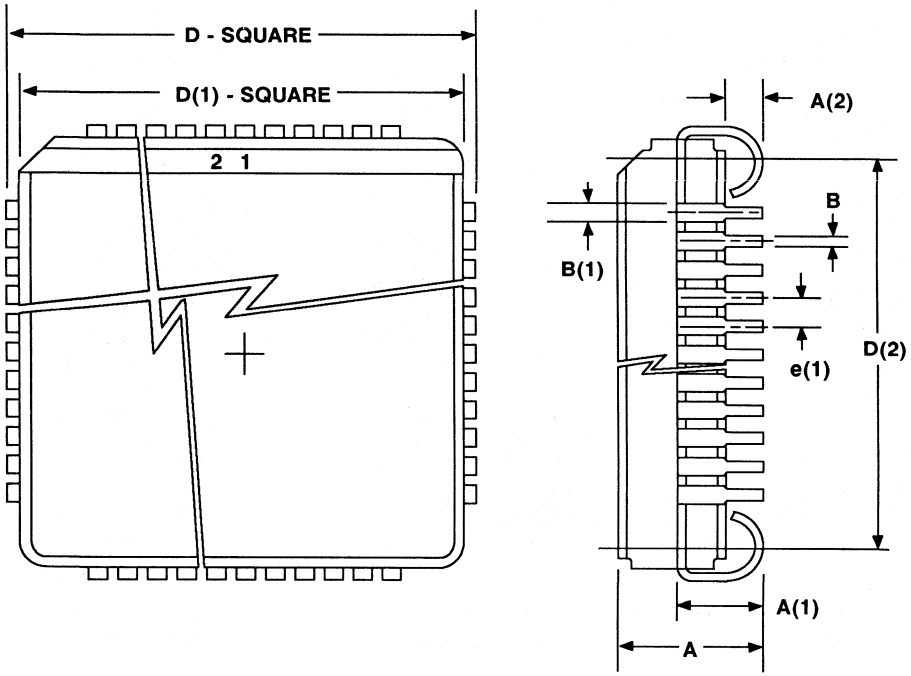
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.053	0.069
A(1)	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-14	8.35	8.95	0.329	0.352
D-16	9.60	10.20	0.378	0.402
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

PLCC Package (N Suffix), 20-44 Leads



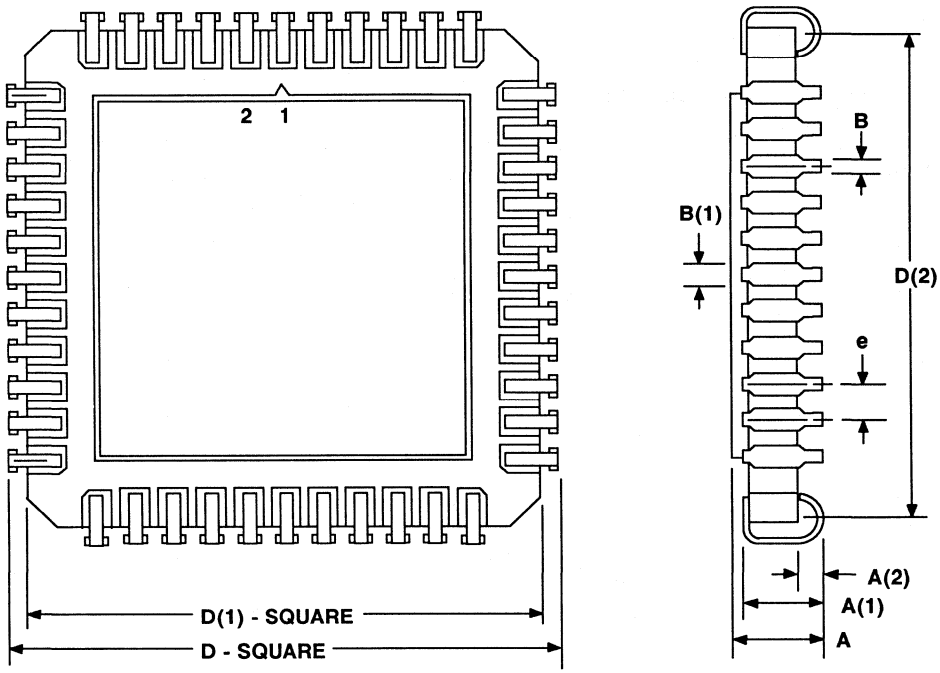
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.57	0.165	0.180
A(1)	2.29	3.04	0.090	0.120
A(2)	0.51	–	0.020	–
B	0.331	0.553	0.013	0.021
B(1)	0.661	0.812	0.026	0.032
D-20	9.78	10.03	0.385	0.395
D-28	12.32	12.57	0.485	0.495
D-44	17.40	17.65	0.685	0.695
D(1)-20	8.890	9.042	0.350	0.356
D(1)-28	11.430	11.582	0.450	0.456
D(1)-44	16.510	16.662	0.650	0.656
D(2)-20	7.37	8.38	0.290	0.330
D(2)-28	9.91	10.92	0.390	0.430
D(2)-44	14.99	16.00	0.590	0.630
e(1)	1.27 BSC		0.050 BSC	

CerQuad Package (M Suffix), 28 & 44 Leads



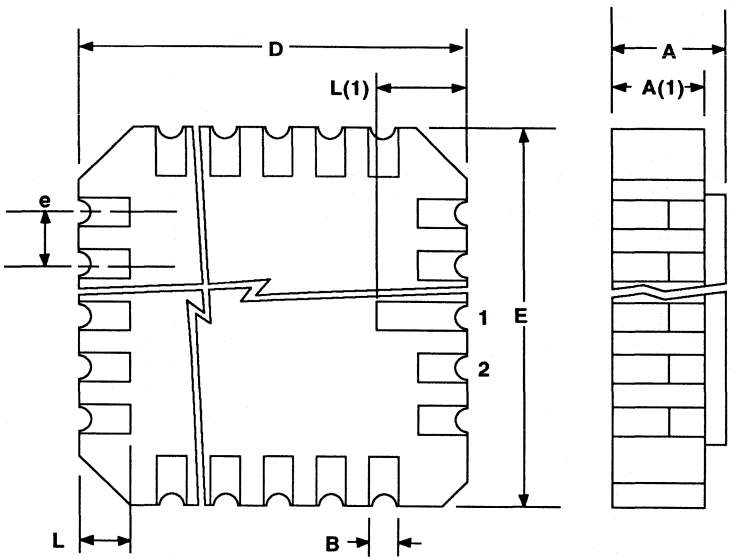
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.20	4.83	0.165	0.190
A(1)	2.29	3.04	0.090	0.120
A(2)	0.51	–	0.020	–
B	0.46	0.56	0.018	0.022
B(1)	0.66	0.81	0.026	0.032
D–28	12.32	12.57	0.485	0.495
D–44	17.40	17.65	0.685	0.695
D(1)–28	11.23	11.63	0.442	0.458
D(1)–44	16.31	16.71	0.642	0.658
D(2)–28	9.91	10.92	0.390	0.430
D(2)–44	14.99	16.00	0.590	0.630
e(1)	1.27 BSC		0.050 BSC	

CLCC Package (M Suffix), 44 Lead



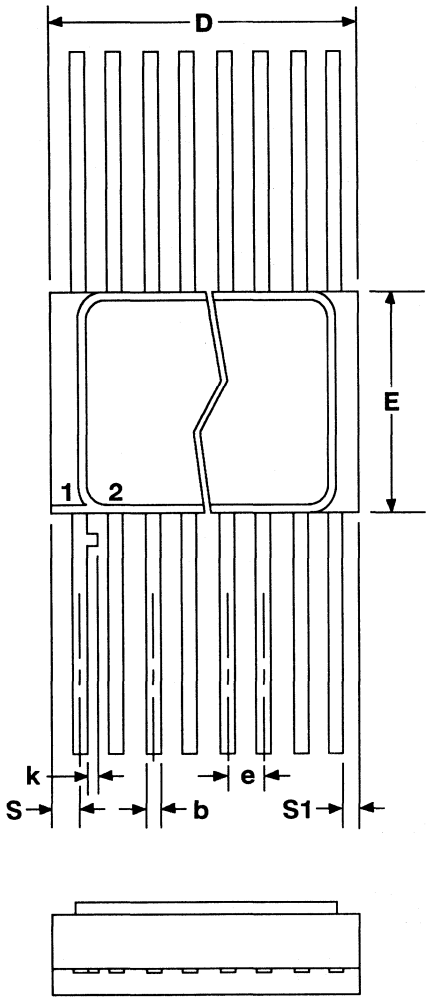
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.54	3.43	0.100	0.135
A(1)	2.03	3.30	0.080	0.130
A(2)	0.64	–	0.025	–
B	0.33	0.58	0.013	0.023
B(1)	0.51	0.81	0.020	0.032
D	17.27	17.78	0.680	0.700
D(1)	15.95	16.81	0.628	0.662
D(2)	14.99	16.51	0.590	0.650
e	1.27 BSC		0.050 BSC	

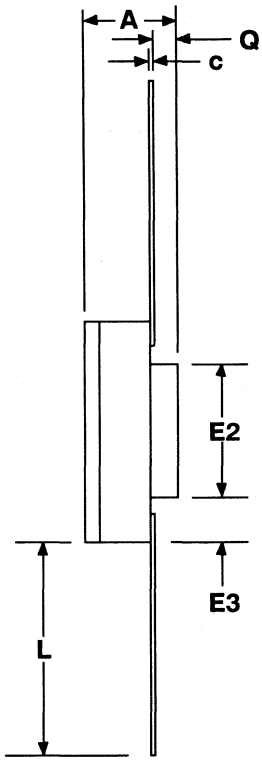
LCC Package (Z Suffix), 20 & 28 Leads



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.52	2.54	0.060	0.100
A(1)	1.27	2.16	0.050	0.085
B	0.56	0.71	0.022	0.028
D-20	8.69	9.09	0.342	0.358
D-28	11.23	11.63	0.442	0.458
E-20	8.69	9.09	0.342	0.358
E-28	11.23	11.63	0.442	0.458
e	1.27 BSC		0.050 BSC	
L	1.14	1.40	0.045	0.055
L(1)	1.96	2.36	0.077	0.093

Flat Package (L Suffix), 14 & 16 Leads

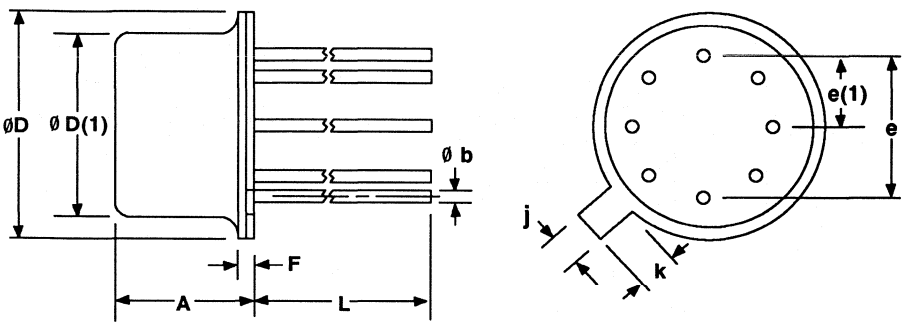




* New Outline Meets MIL-M-38510H

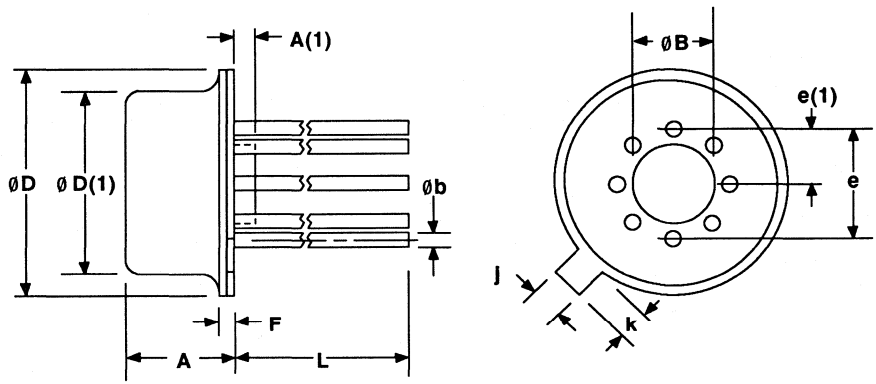
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.03	2.54	0.080	0.100
b	0.38	0.48	0.015	0.019
c	0.10	0.15	0.004	0.006
D-14	8.64	9.14	0.340	0.360
D-16	9.91	10.41	0.390	0.410
E-14	6.10	6.60	0.240	0.260
E-16	6.60	7.11	0.260	0.280
e	1.27 BSC		0.050 BSC	
E2	4.45	4.95	0.175	0.195
E3	0.76	1.27	0.030	0.050
k	0.20	0.38	0.008	0.015
L	7.62	8.89	0.300	0.350
Q	0.66	1.14	0.026	0.045
S	–	1.14	–	0.045
S1	0.13	–	0.005	–

MO-002AG (Formerly TO-78)



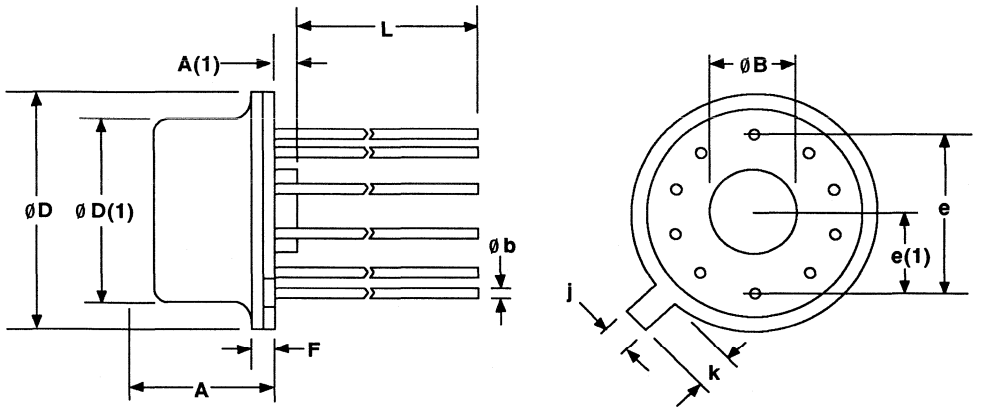
DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	0.165	0.185
Ø b	0.41	0.53	0.016	0.021
Ø D	8.51	9.39	0.335	0.370
Ø D(1)	7.75	8.50	0.305	0.335
e	5.08 BSC		0.200 BSC	
e(1)	2.54 BSC		0.100 BSC	
F	–	1.02	–	0.040
j	0.71	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	–	0.500	–

MO-002AK (Formerly TO-99)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	0.165	0.185
A(1)	0.25	1.01	0.010	0.040
ØB	3.56	4.06	0.120	0.160
Øb	0.41	0.53	0.016	0.021
ØD	8.51	9.39	0.335	0.370
Ø D(1)	7.75	8.50	0.305	0.335
e	5.08 BSC		0.200 BSC	
e(1)	2.54 BSC		0.100 BSC	
F	–	1.02	–	0.040
j	0.71	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	–	0.500	–

MO-006AD (Formerly TO-100)



DIM.	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.19	4.70	0.165	0.185
A(1)	0.25	1.02	0.010	0.040
Ø B	2.79	4.06	0.120	0.160
Ø b	0.41	0.53	0.016	0.021
Ø D	8.51	9.39	0.335	0.370
Ø D(1)	7.75	8.50	0.305	0.335
e	5.84 BSC		0.230 BSC	
e(1)	2.92 BSC		0.115 BSC	
F	–	1.02	–	0.040
j	0.71	0.86	0.028	0.034
k	0.74	1.14	0.029	0.045
L	12.70	–	0.500	–

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VIDEO CROSSPOINT SWITCH SIMPLIFIES LARGE MARTRIX DESIGNS

By Andy Fewster

The DG884 is a digitally selectable eight-input to four-output monolithic bidirectional crosspoint IC suitable for wideband analog and digital signal routing. Wideband here is used to define signals with bandwidths in the range of 60 to 200 MHz. Fabricated with the Siliconix D/CMOS technology, the DG884 incorporates n-channel DMOS switching FETs with low-power CMOS control logic, drivers, and latches. The low-capacitance DMOS FETs are connected as low on-resistance T-switches to achieve high levels of off-isolation and low levels of crosstalk. On-chip TTL-compatible address latches and data readback are included to simplify microprocessor interfacing. Double buffering of the switch addressing allows update information to be loaded without affecting the existing state of the crosspoint. A single SALVO command is all that is required to transfer previously set information to the current event latches. This single command significantly speeds up the setup time, especially in large matrices requiring more than one DG884.

The Signal Path

The internal function blocks of the DG884 are shown in Figure 1, and the signal path from one input to one output is shown in Figure 2. The signal path is composed of a T-switch at the matrix and an additional low-resistance switch in series with each output. The T-switch connection maximizes the off-isolation by shunting to ground any signal that feeds through the small series capacitances of the off series switches. The series output switches offer a number of advantages, namely:

- They provide an extra stage of isolation at the output
- They reduce the off-state output capacitance, which is necessary when other DG884 outputs are connected in parallel.
- They reduce the off-output leakage.

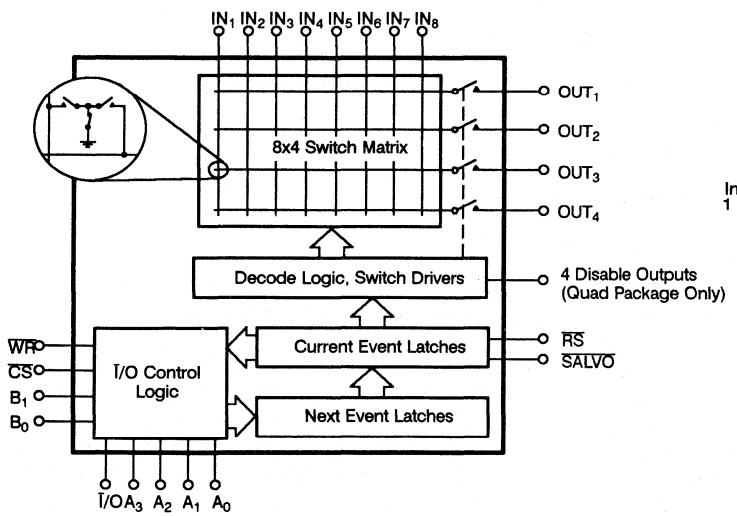


Figure 1. DG884 Block Diagram

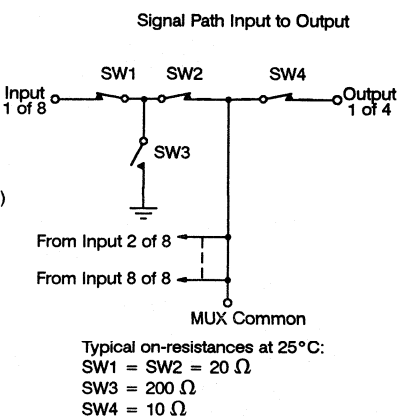


Figure 2. DG884 Signal Path

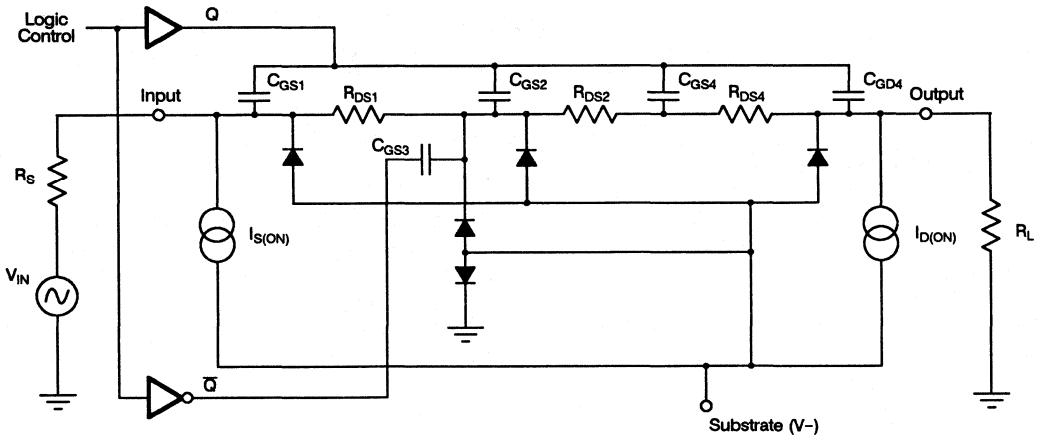
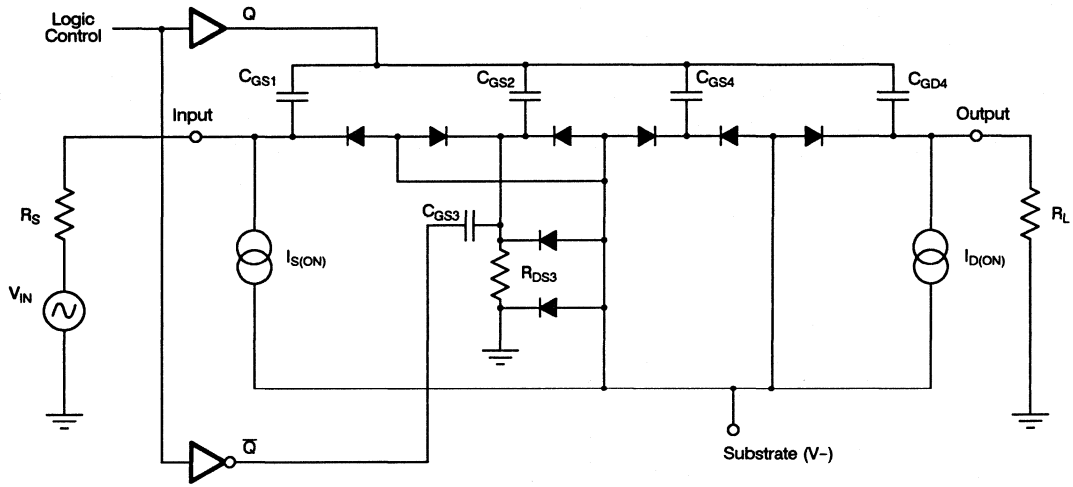


Figure 3. On-State Model



NOTE: Individual drain-source capacitances not shown for clarity.

Figure 4. Off-State Model

Figures 3 and 4 show low-frequency models of an "on" channel and an "off" channel, respectively. The models allow us to visualize the effects of leakage, low-frequency transmission loss, and analog overvoltage on the overall circuit performance. The term "low-frequency" is used for the models because they use single components to represent the characteristics of the channel. In other words, components distributed over an area of silicon are lumped together for simplicity's sake. An accurate high-frequency model of an "on" channel demands a more complex RC network (more on this later).

Leakage-Generated Offsets

Depending on the value of source and load impedances connected to input and output, leakage-generated offset voltages can be obtained using Ohms Law. In practice, however, the DG884 will be used surrounded by fast linear circuitry whose bias currents will be much higher than the nanoampere leakage currents of the D/CMOS process. Thus, offset voltages will be dominated by the external circuitry around the crosspoint and not the DG884.

Transmission Loss

Transmission loss is a function of the load connected to the crosspoint output for a fixed channel on-resistance and source impedance. Transmission loss is given by

$$\text{Loss (dB)} = 20 \log_{10} \frac{R_{load}}{R_{source} + R_{channel} + R_{load}}$$

Where $R_{channel} = R_{DS1} + R_{DS2} + R_{DS4}$.

This equation is accurate at frequencies below 1 MHz, where device capacitances (i.e., on-state input capacitance) can be safely ignored.

Input Overvoltage

Overvoltage effects are the third important characteristic that can be visualized from the models shown in Figures 3 and 4. Unlike mechanical switches, solid-state analog switches have electrical "end-stops" beyond which the switch ceases to behave as a switch. These "end-stops" are defined by the power supply rails. For an "on" channel, a signal at the input can swing to the negative rail before the shunt-switch body diodes (Figure 3) begin to conduct. When these diodes conduct, a large current from the negative rail can result. This current flow should be limited to 20 mA dc as defined in the absolute maximum ratings. During the period of negative overvoltage, the crosspoint outputs will be corrupted whether they are selected or not. A single diode in series with the negative rail will prevent reverse current flow and output corruption during negative overvoltage.

In the positive direction, if the input is allowed to continue rising towards the positive supply rail, its amplitude should be limited to the breakdown voltage of the body-to-source junction of the switching FETs. This is specified in the data sheet maximum ratings section, where a value of 14 V above the negative rail is quoted. Where rails of + 15 V and -5 V are used, the body-source breakdown voltage is the maximum positive limit of the signal at the source (input) or the drain (output) terminals. In a power down situation, where the positive and negative rails are at zero, the maximum positive input signal is also 14 V above the negative rail. No output corruption will occur during positive overvoltage.

Distortion

The change of on-resistance with signal swing, explained above, will give rise to distortion unless specific precautions are taken. A study of the equation for transmission loss reveals that distortion caused by changing on-resistance is inversely proportional to load resistance. Thus, distortion is given by

$$\text{DIST} = 20 \times \text{Log} (\Delta R_{on}/R_{load})$$

From the above, the decibel level below the fundamental may be calculated. Figure 5 shows how the on-resistance varies with signal swing. ΔR_{on} is 5 Ω for a signal swing of ± 5 V. Thus, for $R_{load} = 5\,k\Omega$, distortion is -60 dB. For low-frequency operation of the DG884 (where isolation and crosstalk performance may be critical in demanding applications), signal swings are usually much greater than those found at video frequencies and above. Thus, R_{load} should be increased accordingly. In all cases, some form of high-performance buffer/amplifier will be required at the output to translate the crosspoint load resistance to a lower "interface" value, i.e., 50 to 75 Ω for high-frequency designs.

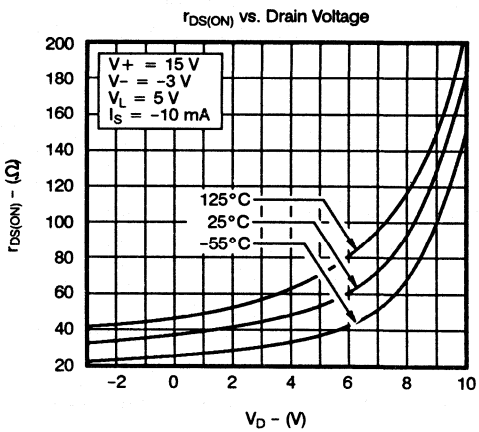


Figure 5. Change of On-Resistance with Signal Amplitude

Decoupling

A high-frequency signal path exists between the analog channel and the power rails via the gate-to-source capacitances of the switching FETs, as shown in Figures 3 and 4. This is because the drive logic applies either rail voltage to the gate via a low impedance path. Good decoupling shunts this signal leakage harmlessly to ground.

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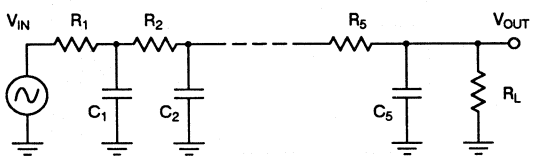
High-Frequency Model

The parameters that determine the frequency response of the selected crosspoint are input capacitance and on-resistance. Input capacitance is made up of interconnect lines on the chip, FET capacitance, and small bond wire and interconnect capacitances. On-resistance is made up of the three series FETs that form the crosspoint path. DMOS FETs are very efficient at providing low on-resistance in a small area; however, the resistance is spread over the entire channel length. Thus, resistance and capacitance are distributed, and the simple lumped models of Figures 3 and 4 are inadequate for high frequencies. Figure 6 shows a suitable model of an "on" channel. The five-stage model is easily obtained from the data sheet by taking on-resistance and capacitance values and dividing them by five to obtain the element values, as shown in Figure 6. Worst-case values are those obtained from a one input to four output set-up condition. Note that we show the model driven by a voltage source with zero output impedance -- the importance of this in maximizing operating bandwidth should not be underestimated. To generate the data sheet frequency curves, Siliconix uses a network analyzer to obtain V_{out}/V_{in} with respect to frequency. In this way, the device plots are independent of source impedance.



$$R_1 + R_2 + R_3 + ...R_n = r_{DS(ON)}$$
$$C_1 + C_2 + C_3 + ...C_n = (C_S + C_D)\ (ON)$$

Figure 6. Wideband On-Channel Equivalent Circuit

The DG884 is a high-performance device and must be driven by very high-performance analog buffers, such as the Siliconix Si581 and Si582. The accompanying performance curves were derived from an evaluation board consisting of Si581s at the inputs and gain-of-two Si582s at the outputs of a DG884.

The Digital Interface

The DG884 has comprehensive microprocessor interface facilities. A brief explanation of the sequence of commands required to set up the device follows.

A $\overline{\text{RESET}}$ command may be used as a power on reset. This will clear the current event latches and will result in all outputs being turned off. The $\overline{\text{RESET}}$ command operates on the current event address latches only. This is to allow existing or new data to be retained in the next event latches independent of the $\overline{\text{RESET}}$ operation.

To address the device, $\overline{\text{CHIP SELECT}}$ should be set low, I/O low, and $\overline{\text{RESET}}$, $\overline{\text{WRITE}}$, and $\overline{\text{SALVO}}$ all high. The input-to-output path is selected by $A_0 - A_3$ for the input, and B_0, B_1 for the output. Each addressing byte ($A_0 - A_3$) is latched into the next event latch (selected by the B_0, B_1 address) by the $\overline{\text{WRITE}}$ line going low and returning high again. This is repeated three more times to address all four output lines. Note that the internal logic forbids any addressing that tries to connect two separate inputs to the same output.

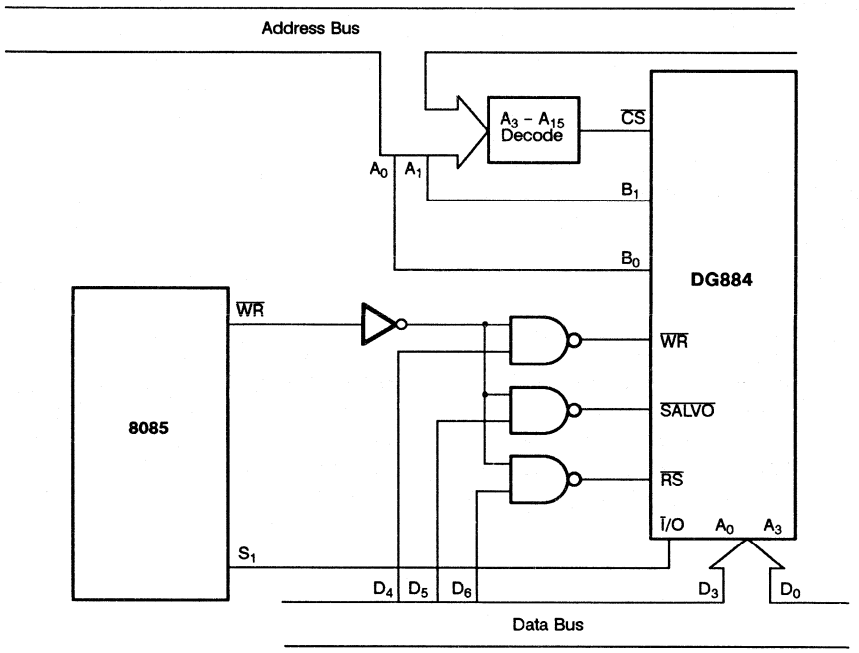
Having set four input-to-output paths into the next-event latches with four $\overline{\text{WRITE}}$ commands, the current event latches are then simultaneously loaded by $\overline{\text{SALVO}}$ going low and returning high.

The $A_0 - A_3$ address inputs are tri-stated when $\overline{\text{CHIP SELECT}}$ returns to high, along with $\overline{\text{RESET}}$, I/O, $\overline{\text{WRITE}}$, and $\overline{\text{SALVO}}$. This ensures that no bus contention will occur during input addressing or data readback when a number of devices are connected in parallel.

The DG884 has data readback built in. This useful facility enables a form of handshaking to verify that a particular address has been set. Data readback is enabled by the I/O line going high and $\overline{\text{CHIP SELECT}}$ going low on the device being interrogated.

Address A_3 functions as an output turn-off command. There are four open-drain $\overline{\text{DISABLE}}$ pins that are active low when the particular output is off. They are designed to interface directly with the disable pin of the Si582 current feedback op amp. For other uses, the DG884 $\overline{\text{DIS}}$ outputs look like 200 Ω to ground, when V+ = 15 V.

Figure 7 shows a memory mapped interface scheme for an 8085 microprocessor. From the circuit diagram, assume that the address decode gives a base address to the DG884 of 0 N_1 N_2 N_3 0 H, where N is a specific hex number. The A_0 and A_1 address lines connected to B_0 and B_1 inputs, respectively, of the DG884, map its address from 0 $N_{1\text{-}3}$ 0 H through to 0 $N_{1\text{-}3}$ 3 H (i.e., four address locations).



DATA									RESULT
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	$\overline{WR}$	
X	0	0	0	B	B	B	B		Nothing; $D_4 = 0$
X	0	0	1	B	B	B	B		4 -bit binary data written into one of four next event latches. The latch is decided by status of B_0 and B_1 lines.
X	0	1	0	X	X	X	X		Salvo pulse - updates current event latches.
X	1	0	0	X	X	X	X		Reset or clear pulse resets all latches and sets all switches to open circuit.

Figure 7. 8085 Microprocessor Interface

Four-bit data to be written to or read from the DG884 is applied to the A_0 - A_3 input lines. These inputs are connected to D_0 - D_3 of the computer data bus. Three of the higher order data bus lines, $D_{4,5,6}$ (D_7 is not used at all with the DG884), are used to gate the $\overline{WRITE}$ pulse through to either the $\overline{WRITE}$, $\overline{RESET}$, or $\overline{SALVO}$ inputs. The truth table gives the implementation of the gating shown in the circuit diagram.

To read four-bit data from the DG884 (i.e., the current event latch status), the $\overline{I}$/O terminal is connected to the S_1 output of the 8085. This signal provides an advance Read/Write control to the DG884. A read operation from the above four separate memory locations will give the status of each current event latch. Data being read from the DG884 will appear on the four lower data lines, D_0 - D_3, of the computer data bus.

Differential Applications

Although the DG884 is a single-ended 8 x 4 crosspoint, it may be used as a differential 4 x 2 crosspoint. Address A_2 defines inputs 1 - 4 or 5 - 8, while address B_1 defines the outputs, namely 1 and 2, or 3 and 4. A suitable wideband differential amplifier (Si582) at the output will provide common-mode rejection of incoming signals and charge injection thanks to the inherent path match within the crosspoint IC.

There is also a need for wideband two-input/output crosspoint systems when dealing with S-VHS (Super-VHS) signals. S-VHS is a much enhanced form of the VHS system from JVC, and it virtually eliminates signal degradation caused by multi-separation and combination of the luminance (Y) and chrominance (C) components that make up a color video signal. In S-VHS, separate Y and C signals are fed to the recorder, and at playback, Y and C signals are obtained for feeding directly to a suitable TV monitor, i.e., one fitted with an S-connector (SCART).

The S-VHS frequency spectrum extends the peak white portion of the FM signal from 4.8 MHz to 7 MHz. Thus there is a need for wideband two input/output crosspoint systems such as the DG884. Figure 8 outlines the DG884 as a 4 x 2 x 2 crosspoint. A key feature of this use is the reduced change of capacitance at the inputs, compared to the normal 8 x 4 connection. The worst-case input capacitance for one input to two outputs is 80 pF, and the worst case for one input to one output remains the same at 40 pF. Substituting these values into the HF model outlined above, bandwidth and source impedance trade-offs can be evaluated.

Power Supplies

The DG884 requires three power supplies for ground-referenced signal handling (V+, V–, and V_L = 5 V). The negative and positive supplies should always be established first. The logic supply should not be allowed to rise above the V+ pin during power supply on/off sequencing. This is because a PN junction exists between the V+ and V_L pins, and large currents could flow if this junction becomes forward biased. If both V+ and V_L are derived from the same supply there will be no problems. Figure 9 shows power supplies and decoupling for bipolar signal operation.

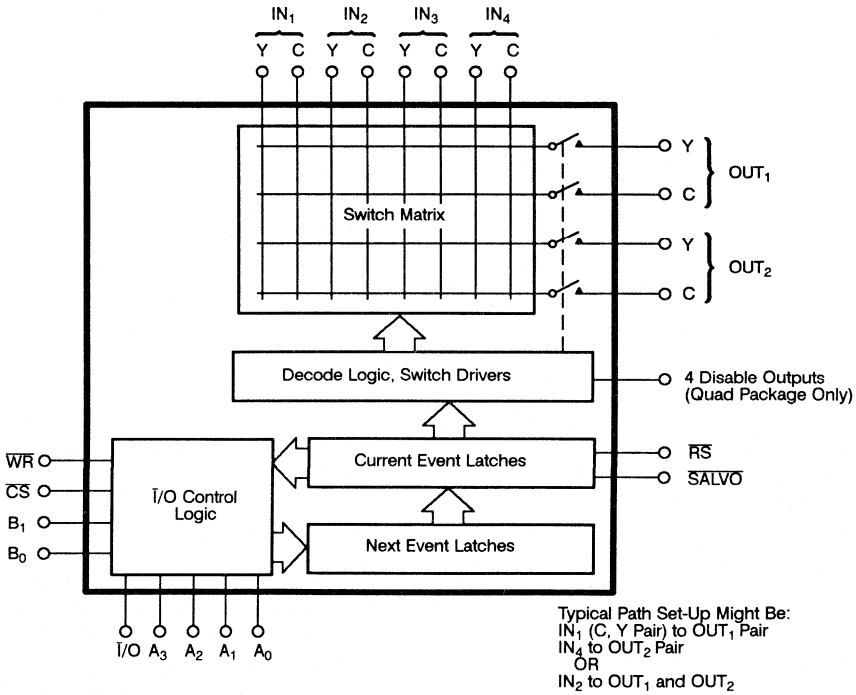


Figure 8. 4 x 2 x 2 Crosspoint

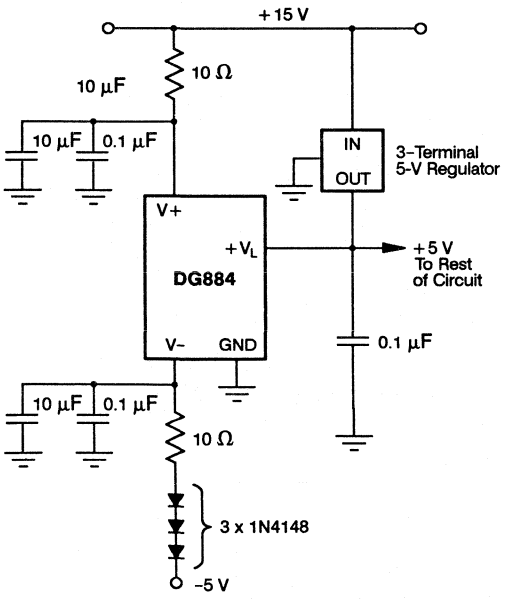


Figure 9. Power Supplies for DG884.

The DG884 may be operated in single supply situations (with V- connected to 0 V) with no loss of logic threshold accuracy. However, the signal should be offset to +3 V to preserve signal fidelity through the device.

Audio Operation

While the DG884 was designed for wide bandwidth applications, its excellent crosstalk and isolation specifications resulting from the T-switch configuration, together with the high level of integration (four 8-channel multiplexers in one package), make the part very attractive for audio applications. Used with load resistors of 1 MΩ or more, the distortion is below 0.01% for audio signals at -10 dBu (0.316 V_{RMS}) level when powered from +12 V and -5 V supplies. The high value load resistors can cause excessive levels of noise at the output amplifier when the crosspoint is disabled. This can be reduced by using the $\overline{\text{DISABLE}}$ outputs of the crosspoint to shunt the high value load resistors to ground during disable mode.

Layout Considerations

As with all high-frequency work, good PCB layout practice is essential if the inherent device performance is not to be degraded. Maximum ground plane area ensures that circuit ac ground really has low impedance. The inter-channel ground pins of the DG884 provide essential screening between channels right to the silicon, as well as separate return paths for each input. Thus input crosstalk is doubly improved. Similar considerations apply for the output inter-channel grounds.

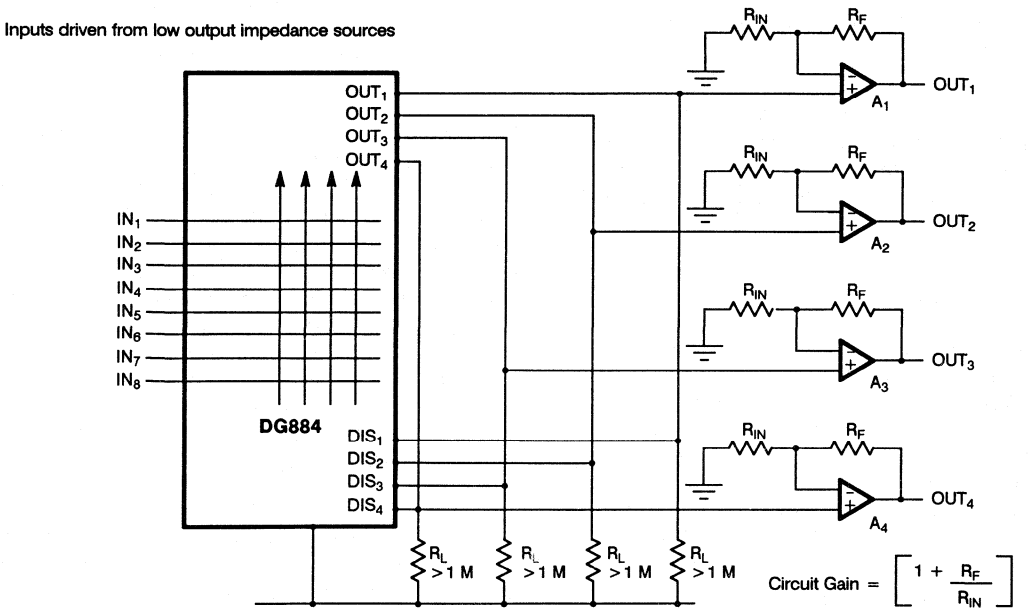


Figure 10. Audio Voltage-Mode Crosspoint

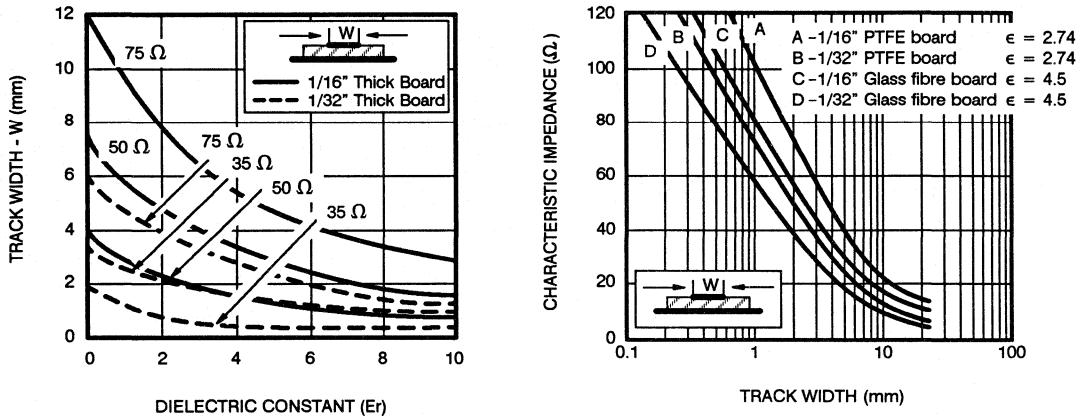


Figure 11. PCB Trace Characteristic Impedance

The inherent channel match of the monolithic DG884 can be upset by poor external layout. Ideally all input lines to and from the inputs and outputs should be exactly the same electrical length to minimize external path (and therefore phase) differences between the channels.

It may be useful to incorporate transmission lines on the PCB where the layout forces lengthy track runs. In this case, the curves in Figure 11 will help define trace geometry to obtain particular characteristic impedances, such as 50 to 75 Ω.

The importance of good decoupling has already been mentioned. However, it is worth stressing that component placement should ensure the absolute minimum track length from the decoupling point to ground.

Evaluation Results

Figure 12 shows the circuit diagram of the DG884 evaluation board used with the Si581 as an input buffer and the Si582 gain-of-two amplifier at the output. The Si582s provide output disable and "loss-less" cable termination. Thanks to its excellent reverse gain characteristics, the input Si581 provides a solid input impedance of 75 Ω that is independent of the path setting of the DG884. Ideally, the outputs of the Si581s should feed directly to the crosspoint inputs. However, the capacitive load presented by the DG884 reacts with the open-loop output impedance of the Si581 to cause amplitude peaking by reducing the feedback within the buffer at increasing frequencies. A series resistance at the output of the buffer corrects for this. From the Si581 data sheet, a value of 12 Ω is required for load capacitances of about 150 pF, which corresponds to the worst-case on-state capacitance of the DG884 when set for one input to all outputs.

At the output, the 4.7 kΩ load is chosen as a compromise between loading and output offset. With this value, offsets will typically be less than 10 mV.

Figures 13 and 14 show gain and phase plots obtained from the circuitry shown in Figure 12. Figure 13, the response for one input to one output, shows a bandwidth of 150 MHz. Figure 15, the response for one input to four outputs simultaneously, shows a bandwidth of 55 MHz. Figure 14 shows the measurement setup. The plots are typical of all channel selections and demonstrate the change in bandwidth between best- and worst-case path selections. The prototype showed a maximum delta phase shift of 10° at 30 MHz across inputs 1 through 8. This equates to a differential delay of 0.9 ns and is probably due to the input trace layout on the PCB, adding some 10 cm (worst case) differential path length.

The isolation available from a disabled output (all other outputs driven and terminated) is in reality a measure of the output adjacent crosstalk of the prototype and shows a healthy -50 dB at 30 MHz (Figure 16).

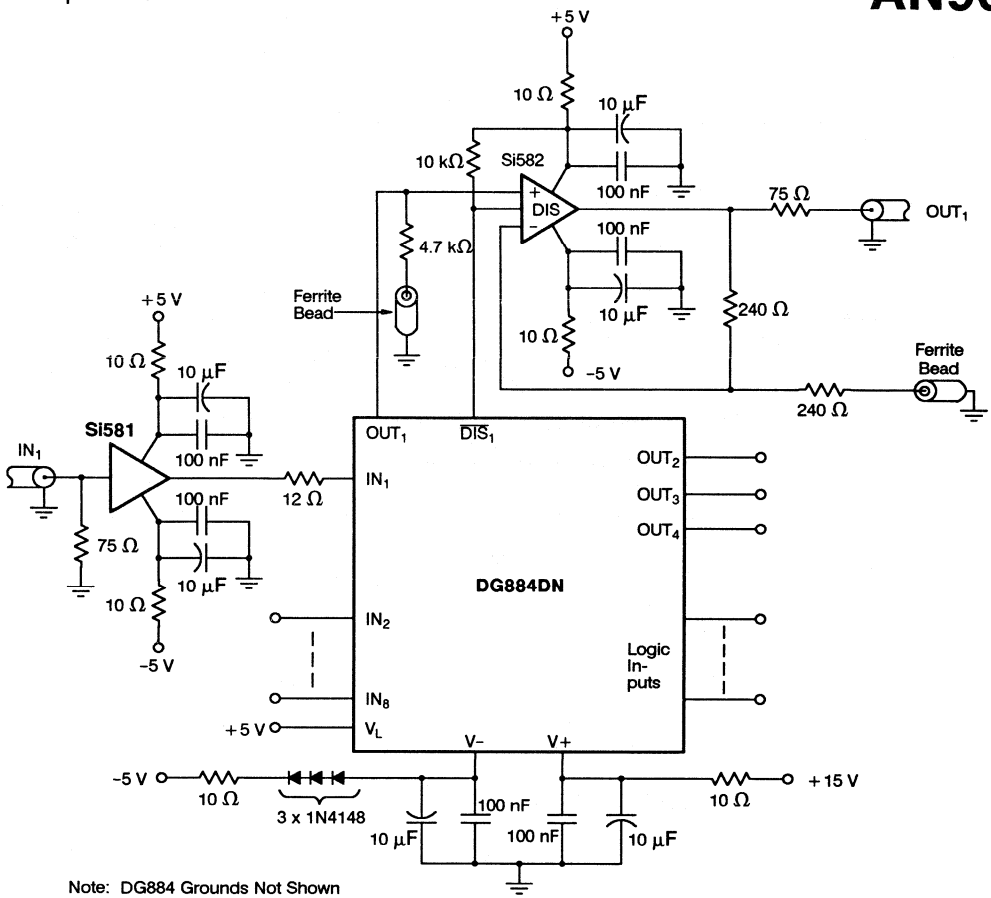


Figure 12. DG884 Wideband Crosspoint

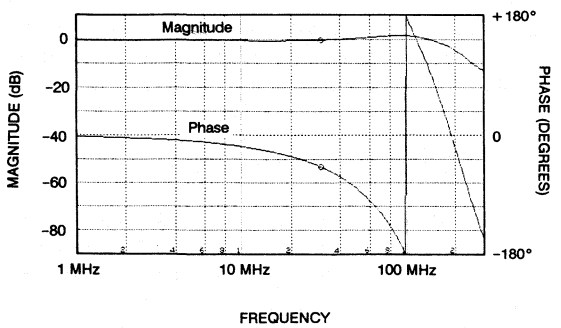


Figure 13. Response for One Input to One Output

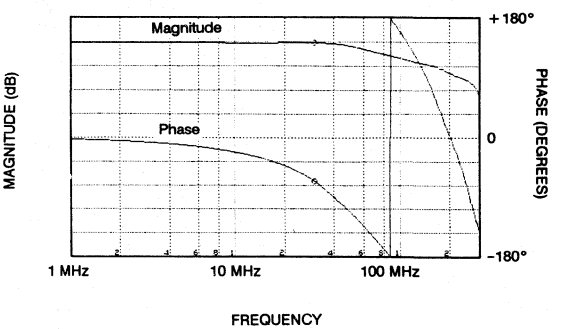
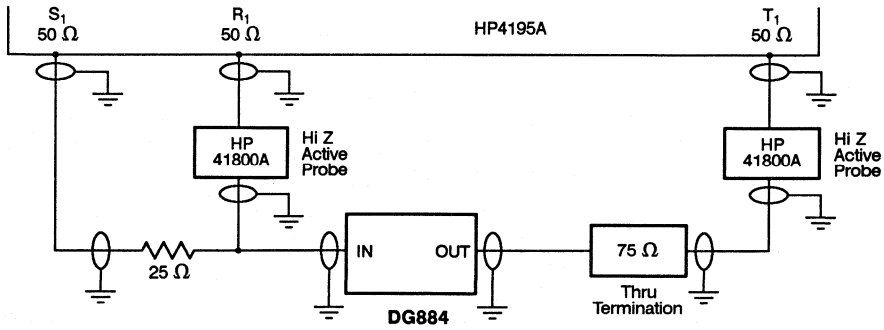


Figure 14. Response for One Input Going to All Four Outputs



Oscillator Level Set to 0 dBm

Figure 15. Network Measurement

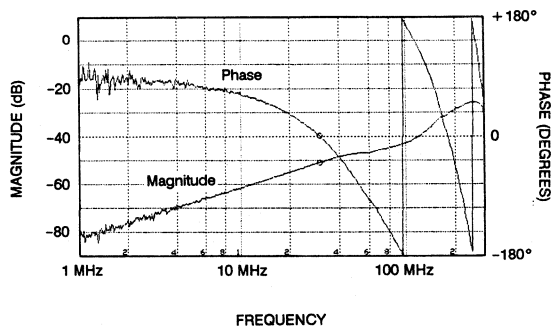


Figure 16. Output Isolation

To measure the overall distortion of the DG884 setup, two methods were chosen. Differential gain and phase are well known to the video community and show how well the overall signal path maintains a constant small-signal gain and phase for the low-level color carrier at 4.43 MHz (PAL) or 3.58 MHz (NTSC) as the brightness (luminance) signal is ramped through its specified range. The second method uses a two-tone intermodulation test to determine large signal performance and arrive at a figure of merit known as third-order intercept point. This is well known to communication engineers who need to judge the ability of a channel to resolve small signals in the presence of many large ones without the benefit (and complexity) of filter selectivity. The differential gain and phase measurements were made using a network analyzer (HP4195A), and a distortion analyzer (Marconi TF2910/4) was used to provide a cross check. Figure 17 shows the measurement setup for the analyzer, and Figure 18 shows the Marconi setup.

The results from the analyzer are shown in Figure 19 for one input to one output, and in Figure 20, for one input to four outputs, the latter being the worst-case loading. The analyzer test signal was a ramp of 700 mV with a 280 mV peak, 4.43 MHz signal superimposed to represent the dynamics of a video signal. The analyzer plots clearly show the gain reduction (negative slope) at peak brightness and also the phase change .

Tests with the Marconi set up showed that differential gain and phase measurements were below 0.08% and 0.05 °, respectively, when the test waveform was an EBU International Test Line signal C. Measurements below 0.1% and 0.1° are difficult to resolve with the Marconi setup, which is why the analyzer method was tried as well.

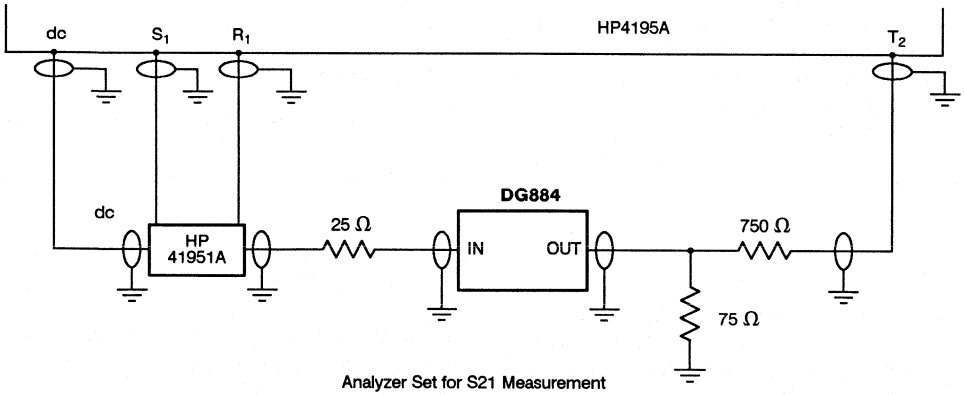


Figure 17. Differential Gain and Phase

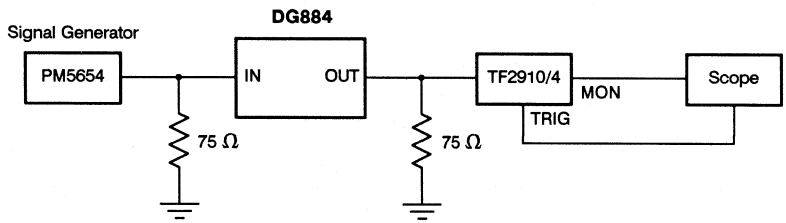


Figure 18. Marconi TF2910/4 Setup

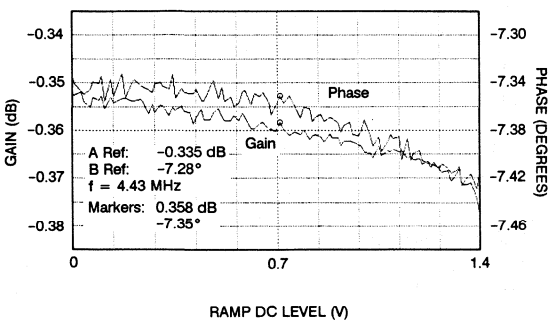


Figure 19. One Input to One Output

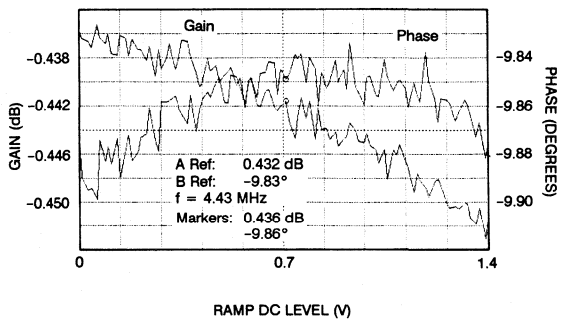


Figure 20. One Input to Four Outputs

9

The setup for the third-order intercept measurement is shown in Figure 21, and a plot of the of results is shown in Figure 22. The test was for one input to four outputs simultaneously. A signal spacing of 1 MHz was chosen to reflect the broadband nature of the crosspoint setup. For two signals at −10 dB, the third-order products were −60 dB, giving an intercept point of +30 dBm -- a very respectable figure.

Summary

The DG884 wideband crosspoint IC extends the state-of-the-art in monolithic wideband switching technology. Accompanied by the Si581 and Si582 linear ICs, the DG884 further simplifies the task of designing low-distortion wide-bandwidth crosspoint systems.

Note: an evaluation PCB, providing a working 8 x 4 wideband crosspoint with 75 Ω interface is available from Siliconix. Check with your local Siliconix sales office for details.

References

G.R. Jessop, RSGB VHF UHF Manual, 4th edition.

E.C. Jordan, ed., Reference Data for Engineers, 7th edition.

Fink and Christiansen, eds., Electronic Engineers Handbook, 3rd edition.

Brain D. Mathews, Harris Semiconductor, "Make Accurate Measurements on Video Systems", Electronic Design, March 3, 1988.

Comlinear application note OA-08.

Gareth Powell, Siliconix application notes AN86-1 and AN89-4.

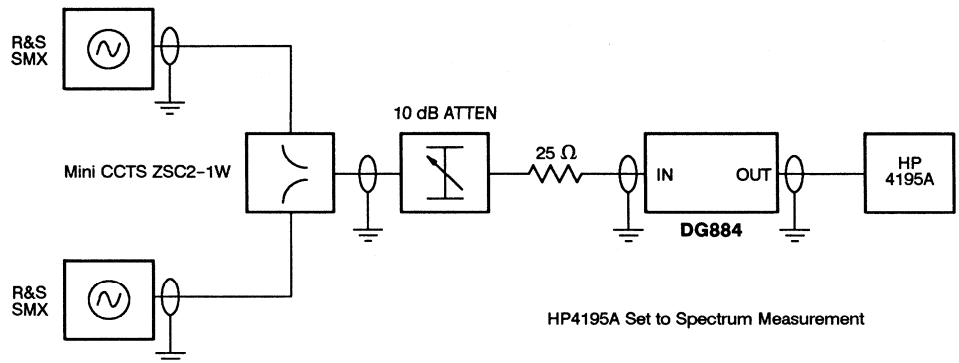


Figure 21. Two-Tone Intermodulation Test

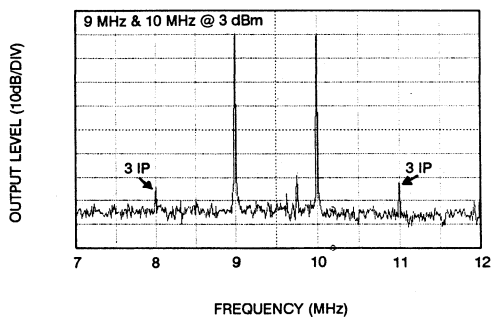


Figure 22. Third Order Intercept Points

Si581 WIDEBAND BUFFER APPLICATIONS

Andy Fewster

The new Si581 is a monolithic, closed loop, unity gain buffer amplifier. It features truly wideband, low distortion signal handling capability, and is an excellent complement to the Siliconix family of D/CMOS wideband/video switches and multiplexers (DG53x and DG54x).

Siliconix' wideband switches and multiplexers require high-performance impedance transformation to and from a 50- or 75-Ω environment without significant transmission loss. To drive coaxial cables or any "reactive" load, the Si581 may be used alone or in combination with a suitable wideband op amp. Reactive loads require a low-impedance source (<50 Ω) to preserve the operating bandwidth. Features and characteristics of the Si581 are listed in Table 1.

Table 1. Si581 Typical Characteristics (R_L = 100 Ω)

Parameter	Condition	Si581
dc output current	R_L = 100 Ω	±70 mA
Slew rate	±5-V supplies	800 V/µs
-3-dB bandwidth (MSBW)	V_O = 1 V_{pp}	450 MHz
-3-dB bandwidth (LSBW)	V_O = 5 V_{pp}	90 MHz
Voltage gain	V_O = 5 V_{pp}	0.97 V
Output offset voltage	V_O = 5 V_{pp}	2 mV
Input bias current	V_O = 5 V_{pp}	±20 µA
dc output resistance	V_O = 5 V_{pp}	2 Ω
Power supply rejection	V_O = 5 Vpp	50 dB

Circuit Description

The Si581 is fabricated with a very high-performance complementary bipolar process which provides high-frequency NPN and PNP transistors with gigahertz transition frequencies (f_T). Power supplies are rated at ±7-V maximum with the data sheet parameters specified at supplies of ±5 V. Figure 1 displays the circuit symbol, and Figure 2 reveals the simplified internal circuit diagram.

The input stage is a complementary pair of differential transistors connected in parallel to provide excellent symmetry, overload recovery, and low noise. At the input, the NPN and PNP transistors have slight mismatches that give rise to the net bias current specification. Depending on the direction of the mismatches, the bias current may flow into or out of the input terminal. The symmetrical class AB output stage provides current sourcing or sinking and relatively constant output impedance during load excursions. The gain and level shift stages provide power supply rejection at low frequencies; they also contribute to the excellent reverse gain and phase characteristics of the buffer.

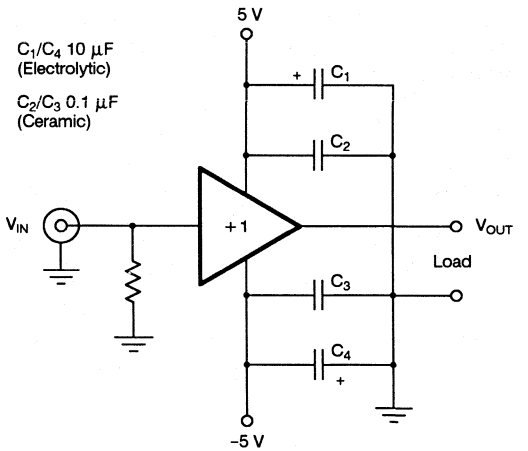


Figure 1. Circuit Symbol of the Si581

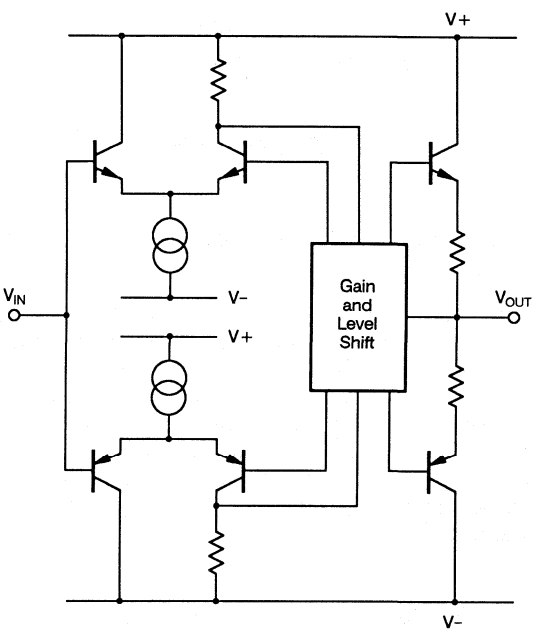
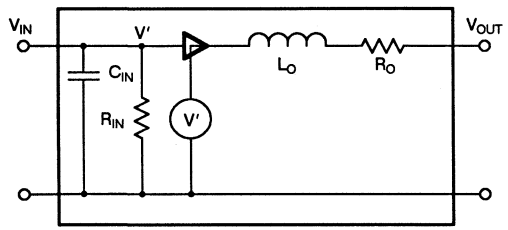


Figure 2. Simplified Internal Circuit Diagram of the Si581

Small-Signal Equivalent Circuit

Equivalent input and output networks to model the small-signal characteristics of the buffer can be obtained from the Si581 data sheet. The model in Figure 3 surrounds an ideal unity-gain buffer with reactive components whose values are obtained from the input and output impedance curves. When the source impedance is known, then a network simulating the effects of the reverse-gain characteristic may be added from input to output.



$$|Z_{IN}| = R_{IN} \sqrt{1 + \omega^2 C^2_{IN} R^2_{IN}}$$

$$\angle Z_{IN} = \text{TAN}^{-1}\, \omega\, C_{IN}\, R_{IN}$$

$$|Z_O| = \sqrt{(R^2_O + \omega\, L^2_O)}$$

$$\angle Z_O = \text{TAN}^{-1}\, \frac{\omega\, L_O}{R_O}$$

At 1 MHz: $Z_{in} = 100\ k\Omega \angle -40°$
$R_{in} = 130.5\ k\Omega$
$C_{in} = 1.02\ pF$

At 100 MHz: $R_O = 1.9\ \Omega$
$L_O = 8.4\ nH$

Figure 3. Small-Signal Equivalent Circuit

Power Supply Decoupling

Figure 1 displays a four-terminal device with input, output, and positive/negative supplies. The ground reference point is located in both of the positive/negative power rails. This location explains the necessity for good power supply decoupling, especially in high-frequency applications. In pulse applications, good power supply decoupling is also important because the output stage cannot dump energy into a load if the power rails are inductive.

The recommended power supply decoupling consists of a 10-µF electrolytic capacitor in parallel with a 10-nF to 100-nF miniature ceramic. Both the electrolytic and the miniature are connected as close as possible to the buffer supply pins. The ground return for the load is the common connection of the decoupling capacitors. Ground plane construction is recommended because it provides a low inductance return for the load.

Forward and Reverse Gain

An ideal buffer has exact unity gain from input to output, irrespective of load. This characteristic is called "forward gain." An ideal buffer also allows a variety of complex (RLC) loads to be driven without modifying the existing input conditions. This characteristic is called "reverse gain." Reverse gain should be zero. Because of the wideband nature of the Si581, forward and reverse gain are specified in S-parameters. S-parameters are reflection and transmission coefficients that are used to describe a linear two-port network in the same way as Y, Z, or h parameters. Short or open circuits are misnomers in RF circuits. Instead, the network is defined in terms of incident and reflected waveforms. Waveforms are easier to measure and the results are more realistic above 50 to 100 MHz.

At 500-mV signal levels, the Si581 forward gain, S_{21}, is −0.2 dB, + 1° at 100 MHz. At the same frequency and amplitude, the reverse gain is −60 dB, +145°. An industry-standard conventional wideband buffer specifies forward gain at approximately −0.5 dB, 0° while reverse gain is specified at only −25 dB, −30° at 100 MHz. This shows that the unique design of the Si581 significantly improves reverse gain.

Applications

Figure 4 shows a wideband crosspoint system for a broadcast video studio switcher or a financial data distribution system. The 8 x 4 wideband crosspoint is formed by four DG538 8-channel multiplexers with their inputs connected in parallel. Each input bus created by the crosspoint represents a considerably reactive load to the input signals. This reactive load would cause unacceptable signal degradation if it were connected directly to the 75-Ω input sources.

The input buffers provide a stable input termination, a low output impedance to drive the input bus, and a high output-to-input isolation. These features enable the input conditions to remain independent of the multiplexer loading.

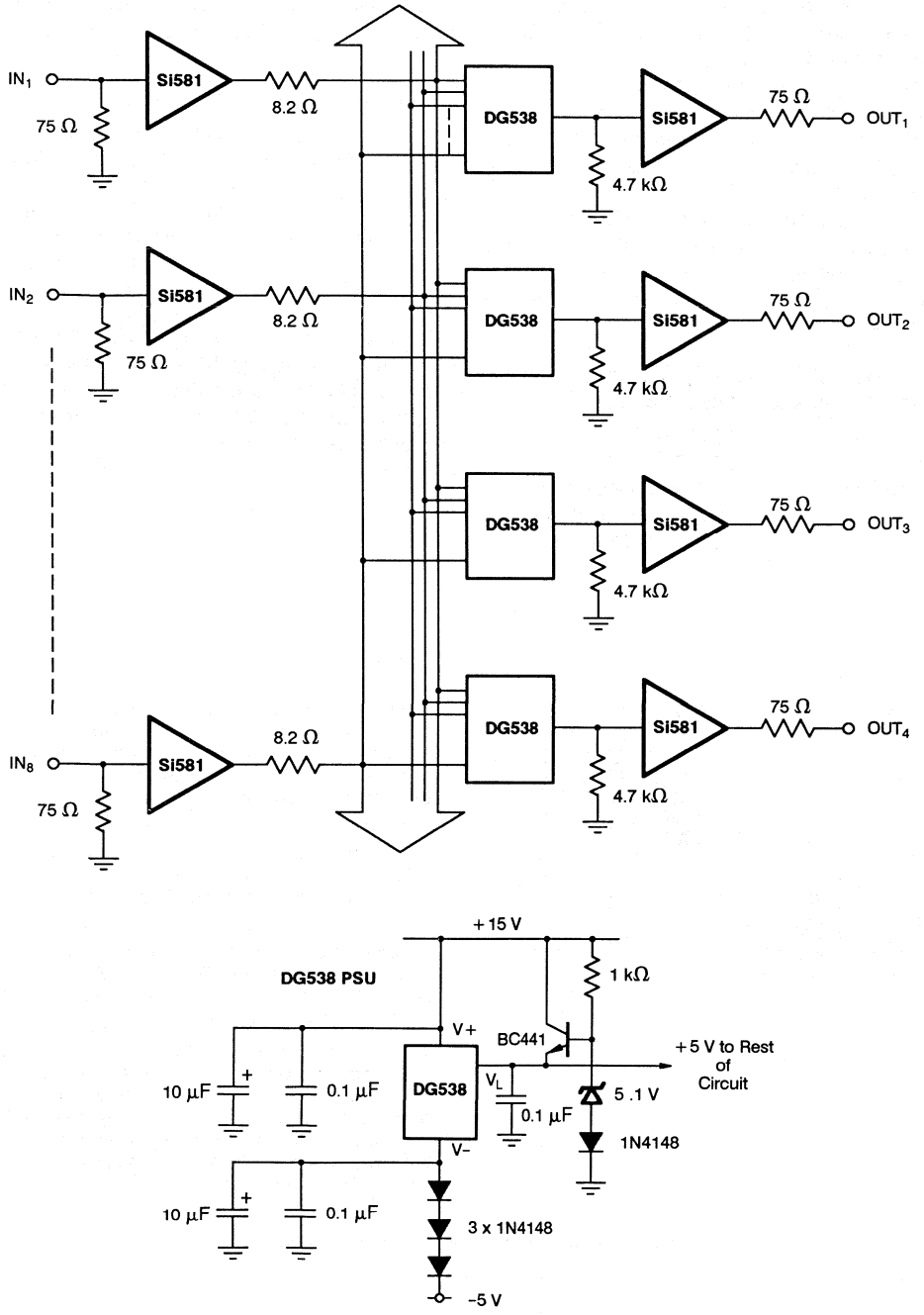


Figure 4. Wideband 8 x 4 Crosspoint Using DG538 Multiplexers and Si581 Buffers

The output buffers provide a "high" input impedance to the multiplexer outputs. This reduces the inevitable transmission loss if the load resistor is 75 Ω. The low output impedance of the buffers allows a single-series resistor in each output to provide reverse termination of 75 Ω. When correctly terminated, this resistor causes a nominal -6 dB loss at the output, but it also isolates any load capacitance from the buffer output terminal. This is important because load capacitance causes amplitude peaking in the passband. The series 8.2-Ω resistor at the input buffers also isolates the switch reactance from the buffer output. Measured performance of this system is shown in Table 3.

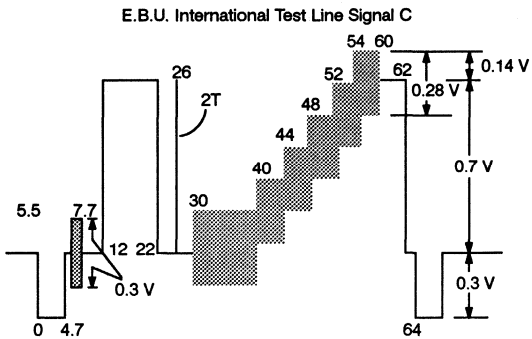
Table 3. Wideband 8 x 4 Crosspoint Using DG538 Multiplexers and SI581 Buffers

-3 dB Bandwidth	145 MHz
-0.3 dB Bandwidth	50 MHz
Phase Shift to 100 MHz	0 to -97°, Linear Slope
Differential Gain	-0.03% EBU Test Signal
Differential Phase	-0.03° EBU Test Signal

To prevent the 6-dB loss at the output, a wideband amplifier, such as the Si582, configured for a gain of 2 may be used.

Performance depends significantly upon high-frequency ground plane techniques, symmetrical layout, and the correct use of the series isolating resistor. Where different capacitive loads are encountered (i.e., an 8 x 2 crosspoint employing just two DG538 multiplexers), the curve in Figure 6 will assist in selecting the correct isolating resistor. As with all high-frequency work, resistors should be noninductive.

In a design similar to Figure 4, the Si581 may be used with the DG54X family of wideband switches to perform IF and or bandwidth switching in numerous receiver applications such as HF communications equipment and multistandard TV chassis.



a. Standard Test Waveform

DEFINITIONS

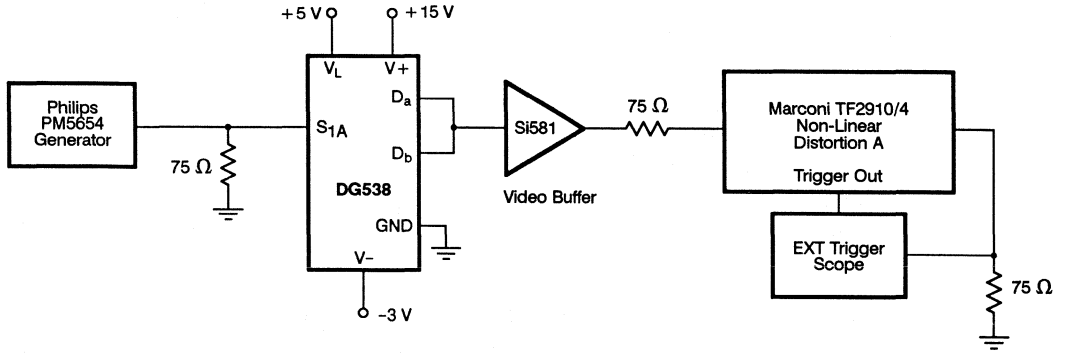
Differential Phase: Measured in degrees, this is the phase shift of the color subcarrier resulting from a change in the amplitude of the associated luminance components. Differential phase shows up in NTSC pictures as a change in hue, a color change more noticeable in a shaded area of the picture.

Frequency related phase shifts (as opposed to differential phase) will cause no change in picture quality since both color burst and chrominance are equally shifted.

Differential Gain: Expressed as a percentage, this is a form of distortion resulting from changes in the amplitude of the chrominance signal as a function of luminance amplitude.

The effect on NTSC and PAL pictures is a change in color saturation with changing luminance level. The eye is fairly tolerant to differential gain since the resulting picture changes are fairly subtle. For instance, a brightly colored car travelling from a sunny area of the picture to a shaded area would appear as though its body color intensity had suddenly changed.

Figure 5. Video Waveforms and Specification Definitions



b. Differential Phase and Gain Test Configuration

Figure 5. (Cont'd) Video Waveforms and Specificatio Definitions

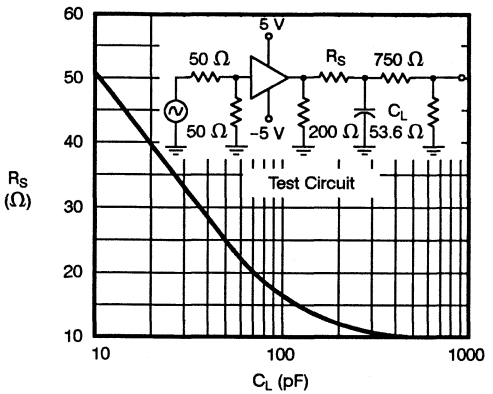


Figure 6. Series Isolating Resistor and C_{LOAD} Selection.

Feeding several cables from one high-impedance wideband signal source can be done with the circuit shown in Figure 7. For optimum broadcast video performance (< 0.1% differential gain, < 0.05° differential phase, EBU), the Si581 should be restricted to driving two reverse-terminated 75-Ω loads. This would give a nominal 75-Ω total output loading. For more outputs, several buffers may be driven from a simple JFET dual-source follower as shown in Figure 7.

The input stage is a compound source follower. It uses a matched pair of JFETs and equal value source resistors to reduce the input-to-output offset from several volts without correction to approximately 40 mV. The output impedance of the input stage is $1/g_{fs} + R_s$; this impedance drives the inputs of the paralleled Si581 buffers. The total input to output offset includes the Si581 buffers. For low-impedance signal sources (50 Ω, 75 Ω), the JFET stage is not necessary. The circuit in Figure 8 is useful when precision offsets are required.

To vary both the current in Q_1 and the voltage across the 33-Ω resistor, Q_2 is added to the input source follower. Q_2 is controlled by the chopper stabilized op amp, the Si7652, which is configured as an inverting integrator. The Si7652 drives Q_2; this varies the current in Q_1 and drives the input-to-output offset to zero. Multiple Si581 buffers can be included in this scheme, but the offset will be the net average of all the offsets as they are summed by the Si7652 input. Variations of the above method, with or without offset correction, make excellent wideband antenna amplifiers. This is due to the square law JFET transfer characteristic and the > 30-dBm third-order intercept performance of the Si581.

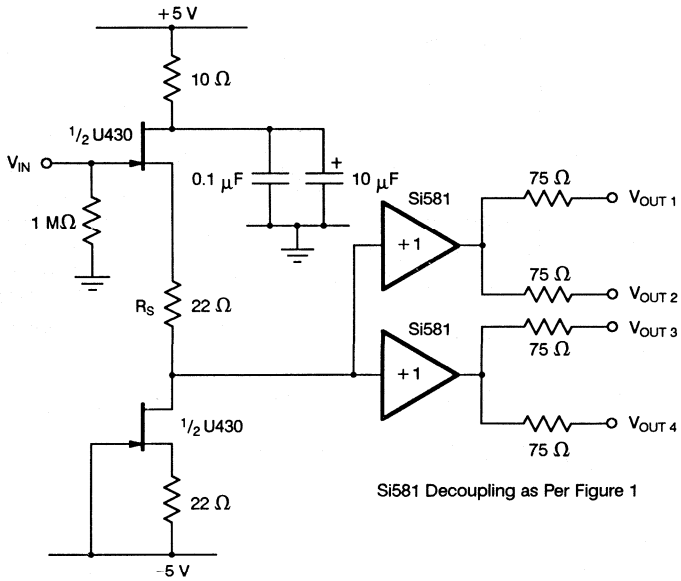


Figure 7. Multiple-Output High-Performance Buffer

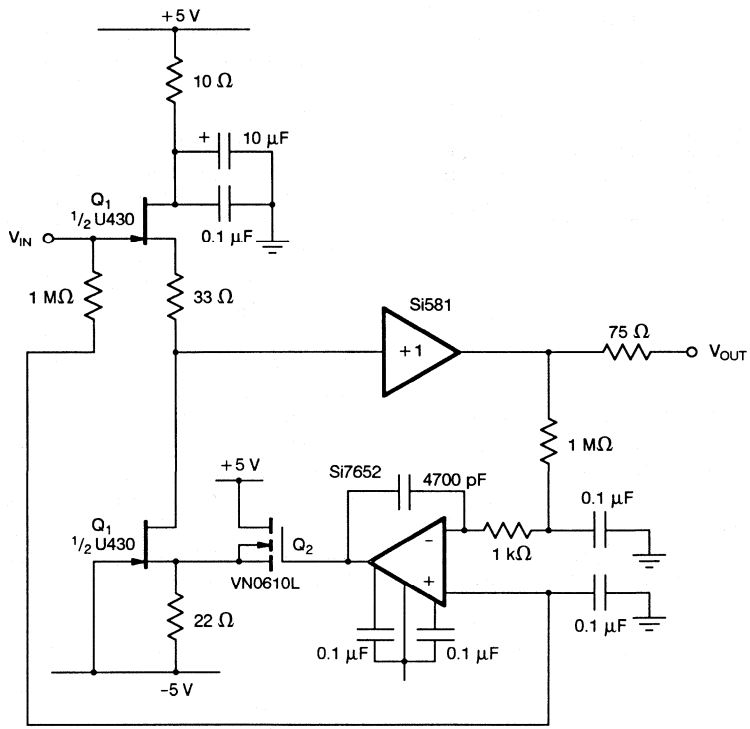


Figure 8. Precision High-Performance Buffer

Single-SupplyOperation

The buffer may be powered from a single 10-V supply without special precautions. A typical application is shown in Figure 9. The input is biased to mid-operating point (5 V here) and is ac coupled. The value of R_2 and R_3 is chosen with the limits of the input bias current in mind. Thus, 27 kΩ is a suitable value that leads to an input impedance of 13.5 kΩ (R_2 in parallel with R_3) at low frequencies. Note that for dc loads referenced to ground, the quiescent current is increased by the input bias voltage/R_L. The test waveform used to obtain the results is shown in Figure 5.

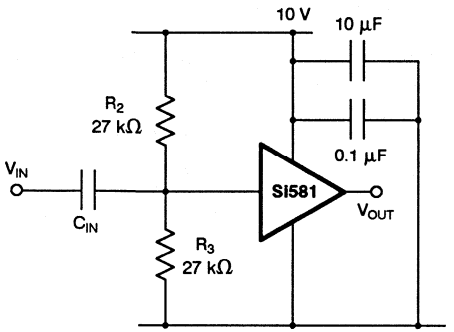


Figure 9. Single-Supply Operation

Cable Shield Driver

To reduce the effective load capacitance seen by the cable driver, the Si581 may be used to drive the outer shield of an unterminated coaxial cable. This is useful in situations when the bandwidth requires very low effective load capacitance and reverse termination cannot be employed because of the transmission loss. Figure 10 shows a typical arrangement where one buffer is the main cable driver and another buffer drives the cable outer shield. In this situation, the cable capacitance seen by IC_1 is bootstrapped by IC_2. This permits high-speed data transmission by IC_1.

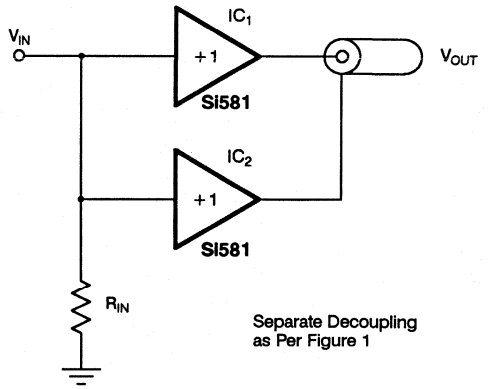


Figure 10. Cable Shield Driver

References

Powell, Gareth, "Microprocessor-Compatible Multiplexers Facilitate Video Switching Designs," Siliconix Applications Note AN88-2.

Carson, Ralph S, "High-Frequency Amplifiers," John Wiley and Sons, 1982.

SERIALLY-CONTROLLED EIGHT-CHANNEL ANALOG SWITCH ARRAY SIMPLIFIES SIGNAL CONDITIONING AND ROUTING

Steve Moore

When analog signals are processed in a digital system, some of the processing must be performed in the analog domain, both before and after the digital portion of the system. CMOS analog switches are frequently used in a variety of analog signal conditioning functions under digital control, such as gain ranging, anti-aliasing filter corner-frequency selection, sample-and-hold functions, input channel selection, input summing, and signal routing.

A new serially-controlled array of precision CMOS switches simplifies the design of these functions, while improving system accuracy and reducing component count and board space. This application note presents simplified solutions for some of these digitally controlled analog signal processing circuits using the new DG485 eight-channel serially-controlled switch array.

The DG485 Switch Array

CMOS analog switches typically come in single, dual, and quad configurations. CMOS multiplexers combine up to sixteen switches on a chip, with decoding logic that allows the selection of one switch at a time. Now there is a new function that combines the best of both types of devices. The DG485 has eight switches on a chip, and through a unique serial data control architecture, any combination of the eight switches can be connected to a common output line.

A New Way to Control a Switch Array

The internal block diagram for the DG485 is shown in Figure 1. It consists of five elements: (1) the logic input stages, (2) an array of eight D-type flip-flops that form an input shift register, (3) an array of eight data latches, (4) eight switch drivers, and (5) eight CMOS analog switches. There are three power supply inputs and a ground. The three supplies are V+, V–, and V_L. V+ and V– set the analog range for the signals being controlled by the switches. The range of operation for V+ and V– is ±5 V to ±20 V and also includes single-supply operation by connecting V– to ground. The V_L input determines the logic switching threshold recognized by the logic input buffer stages. The nominal operating value for V_L should be 5 V to allow for TTL-compatible operation ($V_{INL} \leq 0.8$, $V_{INH} \geq 2.4$ V). However, V_L can be operated anywhere from 5 to 40 V to facilitate compatibility with a wide range of logic levels. The GND, although being the only ground point on the device, is generally considered to be a digital ground, rather than an analog ground, for the purpose of avoiding ground loops.

A simplified schematic of a typical DG485 channel which details its five elements is shown in Figure 2.

The input buffer stages (1) are CMOS inverters which have ESD protection consisting of catch diodes and a resistor to dissipate the energy generated by electrostatic discharge, which can destroy an MOS input. The scheme used in the DG485 provides protection in excess of ±4000 V on all pins of the device. (This protection is required only on the logic inputs because the power supply and output connections have built-in protection via the large parasitic p-n junctions.) The TTL input buffers are CMOS inverter stages that swing between V_L and GND, and drive a level shift stage to drive the D-type master-slave flip flops (2) that swing from V+ to GND. The D-type flip-flops have master-slave inverters with edge-sensitive clocking, and they form the data input shift register. Their outputs are connected to the address register latches (3), which are single-stage clocked-inverter flip-flops with level-sensitive clocking. These latches, in turn, are connected to the switch drivers (4), which provide level translation from the latch outputs, which swing between V+ and GND, to the gates of the CMOS switches (5), which must swing from rail to rail. These switches are pairs of large p-channel MOSFETs in parallel with complementary n-channel MOSFETs; this parallel combination has a low ON-resistance of 85 Ω: (maximum at 25°C). The p-channel device is turned on by driving its gate to the V– rail, and it is turned off by driving its gate to the V+ rail. In an opposite manner, the n-channel device is turned on by driving its gate to V+ and turned off by driving its gate to V–. These parallel switches compensate for each other's increase in

ON-resistance as the analog signal approaches either rail. That is, as the V_{GS} for one device goes to zero, it shuts off, while the opposite polarity device is fully enhanced or turned on hard. The result is a fairly flat ON-resistance as the analog voltage of the source (or drain) ranges from V+ to V−. Typically, a ±8 Ω variation is seen.

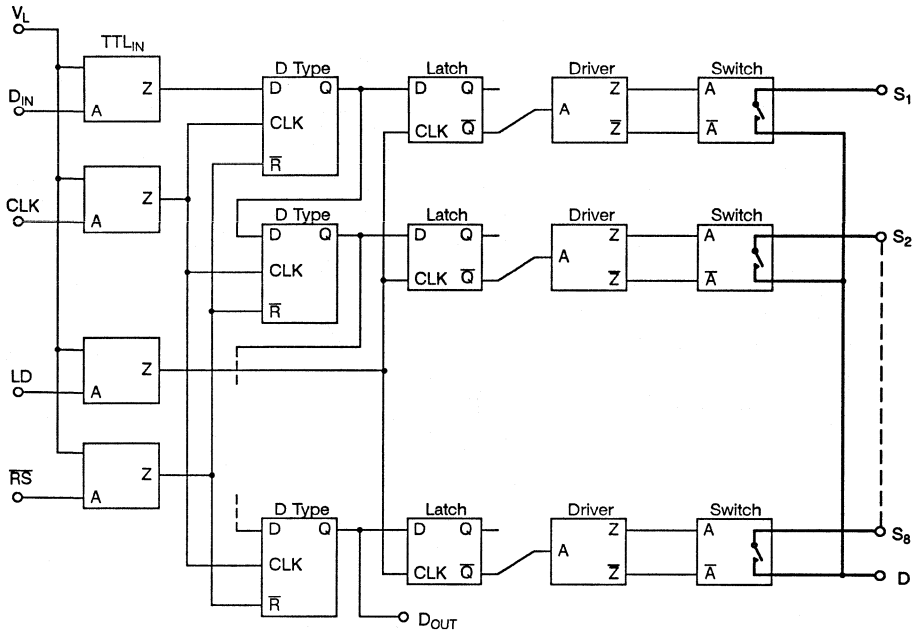


Figure 1. The DG485 Internal Block Diagram

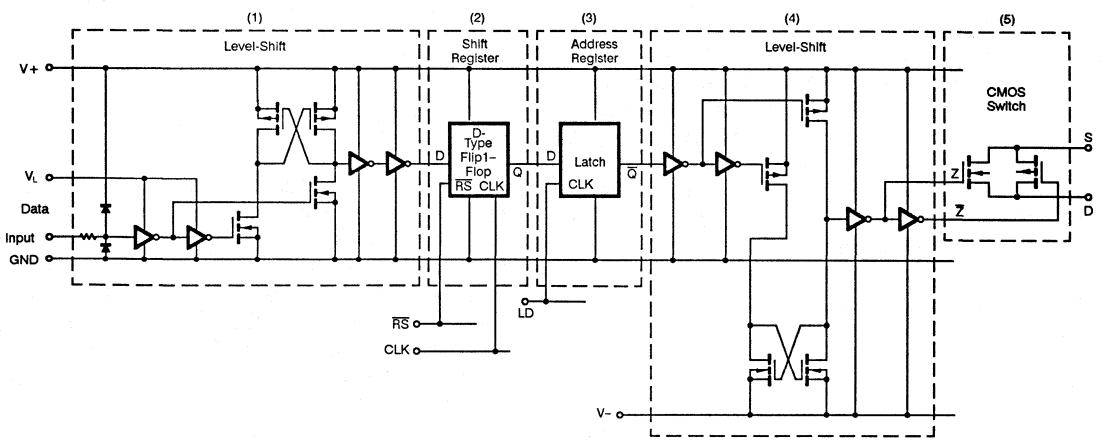


Figure 2. Simplified Schematic of a Typical DG485 Channel.

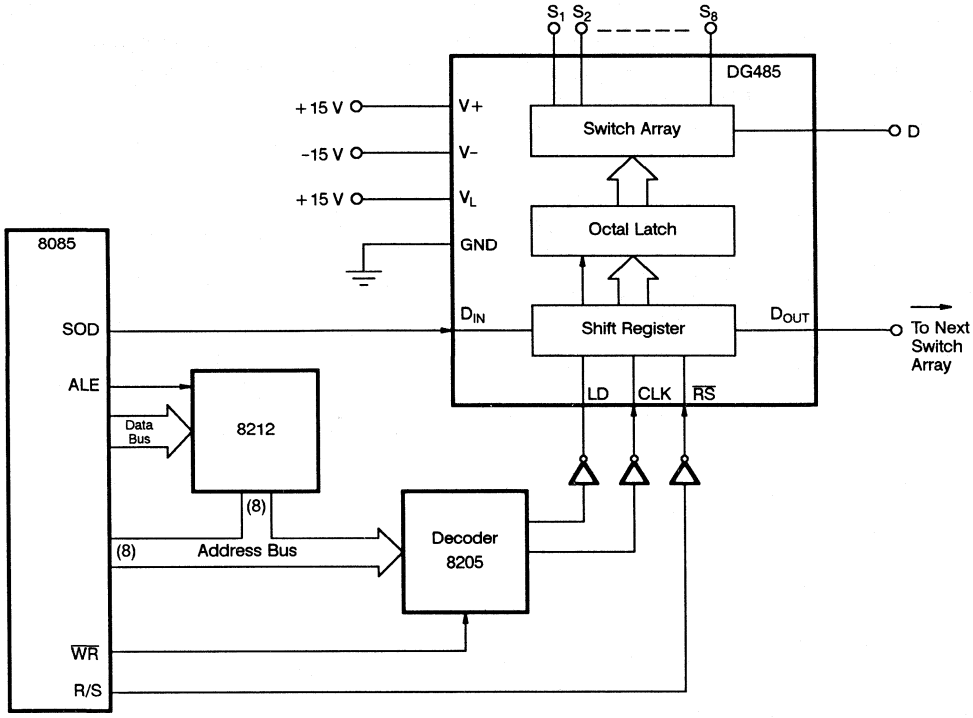


Figure 3. The DG485 simplifies analog signal control with a serial data bus. The input shift register in the DG485 receives switch on/off-state data directly from the serial data (SOD) line from the microprocessor.

Controlling the Array with a Serial Data Bus

The DG485 connects to the serial output of a microprocessor system, as shown in Figure 3. The eight CMOS switches in the DG485 are controlled via the serial data output via the D_{IN} (data in) pin. Data is loaded into the eight-bit shift register with each clock pulse at the CLK (clock) input. The contents of the shift register are loaded into the octal latch when a logic "high" signal is applied to the LD (load) input. The octal latch holds the state (on or off) of the individual switches in the array. The $\overline{RS}$ (reset) input resets the octal latch to all "zeroes" when a logic "low" is applied, turning all switches off with a subsequent LD command.

Analog-Signal Voltage Ranges

The power supplies for the device are V+, V–, and V_L. The analog signal range of the switches is defined by the power supply rails. Because the DG485 is built on a 44 V silicon-gate CMOS process, rail-to-rail signal swings are possible. The power supply voltages range from ±5 V to ±20 V, and single-supply operation is allowed from +5 V to +40 V. The logic levels are set with V_L input. With 5 V applied to V_L, TTL and 5 V CMOS logic compatibility (V_{INL} = 0.8 V, V_{INH} = 2.4 V) is assured.

Switch Array with Improved Speed and Accuracy

In addition to being a useful new function, the DG485 features analog switches with vastly improved performance. They are part of the DG400 family which uses a new silicon-gate CMOS process designed to achieve improved speed, lower power, lower ON-resistance, lower leakage, and improved ESD tolerance. These benefits are the result of the inherent reduced overlap parasitic capacitance of silicon-gate CMOS processing.

For comparison of switch performance, key specifications for the industry-standard DG508A eight-channel multiplexer and the DG485 eight-channel array are shown in Table 1.

The closest standard IC to the DG485 is the eight-channel DG508A multiplexer. While the DG485 array allows any combination of eight switches to be turned on at one time (compared with the one-of-eight decoding of the multiplexer), it also has improved speed and accuracy with reduced power dissipation. Key specifications for the DG485 array and the DG508A multiplexer are compared below.

Table 1.

Key Specification (@ 25°C)	DG508A 8-Channel Multiplexer	DG485 8-Channel Array
Fabrication Process	44 V Metal-Gate CMOS	44 V Silicon-Gate CMOS
ON-resistance ($r_{DS(ON)}$ Max.)	450 Ω	85 Ω
Leakage ($I_{S(off)}$ Max.)	5 nA	1 nA
Switching Time ($t_{(tran)}$ Max.)	1 µs (1000 ns)	200 ns
Power Dissipation (PD Max.)	59 mW (59000 µW)	105 µW
ESD Tolerance	500 V	4000 V

Digitally Controlled Signal Conditioning

Input signal conditioning functions like gain ranging, programmable attenuation, and variable filter time constant circuits have one thing in common -- they use analog switches for selecting various resistor values. There are many ways to create digitally controlled gain stages using CMOS switches.

Using the DG485, as shown in Figure 4a, places the analog switch in series with a high-impedance point, such as the input of an op amp, to eliminate errors associated with switch ON-resistance. Additionally, the gain value is determined by the ratio of the gain-setting resistors rather than their absolute value. Thus, the accuracy of the gain setting is a function of the matching or scaling of the resistors, independent of resistor or analog switch variations. If matched or monolithic resistor arrays are used, excellent gain accuracy and low gain drift is achieved with this architecture. The DG485 allows for selection of eight different resistor ratios under serial control, and its any-combination-of-eight architecture also allows 255 different parallel combinations of resistor ratios for additional gain ranges.

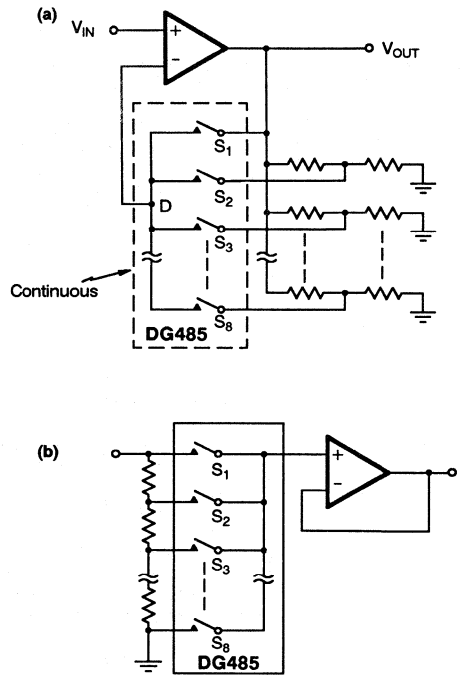
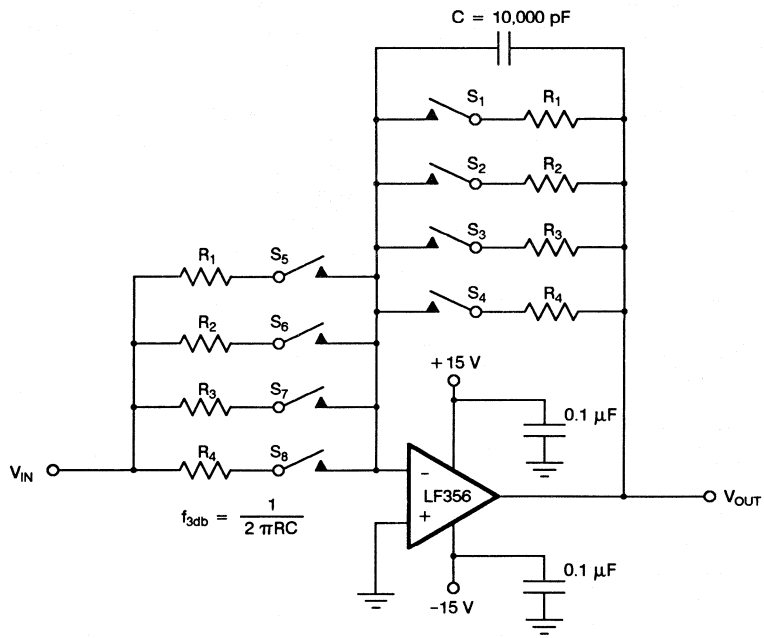


Figure 4. Gain Ranging and Attenuator Circuits

A variation on this theme, shown in Figure 4b, provides programmable attenuation. Again, the analog switches are placed in series with a high-impedance point (the op amp input) to eliminate the effect of switch resistance variations. Attenuation values are selected according to the ratio of the resistors in the string.



	CODE TO SHIFT REGISTER								
	1	2	3	4	5	6	7	8	f_{3db}
R_1 = 1.6 kΩ	1	0	0	0	1	0	0	0	10 kHz
R_2 = 800 Ω	0	1	0	0	0	1	0	0	20 kHz
R_3 = 530 Ω	0	0	1	0	0	0	1	0	30 kHz
R_4 = 400 Ω	0	0	0	1	0	0	0	1	40 kHz

Figure 5. Programmable Low Pass Filter

Digitally Controlled Filter

The programmable filter circuit shown in Figure 5 selects resistors rather than capacitors to change the RC time constant of the low pass. This is a useful function at the input of a data acquisition or digital signal processing system which allows the processor to adjust the corner frequency of its anti-aliasing filter if various sample rates are being used. Only one capacitor is required, and resistors (which are generally low in cost and easier to specify for accuracy and ratios) are selected with the DG485 to generate different filter characteristics. Resistors that are matched to the ones in the feedback loop are switched at the input of the integrator to maintain unity passband gain for any of the four corner frequencies selected.

In this filter topology, unlike the gain-ranging circuit shown above, the analog switches are placed in series with the time-constant setting resistors. Therefore, the resistance characteristics of the switches play a significant role in the accuracy of the time constant selection. Switches with low ON-resistance are preferred since the time constant of the filter is

$$(r_{DS(ON)} + R_f) \times C$$

If R_f is large, compared to the 85 Ω ON-resistance of the DG485, accurate filter break frequencies may be selected via digital serial control. R_{IN} is chosen according to the dc gain requirement of the system. For example, dc unity gain inversion is achieved with $R_{IN} = R_f$. The break frequency, f_{3dB}, is calculated as

$$f_{3dB} = \frac{1}{2\pi RC}$$

The actual measured -3 dB frequencies may vary as much as 10% due to the parasitic drain and source capacitance of the DG485 switches and the variation in ON-resistance seen from channel to channel.

Because any combination of the eight switches can be selected, there are a total of sixteen different RC values that can be programmed by using parallel resistor combinations for a wide range of filter roll-offs.

Switching, Selecting, & Summing Multiple Inputs

Frequently a system will process signals from multiple inputs. Time division multiplexing takes samples of each input in successive time intervals. The traditional approach is a multiplexer followed by a sample-and-hold circuit. The DG485 simplifies this function while allowing faster data throughput and higher precision. The channel selection is accomplished with a serial data line, eliminating the latches that are required with a multiplexer, such as the DG508A, when interfacing with the data bus. In addition, the sample-and-hold function is covered by the DG485 with a hold capacitor. The reduced ON-resistance and faster transition time of the DG485 allows faster sample acquisition, and the low leakage reduces droop rate.

The Summing-Node Mixer

An eight-channel summing amplifier processes eight inputs in a different way. Like the time-division multiplexer, it selects eight inputs, but rather than sampling each input, it adds the inputs to one another. A classic example is the audio mixer, which sums many audio inputs at the summing node of an op amp to a single output (see Figure 6). For precision, low-noise systems, it is important that the switch resistance remain low because the switches are placed directly in series with the summing resistors and, hence, the analog switches become a factor in the gain and nonlinearity (which results in distortion) of the system. The any-combination-of-eight function of the DG485 allows summing, where the conventional multiplexer function only allows selection of one at a time. In addition, the reduced ON-resistance of the DG485 allows a factor of six reduction in the values of the summing resistors, thus reducing noise. The serial control line vastly simplifies addressing in larger mixers. A 24-channel mixer is easily configured without additional address lines using the D_{OUT} (serial data output) feature of the DG485 to daisy-chain the switch arrays (see Figure 6).

The summing-node mixer is a variation of the basic inverting amplifier. If you consider only one channel of the circuit and assume R_{IN} and $R_f >> r_{DS(on)}$ of the DG485 (85 Ω), then the transfer expression is

$$V_{OUT} = -(R_f/R_{IN}) \times V_{IN}$$

or

$$V_{OUT} = -V_{IN} \quad \text{when } R_f = R_{IN}$$

If improved gain accuracy or low values of R_f and R_{IN} are required, the effect of $r_{DS(on)}$ cannot be ignored. The expression becomes

$$V_{OUT} = -[R_f/(R_{IN} + r_{DS(ON)}] \times V_{IN}$$

Placing a dummy "on" switch from the DG485 into the feedback loop in series with R_f will provide an $r_{DS(ON)}$ term in the numerator of the expression.

$$V_{OUT} = \frac{-[R_f + r_{DS(ON)}]}{R_{IN} + r_{DS(ON)}} \times V_{IN}$$

or for $R_f = R_{IN}$

$$V_{OUT} = -V_{IN}$$

When all channels are included, super position gives

$$V_{OUT} = -(V_1 + V_2 + \ldots. V_n)$$

for n inputs.

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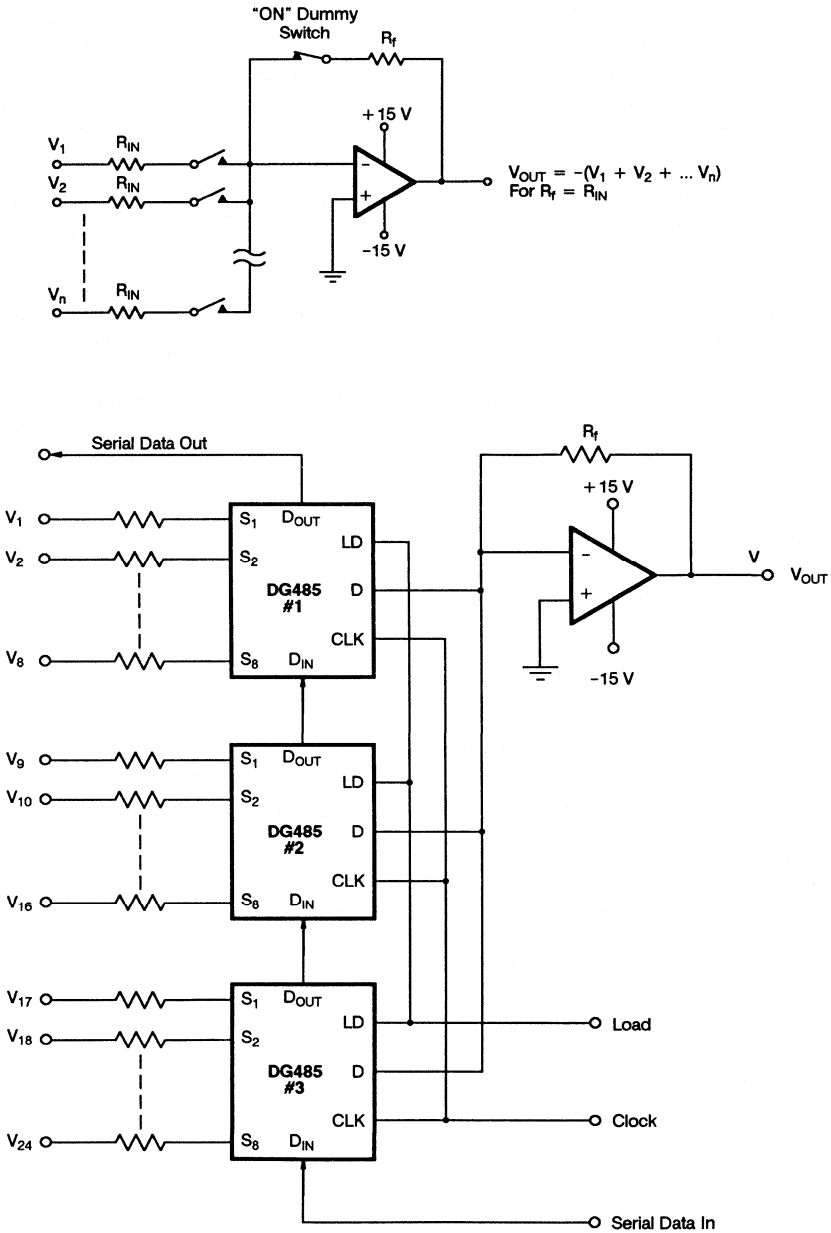

Figure 6. The summing-node mixer is frequently used in audio production consoles. Inputs are switched on and off with the summing node of the DG485.

Crosspoint Arrays

An audio crosspoint array provides interconnection between many inputs and many outputs. The serial data addressing feature of the DG485 simplifies the control of a high-quality audio-frequency crosspoint array, such as the one shown in Figure 7. This eight-input, four-output crosspoint uses four DG485s. Cross connection is directly controlled by a 32-bit serial-control word by taking advantage of the DG485's serial-data output pin. By daisy-chaining the switch arrays, the control data is sent through an effective 32-bit shift register, the contents of which are latched into the 32-bit address register on a LD command which is common to all four DG485s. The CLK and $\overline{RS}$ functions are also shared by all four chips.

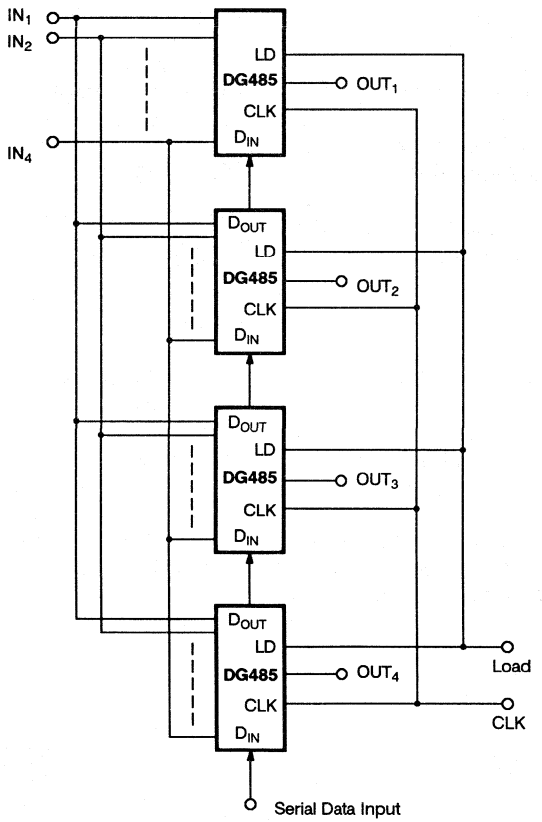

Figure 7. An Eight-by-Four Audio Crossspoint

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SILICON-GATE SWITCHING FUNCTIONS OPTIMIZE DATA ACQUISITION FRONT ENDS

Jack Armijos and Kevin Smith

The trend in data acquisition is moving toward ever-increasing accuracy. Twelve-bit resolution is now the norm, and sixteen bits are not uncommon. Along with this precision, throughput is also very important. When monitoring several hundred channels, sample rates in the hundreds of kilohertz are not only desirable but, in many cases, mandatory.

Analog switches and analog multiplexers find extensive use at the heart of most data acquisition and process control systems. This application note provides useful information about the new high-performance DG400 family of devices. It also reviews many design considerations that will enable you to get the best performance in your data acquisition designs.

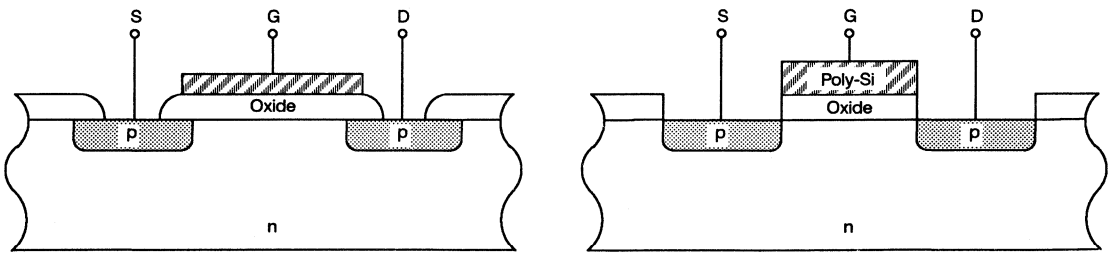
Silicon-Gate Technology

Siliconix's advanced high-voltage silicon-gate CMOS processing brings many benefits to the DG400 family of analog switches and multiplexers: fast switching speed, low power consumption, low charge injection, low leakage, and TTL compatibility. In addition, this family works with reduced or single power supplies.

The metal-gate process (Figure 1) requires that the gate overlap with the drain and source areas to assure reliable operation even when misalignments occur during masking operations. This produces high gate-drain and gate-source capacitances. The silicon-gate process, on the other hand, is self-aligning in that it uses the silicon gate itself as a mask for source and drain diffusions. This produces minimal overlap, resulting in much smaller parasitic capacitances. Because the silicon-gate process is more tightly controlled than the older metal-gate technologies, individual devices can be spaced closer together, resulting in smaller die that achieve equivalent performance.

ESD Tolerance

Electrostatic discharge (ESD) has caused many CMOS device failures, both during manufacture and during handling or PC board assembly. Historically, CMOS devices have shown an electrostatic discharge sensitivity (ESDS) in the ±500 Volt range, which was insufficient in many cases. However, the DG400 family incorporates specially designed ESD protection. These devices have been evaluated using the electrostatic discharge sensitivity (ESDS) test circuit of MIL-STD-883C, Method 3015.3 (100-pF capacitor discharged through a 1.5-kΩ resistor). Results showed that the DG400 through DG405 have tolerances of more than ±2,000 V, whereas the DG408 through DG419 withstand > ±4,000 V on all pins. This qualifies them for a MIL-STD-883C Class 3 rating.



a) Metal-Gate MOSFET

b) Silicon-Gate "Self-Aligned' MOSFET

Figure 1. Comparison of Metal and Silicon-Gate Structures

Typical Data Acquisition System

Figure 2 shows the block diagram of a typical data acquisition system. Analog inputs are converted to a digital format that allows a computer to gather, monitor, display, and analyze the collected data. If the system has digital output capabilities, the computer can be used to accurately control your process so it will run at maximum efficiency. For example, it can react to the input data to maintain a constant temperature, to control flow rates in accordance to a predetermined schedule, etc.

This system accepts analog voltage inputs that can come from temperature sensors, pressure transducers, flow meters, or from optional signal conditioners or remote current-mode transmitters. The signal conditioning stages can perform preamplification, scaling, and multiplexing, and can also provide galvanic isolation or overvoltage protection. The analog multiplexer is basically a monolithic array of analog switches with on-chip address decode logic. The multiplexer is a cost-effective solution that shares the more expensive sample-and-hold (S/H) and analog-to-digital converter (ADC) functions among several inputs. The programmable-gain amplifier's (PGA) purpose is to amplify low-level signals to increase measurement resolution and accuracy. The S/H circuit quickly captures a sample of the analog input signal and holds its instantaneous value for a time that is long enough to allow for the ADC acquisition time to be completed.

Operation of the analog front end is governed by means of a digital controller which, in turn, interfaces to a host computer or microprocessor. Digital event inputs or interrupts go directly to the controller, and its digital outputs provide the feedback necessary to perform automatic process control. In addition to the analog multiplexer, analog switches are found in the PGA, S/H, and ADC circuits. The following paragraphs will review many design considerations as we proceed to the design and evaluation of an experimental data acquisition system front end.

Designing an Experimental Temperature Monitoring System

The purpose of our experimental circuit is to evaluate some of the errors introduced while monitoring temperature via three popular types of transducers: a two-terminal integrated circuit, a resistive temperature detector (RTD), and a type J thermocouple. In addition, we want to sample ground and a +5 Volt reference voltage. These two quantities may be used for calibration and error correction purposes. Signals from the sensors will arrive at the PC board via twisted pair wires to help eliminate any common-mode noise. No cold-junction compensation of the thermocouple will be attempted since compensation circuits are readily available. The schematic diagram is shown in Figure 3.

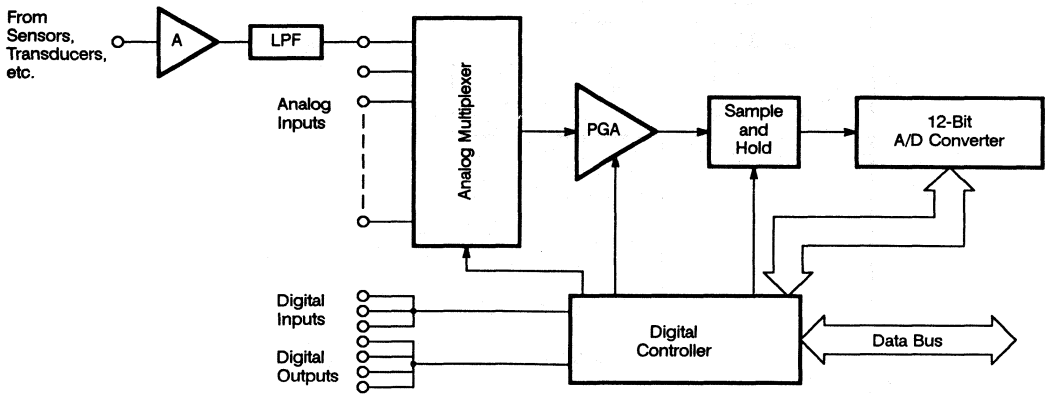


Figure 2. A Typical Data Acquisition System

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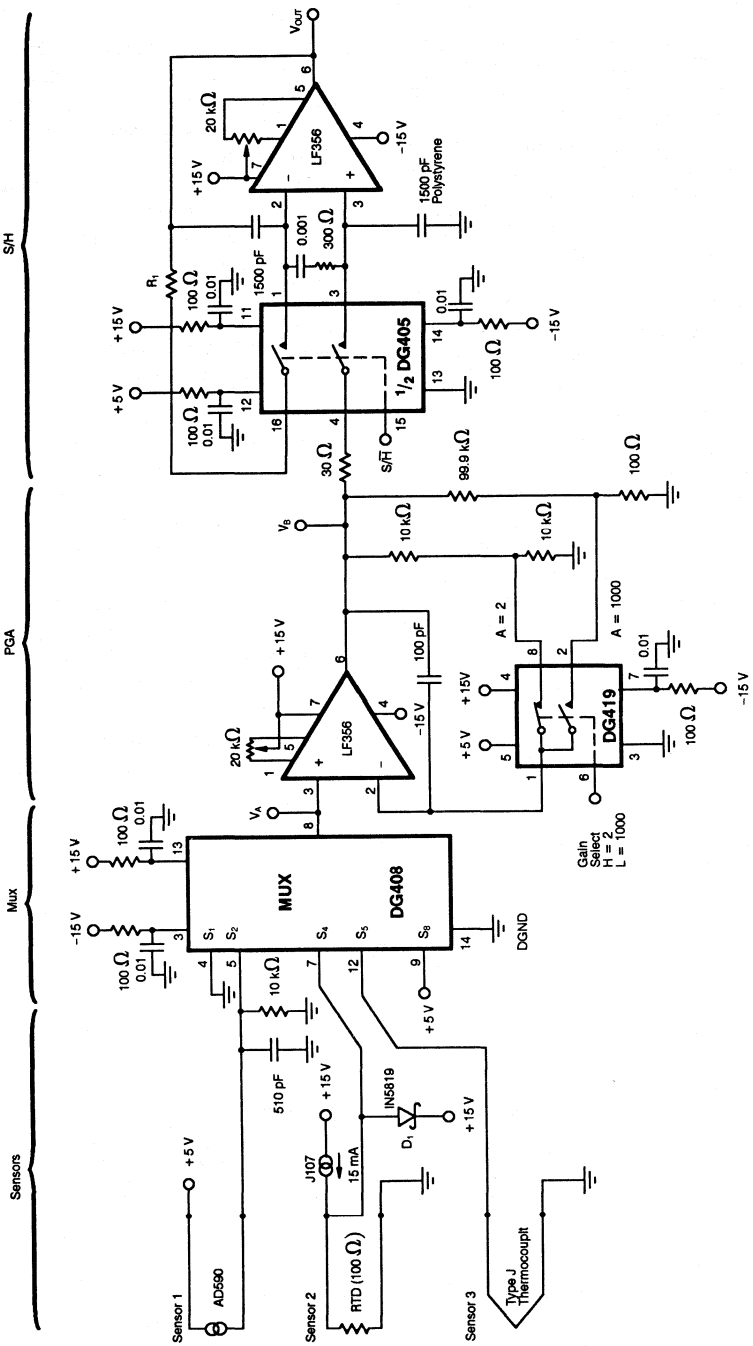

Figure 3. Temperature Monitoring Circuit

The Multiplexer

The DG408 is an 8-channel single-ended multiplexer with an on-chip logic reference that maintains TTL compatibility over a wide range of power supply voltages. Its low ON-resistance and low leakage (see Figure 4) minimize static errors. The worst-case error due to leakage is given by

$$V_e \text{ max} \approx 40\ \Omega \times 100\ \text{pA} \approx 4\ \text{nV}$$

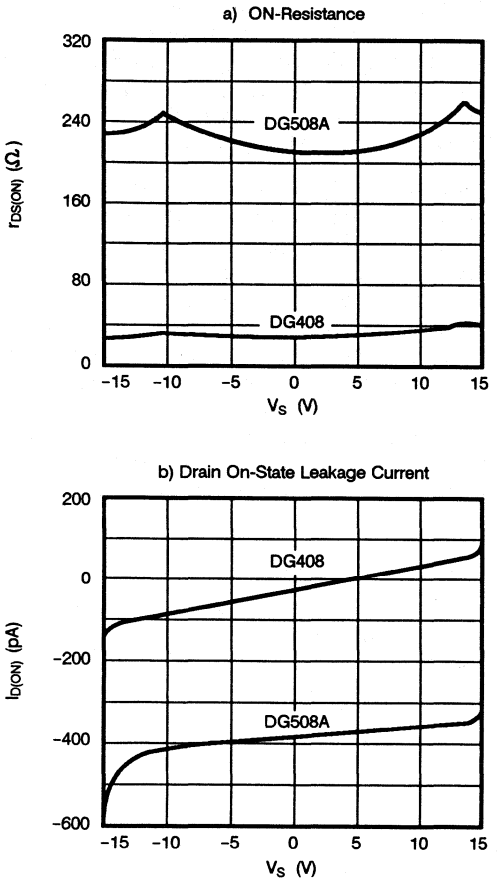

Figure 4. DG408 Typical Characteristics

Figure 5 shows a thermocouple representation of one switch in the multiplexer. If connections J_{1S} and J_{1D} are at the same temperature, their thermoelectric EMFs will cancel out. If a temperature gradient exists between side "S" and side "D," the voltages will not exactly cancel, and a net error voltage will result. Therefore, the multiplexer should be mounted in a thermally stable environment -- that is, soldered to the PC board and away from hot components and air drafts. The DG408, thanks to its low power dissipation (~1 mW), develops less than ± 1 μV in still air at room temperature. When heated to 85°C with a thermal probe, the error becomes as large as 100 μV. ON-resistance ($r_{DS(ON)}$) matching is necessary when the $r_{DS(ON)}$ of the multiplexer is significant when compared to the rest of the circuit, such as when using differential multiplexing or when the transducer is connected in a resistive bridge configuration. Having smaller $r_{DS(ON)}$, the DG408 offers also an "$r_{DS(ON)}$ matching" specification which is three times better than the DG508 in terms of the magnitude of resistance.

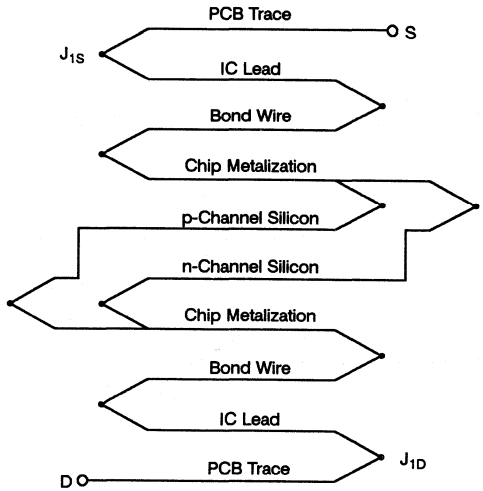

Figure 5. Thermocouple Representation of a CMOS Multiplexer Switch

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The Programmable Gain Amplifier

There are several types of gain-ranging circuits. Although it would be impossible to cover them all here, Figure 6 shows two of the most common types. Each of these types has advantages and disadvantages.

Figure 6a shows a circuit which uses three resistors and two switches. By closing one switch at a time, two different gains can be selected. By closing more than one switch at a time, three gain combinations are possible.

The circuit in Figure 6b uses four resistors to achieve the same two gain values as the previous example.

In comparing the two circuits, it would seem that the first circuit is the better of the two since it requires fewer resistors. Upon closer examination, however, we find that there's more to consider. In Figure 6a, the analog switch is in series with the feedback resistor. This means that the $r_{DS(ON)}$ of the switch is part of the feedback ratio. Instead of the gain being

$$A_V = -R_f/R_1,$$

it becomes

$$A_V = -(R_f + r_{DS(ON)})/R_1$$

While the lower ON-resistance and lower $\Delta r_{DS(ON)}$ of the DG400 family of switches do offer advantages over older metal-gate switches, in this situation, it would be better still if we could eliminate the effect of the switch $r_{DS(ON)}$ altogether. This is where the circuit shown in Figure 6b has an advantage.

As shown in Figure 6b, the gain in each stage is determined by the two resistors in that branch. For the gain of 10, for example, the gain is

$$A_V = (R_{f1} = R_{g1})/R_{g1} = (18 + 2)/2 = 10$$

The $r_{DS(ON)}$ of the switch has no affect at all on the gain! However, the switch leakage current may affect the circuit accuracy. Here, again, the DG400 family of switches have an advantage because their leakage current is much lower than the metal-gate switches. By choosing precision resistors or resistor networks, it is possible to have gains accurate to the 12-bit level.

The output voltages of the AD590 and RTD in Figure 3 are greater than 1 V in the temperature range used. The thermocouple, however, had an output voltage that varied from a few microvolts to several millivolts. Therefore, two different gains are required from the PGA: a relatively low gain of two for the AD590 and RTD, and a gain of 1,000 for the thermocouple. This allows the voltages to the sample-and-hold to be large enough that any errors contributed by the circuit would have minimal effect. The DG419 used to select the gain is a very low-power, high-speed switch. An additional benefit of this particular switch is its compact 8-pin package.

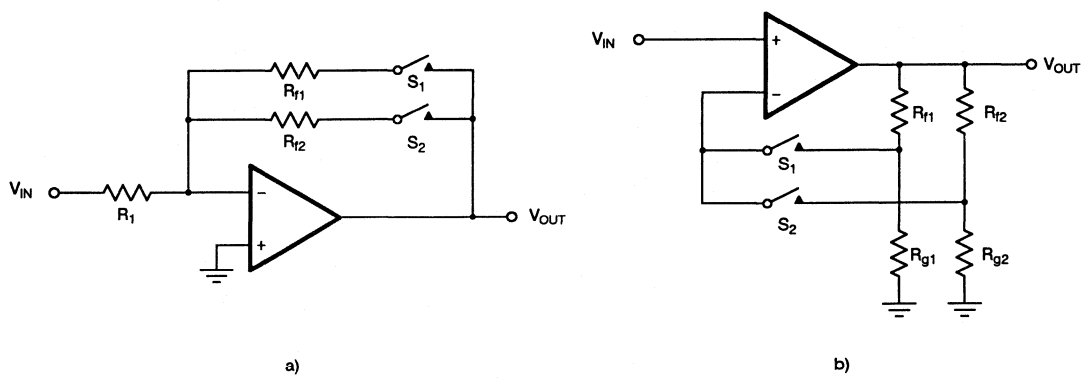

Figure 6. DG408 Typical Characteristics

The 30-Ω resistor serves two purposes. It limits the current through the $^1/_2$ DG405 to less than its 100-mA (maximum pulsed) rating and also helps to decouple the PGA output from the capacitive load, preventing oscillations.

For best results, in applications where high gains are required due to very low-level transducer outputs, as with strain gages and thermocouples, the signal path to the PGA should be differential.

The Sample-and-Hold Circuit

The sample-and-hold (S/H) circuit uses a $^1/_2$ DG405, a fast (t_{ON} < 250 ns) switch. In this circuit, the two switch sections are at similar potentials in the sample mode, so when they open, they create similar charge injections which tend to cancel each other, therefore, helping to minimize the step error. R_1 can be trimmed to obtain the best possible charge injection cancellation. During the hold mode, the dual switch arrangement also helps to reduce the droop rate. Figure 7 is a scope plot that illustrates the S/H action. Note that acquisition time is a function of the output amplifier's slew rate and settling time.

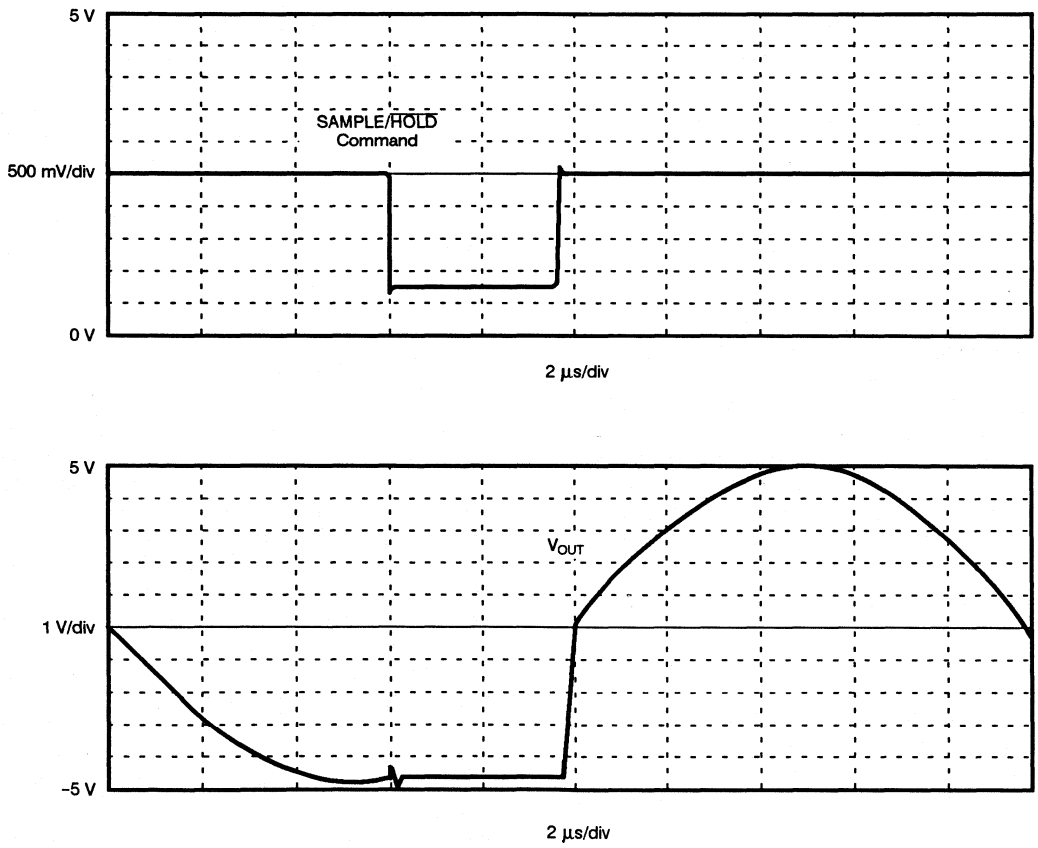

Figure 7. Acquisition Time Depends on Amplifier's Slew Rate

Evaluation Results

Figure 8 shows the transfer characteristics obtained for the three different temperature sensors used. Curve (c) is produced by the "mV output" of a digital thermometer, using the same thermocouple that produced curve (d). Notice the effect that the cold-junction compensation has on the curve (i.e., it causes a 0-V output at 0°C).

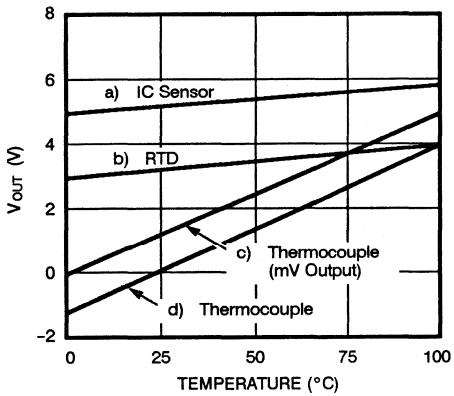

Figure 8. Transfer Characteristics for Various Temperature Sensors

As far as resolution is concerned, all three sensors showed satisfactory results for the 0 to 100°C range evaluated. The thermocouple output gave a resolution equivalent to 0.05°C/bit in a 12-bit system. The RTD and AD590 outputs, as configured, only gave the equivalent of 0.5°C/bit and 1°C/bit resolution, respectively. However, depending on the temperature range of interest, this circuit can be modified to produce a larger ΔV and offer a resolution equivalent to 0.01°C/bit.

Figure 9 shows the waveforms obtained when switching back and forth between channel S_2 (AD590) and S_4 (RTD). Note that the PGA output takes longer to settle when the AD590 is selected. On the other hand, the lower output impedance of the RTD sensor makes the PGA output settle about three times faster. From these waveforms, we can estimate the throughput of the system. Allowing 20 µs for settling times and assuming a 12-bit A/D converter with a 15-µs conversion time,

Throughput rate = 1/35 µs = ~28 kHz

Precision will depend on the method used to read the transfer characteristics. Factors such as ADC accuracy, transducer accuracy, noise corruption, leakage throughout the signal path, and amplifier offsets must be considered. The DG400 switching devices, with their extremely low-leakage specifications and micropower consumptions, practically eliminate leakage and parasitic thermocouple errors. In our case, two transducers outputs are large enough that they are sufficiently free from 60-Hz noise corruption. The thermocouple leads need to be shielded to reduce this problem. Also, a low pass filter is recommended. The amplifiers' offsets were trimmed out, and the PGA's gains could also be trimmed. In this case, we selected precision resistors to get within 0.00025% of the target gains desired.

The PGA was configured for $A_V = 2$ and the op amp offsets were adjusted with trimpots. In our circuit, we selected AGND at the input to the multiplexer and adjusted the PGA offset for 0 V at its output. We then adjusted the S/H amplifier offset for 0 V at V_{OUT}. When we switched to $A_V = 1{,}000$, the PGA output went to above 30 mV. In a microprocessor-based system, the amplifier offsets could be compensated in software. This type of correction would also allow the system to compensate for amplifier drifts with time or temperature, which is much more difficult to do using trimpots.

Overvoltage Protection

The supply voltage applied to the constant current source was intentionally raised to +25 V, and the RTD was disconnected. This allowed us to simulate one of those "unlikely" events where the current source would force a voltage on S_4 that is higher than V^+. This would create an overvoltage condition that won't damage the multiplexer since the current source does not force more than the absolute maximum current rating (20 mA) into the clamping source-to-substrate diode. However, to prevent the possibility of parasitic transistor action that can cause errors on other channels, a low-V_F (1N5819) Schottky diode (D_1) was installed from S_4 to V^+. The low forward voltage of the Schottky diverts the overvoltage current so that the clamping diode and its associated parasitic transistors are not activated. Another form of overvoltage protection would be to connect a Zener diode (like a 1N5928) from S_4 to ground to keep the S_4 input voltage below +15 V.

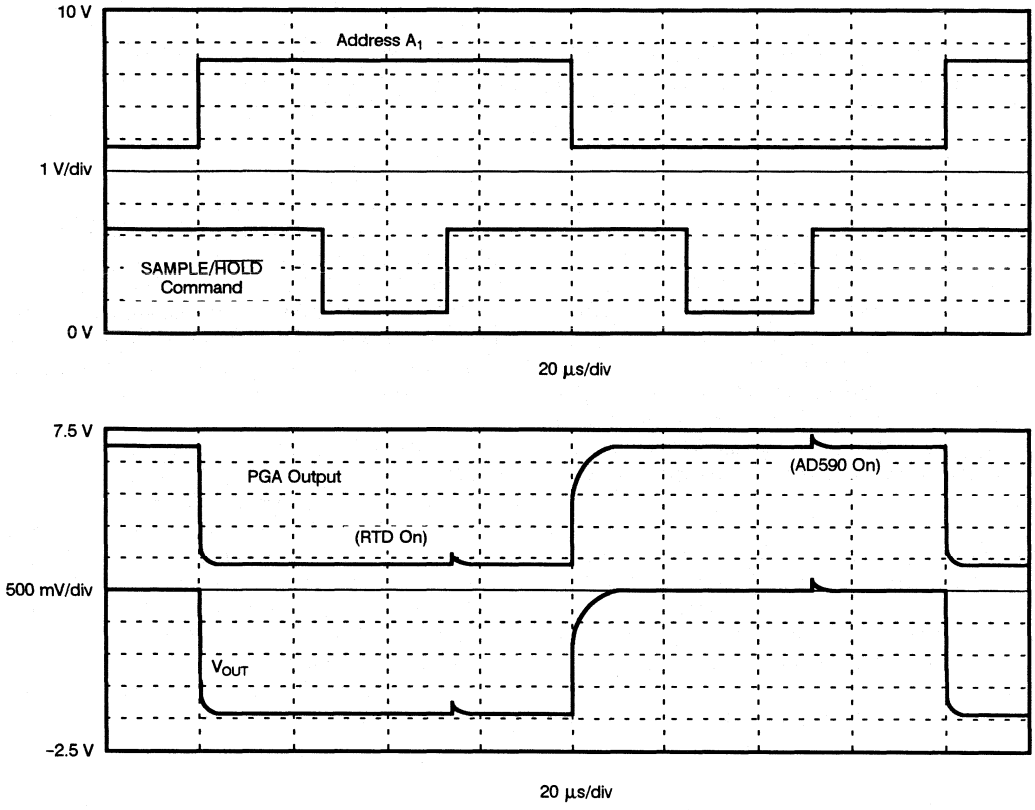

Figure 9. Waveforms Obtained When Monitoring S_2 and S_4 Only

Conclusion

The low $r_{DS(ON)}$, low leakage, low power, and high speed of the DG400 family of analog switches and multiplexers improve the performance attainable in precision data gathering systems. Since they are pin-compatible with older metal-gate devices, the DG400 family permits an easy upgrade of many existing designs.

References

1. *Integrated Circuits Data Book*, **Siliconix incorporated, 1988.**
2. *Interface Magazine*, **Siliconix incorporated, Winter 1988.**
3. *Omega Temperature Measurement Handbook and Encyclopedia*, **Vol. 26, 1988.**
4. *Analog Switches and Their Applications*, **Siliconix, 1980.**
5. **J. Taylor,** *Computer-Based Data Acquisition Systems Design Techniques*, **ISA, 1986.**

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Siliconix incorporated

MICROPROCESSOR-COMPATIBLE MULTIPLEXERS FACILITATE VIDEO SWTICHING DESIGNS

Gareth Powell
Revised June 1989

For many new communications systems – such as ISDN (Integrated Services Digital Network), cable TV, and local area networks (LANs) – traditional switching techniques have become inadequate. To meet the demands of these applications, semiconductor switching devices must now handle wider bandwidths and offer more on-chip features to achieve low chip-count solutions. Higher integration, smaller packages, easier device paralleling/combining, and improved dynamic performance are essential features for designing large-capacity switching systems.

Analog video information is frequently digitized for processing in frame grabbers, TV standard converter (e.g., NTSC to PAL), time-base correction, special effects, or merely as a means of reducing noise levels and enhancing resolution. However, the price paid for the advantages of the digital technique is the substantially wider bandwidth occupied by the digitized signal. Thus, in a typical 8-bit conversion, the sampling rate must be at least three times the chrominance subcarrier frequency of 4.43 MHz: that is, 13.3 MHz. Thus, the bit rate is 8 x 13.3 = 106.44 Mbps. This bandwidth requirement precludes the use of a majority of components and switching techniques commonly employed in video systems.

Video switching applications, such as high-definition TV, digital video equipment, and broadcast studio switches have forced improvements in semiconductor switch performance. The Siliconix DG534 and DG538 are members of a fast growing family of multiplexer/demultiplexer devices with performance characteristics optimized for wideband switching applications. This application note presents the benefits of the DG534 and DG538 in a diverse range of wideband switching applications, highlighting the devices' performance features and providing useful circuit design techniques.

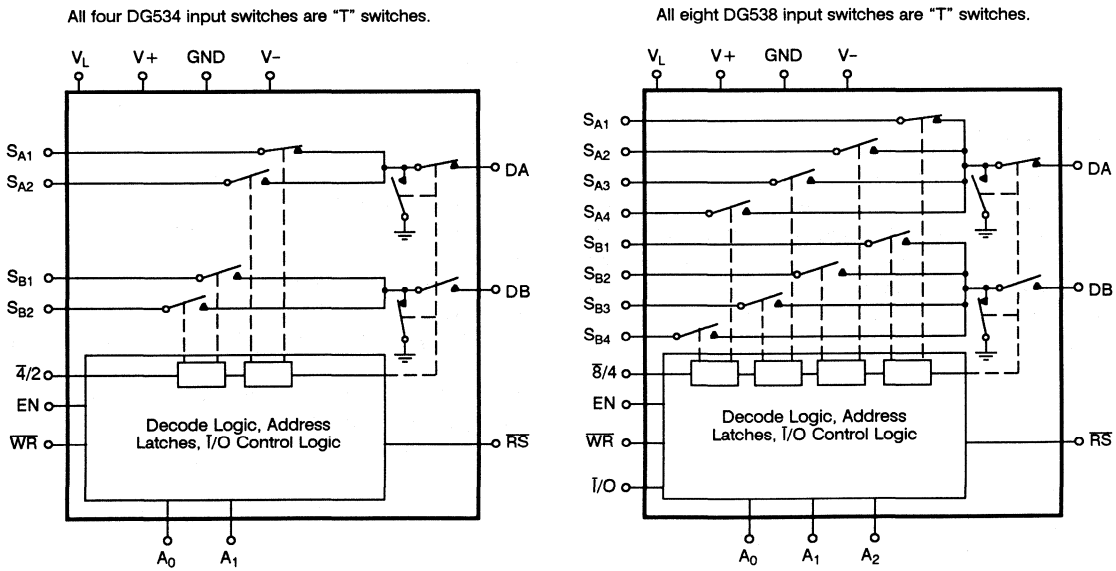

Figure 1. DG534 and DG538 Functional Schematics

Device Description

The DG538 is a wideband single-ended 8-to-1 or differential 4-channel multiplexer. Several DG538s can easily be configured to create a more complex matrix or to handle crosspoint functions. The DG534, similar to the DG538 with half the number of channels, is a 4-to-1 single-ended or a 2-to-1 differential multiplexer.

D/CMOS processing enables these devices to be optimized for high-frequency signal handling with low ON-resistance while on-chip CMOS circuitry provides all the level shifting, logic interfacing, and latching functions that permit easy system design. The switch structure utilizes lateral n-channel DMOS transistors configured in a "T" arrangement, as shown in Figure 1. The "T" switches are arranged into two groups. Each group is selected by the second-stage "L" switches. This two-level switching configuration minimizes channel capacitance and off-state signal crosstalk (maximizes OFF-isolation).

For comparison, Figure 2 shows the single-channel crosstalk characteristics of the DG538 video multiplexer and the industry-standard DG508A. Note the 35-dB performance improvement of the DG538 versus the standard CMOS 8-channel multiplexer.

The DG538 data sheet specifies all-hostile crosstalk. This is a much more rigorous test specification than single-channel crosstalk since it requires all seven "off" channels to be tied together. More crosstalk signal is seen at the switch under these test conditions because there are seven parallel paths, as opposed to only one, and the crosstalk contribution of the package and the PC board are also more apparent. Nevertheless, the all-hostile crosstalk of the DG534 and DG538 approaches –70 dB at 5 MHz, easily meeting most video switching requirements.

It is not merely the "T" and "L" configurations that give improved crosstalk. Careful on-chip layout and optimum device sizing were also required. A small device exhibits low intrinsic capacitances, but has greater ON-resistance and, hence, will give a greater insertion loss. However, by employing DMOS (double diffused MOS) FETs for the switches, an excellent compromise between $r_{DS(ON)}$ and intrinsic capacitances is achieved.

Figure 3 shows a cross section of an n-channel device made with the D/CMOS process, incorporating DMOS and PMOS transistors. The fabrication of the "T" switch is shown. The short-channel feature of the DMOS devices offers 8 to 10 times less channel capacitance than a conventional lateral NMOS transistor for a given $r_{DS(ON)}$. Figure 3 also shows the n- and p-channel devices that form the CMOS logic interface, level shifting, and latches.

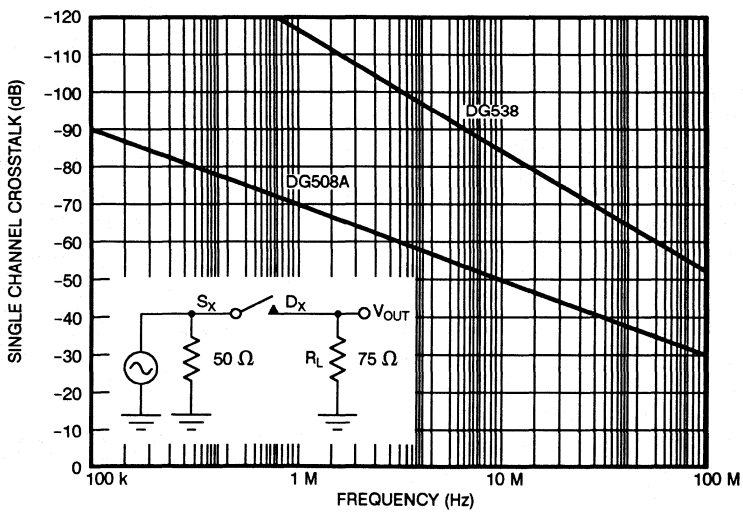

Figure 2. DG538/DG508A Single-Channel Crosstalk vs. Frequency

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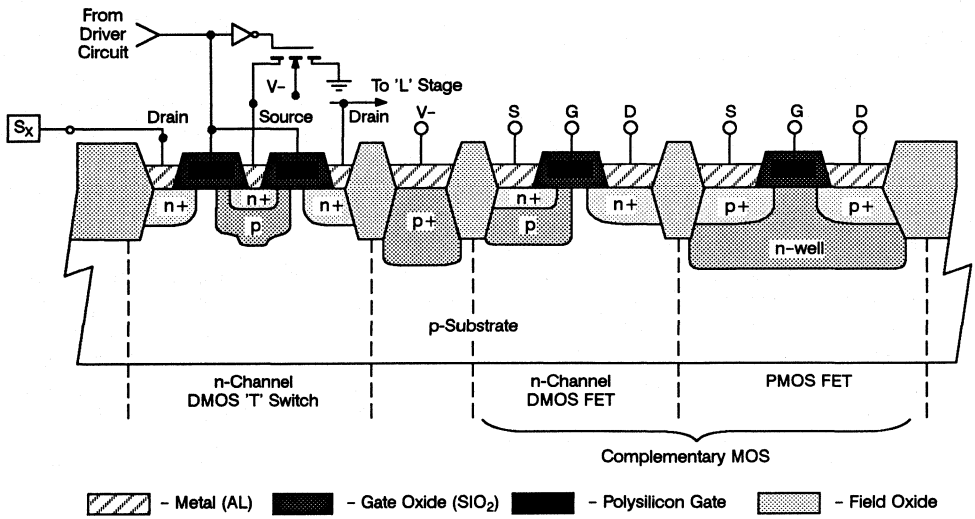

Figure 3. Cross Section of the D/CMOS Process

The cross section shows many pn junctions which would become forward biased if signals applied to the device were more negative than the "p" substrate. For this reason, when handling ac signals, the substrate is connected to a negative voltage (V-) to allow signals to swing below ground.

Using a negative supply also optimizes device capacitances. The body effect on DMOS devices causes the ON-state capacitance to change as a function of V-. For a fixed analog signal, C_{ON} reduces exponentially as the source-to-substrate voltage increases (see Figure 4). Other performance benefits can be attained by choosing a particular V- (see Figure 19).

In the event of an overvoltage (analog signal going more than a diode drop beyond V-), the pn junction between the source or drain and the substrate will forward bias, causing a large current to flow. This fault current will not damage the device as long as the current flow is less than 20 mA. However, low-impedance source circuitry is typical of many applications; for example, the characteristic impedance of video systems is 75 Ω. Thus, a means of current limiting should be employed in circuits where overvoltage transients are possible. Figure 5 shows a transient protection scheme that uses a diode in V-. This diode (normally forward biased) becomes reverse biased with overvoltage transients, thus eliminating fault current flow.

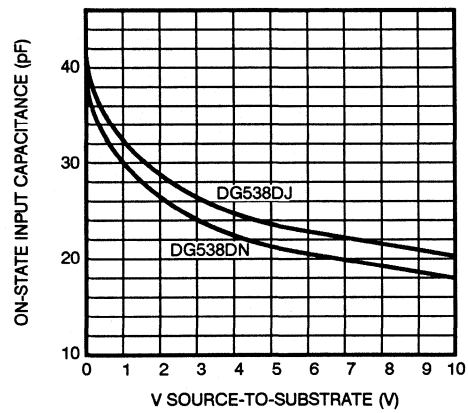

Figure 4. DG538 ON-state Input Capacitance vs. Source-to-Substrate Voltage

Positive overvoltages (> V+) are a different problem. The switch will merely turn OFF (no enhancement) if signals approach or exceed V+. The DMOS drain diffusion has a fairly high breakdown voltage (typically > 30 V). Large avalanche currents can flow during

breakdown, therefore, either the signals must be externally clamped to avoid exceeding breakdown voltage, or a means of external fault current limiting should be adopted. Since the source diffusion will only develop a voltage during the switch "ON" state, under normal supply conditions this breakdown (source-to-substrate) is unlikely to occur due to the device turning OFF when the source voltage, V_S, approaches V+. Therefore, external positive overvoltage protection is only required when transients or overvoltages are expected to be in excess of +30 V.

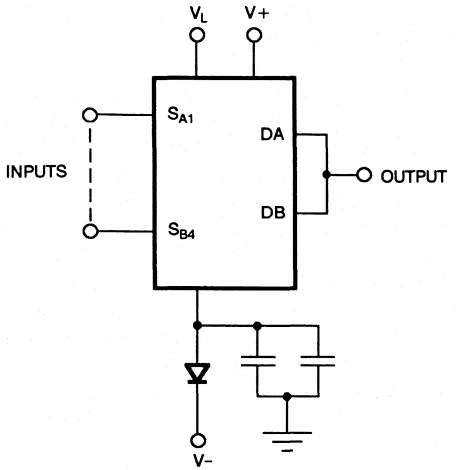

Figure 5. Negative Overvoltage Transient Protection

Addressing and Logic

A DG538 device can be configured as a single-ended or as a differential multiplexer by applying the appropriate logic to the $\overline{8}/4$ pin. When this pin is high (the differential condition), address A_2 is not used. Note that DA and DB must be externally connected for the single-ended mode.

The logic trip-point reference for the internal comparators is derived from logic voltage, V_L, i.e., when V_L = +5 V, true TTL compatibility is achieved. In this case, the logic levels required to activate the various control pins($\overline{8}/4$, $\overline{I}/O$, EN, A_X, $\overline{WR}$, $\overline{RS}$) are 0.8 V and 2 V. Variation of V_L enables the switching threshold to be shifted (Figure 6).

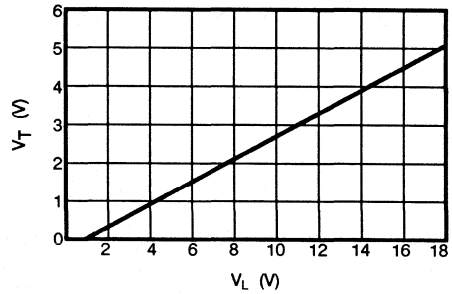

Figure 6. DG538 Switching Threshold vs. Logic Supply Voltage (V_L)

The DG538 and DG534 have tri-state latches on their address pins, allowing three modes of operation:

1. **Input Data.** In this mode, the multiplexer accepts data applied to A_X causing appropriate switch selection. This mode is selected by the following logic conditions:

   $\overline{I}/O$ = 0 (input mode)
   $\overline{WR}$ = 0 (latches transparent)
   EN = 1 (device enabled)
   $\overline{RS}$ = 1

2. **High Impedance.** In this mode, the address pins assume a high impedance (open circuit) state. It is selected by

   $\overline{I}/O$ = 0
   $\overline{WR}$ = 1 (data latched state)
   EN = X
   $\overline{RS}$ = 1

   The tri-state (high-impedance) mode of operation is particularly useful in microprocessor-controlled systems. It enables many devices to be paralleled on a common control bus without significant loading. This feature helps fulfill the demands of large matrix systems.

   By decoding the microprocessor's address bus, the DG538/DG534 can be activated to respond to logic control signals transmitted by the microprocessor on its data bus, only when required to do so.

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3. **Output Data.** The last data written to the latches are reflected as logic outputs on A_0, A_1, and A_2. This is achieved when

   $\overline{I/O}$ = 1 (output mode)
   $\overline{WR}$ = 1
   EN = 1
   $\overline{RS}$ = 1

The "data readback" feature is convenient in handshaking functions where "route-selected" status monitoring is required. This also eliminates additional peripheral devices for this function. Data readback may also be used to preserve the switch configuration during and after a power failure to the microprocessor. Normally after power failure, the microprocessor must go through a complete system reset routine. Provided power to the DG538/DG534 has not been disrupted, when the microprocessor's power is re-established, it can poll the multiplexers and resume immediate control. This capability simplifies microprocessor software requirements and reduces service interruptions.

In the address output state, the address outputs can source or sink 0.4 mA. Logic high from the address output is V_L. When operating V_L at voltages higher than +5 V, it is important to consider the possibility of damaging effects on TTL devices connected to the address bus.

To ease microprocessor interfacing, additional control pins are featured.

- $\overline{WR}$. This input activates the data latches for strobing-in an address word when $\overline{WR}$ goes low (i.e., transparent latches). The strobing signal is normally obtained by decoding the microprocessor address data. This pin eliminates the need for external latches or peripheral devices such as $\overline{I/O}$ ports for connection to the microprocessor's bus.

- $\overline{RS}$. This input initiates a direct reset command that clears all data latches and opens all switches. This pin can be used as a "master reset." It is of particular significance during system power-up since the microprocessor's reset control pin may be used to clear all switches prior to channel/routing selection. Thus, the software used to sequentially clear all multiplexers is unnecessary.

Figure 7 illustrates the ease of microprocessor interface with the DG538 and shows an alternate use for the $\overline{RS}$ function as a chip-select control in a 32-to-1 video switching application. The $\overline{RS}$ function overrides all other control signals. Note that $\overline{RS}$ is not a latched input. An external D-type latch is required so that A_4 can be connected directly to the data bus. A_0 to A_3 are latched internally to the DG538.

The 8085 microprocessor data bus (after having its low-order address lines demultiplexed) connects directly to the address inputs (A_0 to A_2) on all the DG538s and on A_3 and A_4. The system responds to stimuli on the data bus only when a write command is received. A write signal is produced by first decoding three (or more) lines of the high-order address lines using a 3-to-8 decoder and then gating (OR) one of the decoder output lines with the microprocessor's $\overline{WR}$ output. This enables switch selection only when the appropriate address data is received; otherwise, switch states remain latched and their control inputs are all in the high-impedance mode, leaving the microprocessor's data bus free to execute other routines.

Switch inputs 1 to 32 can be selected by a 5-bit word transmitted on the data bus coinciding with a write signal.

Even though the $\overline{RS}$ pins on the four DG538 devices are used for chip select, a direct reset or no-channel-selected condition is easily achieved using a CMOS analog switch (DG403), as shown in Figure 7.

An important consideration for direct microprocessor interface is input timing compatibility. Table 1 shows minimum input timing requirements of the DG538/DG534 compared with the corresponding minimum output timing specifications of some popular microprocessors.

TABLE 1. Microprocessor Timing Compatibility

PARAMETER		DG538/4	8085A	8085A-2	Z80	6800
t_{WW} Width of Control Low ($\overline{WR}$)	(ns)	200 (min)	400 (min)	230 (min)	360 (min)	470 (min)
t_{DW} Data Valid to Trailing Edge of Write	(ns)	100 (min)	420 (min)	230 (min)	200 (min)	575 (min)
t_{WD} Data Valid to Trailing Edge of Write	(ns)	50 (min)	100 (min)	60 (min)	100 (min)	150 (min)

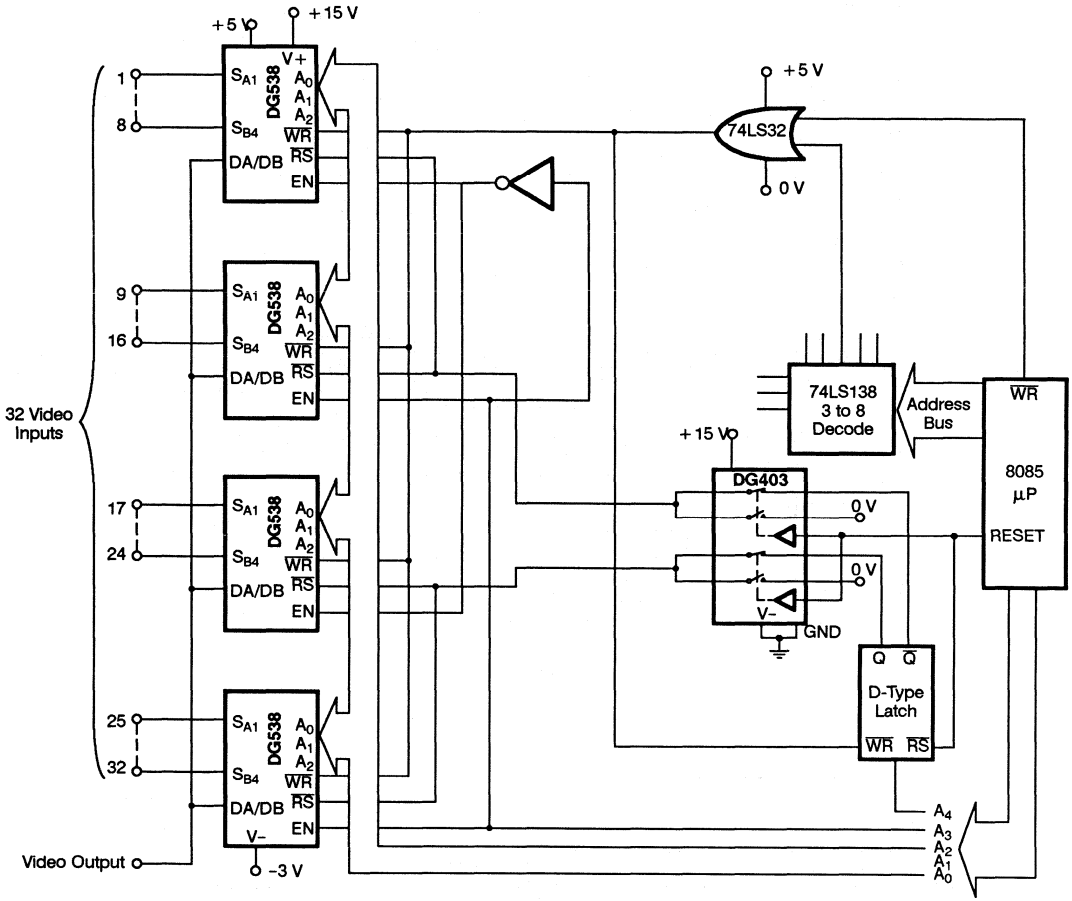

Figure 7. A 32-Channel Single-Ended Wideband Multiplexer Controlled by an 8085

Methods of interface to other microprocessors are shown in Figure 8. An address decoder (for a memory-mapped type of operation) is required for all interface circuits. Various gating arrangements are required, depending on the microprocessor's peripheral control output architecture.

In some cases, it might be convenient to use $\overline{RS}$ as a power-up failsafe. The circuit shown in Figure 9 illustrates a method for using $\overline{RS}$ as a power-up delay circuit. This allows microprocessor buses or control logic sources to stabilize after power-up before the DG538 responds to control signals. During power-up, indeterminate logic states and/or transients might be present on control or data lines. The RC values are set to ignore spurious control signals.

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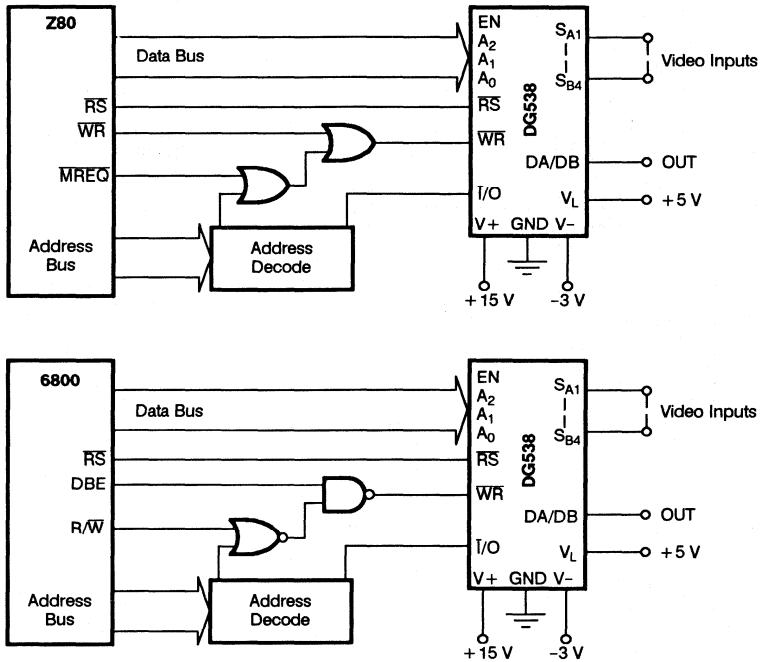


Figure 8. Other Microprocessor Interfaces

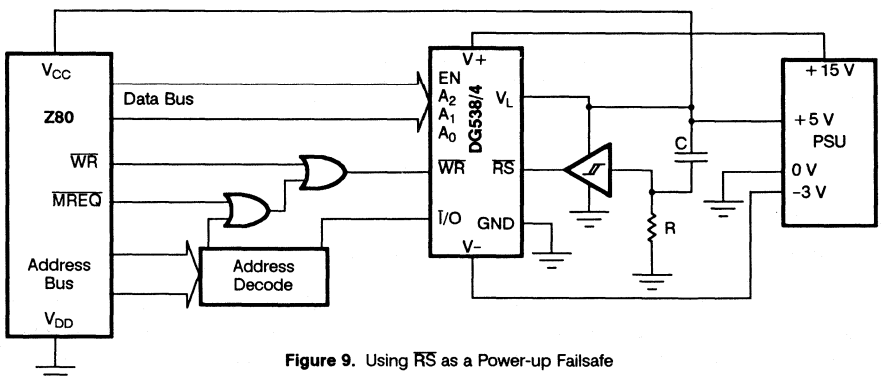


Figure 9. Using $\overline{RS}$ as a Power-up Failsafe

Characteristics

The DG538 and DG534 data sheets include detailed operating characteristics, typical parameters, and limit values. The important dynamic characteristics, such as crosstalk and bandwidth, are plotted against frequency (to 100 MHz) to help designers predict system performance, since these parameters are measures of the ON-state and OFF-state multiplexer performance.

Specialized video specifications not included on the data sheet are presented here to provide a better understanding of the devices' performance and suitability for a wide range of video and general wideband switching applications.

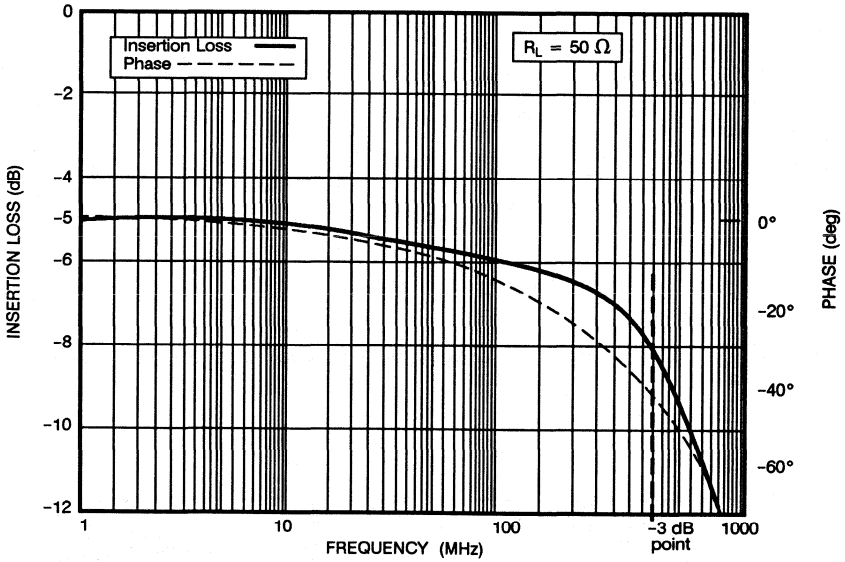


Figure 10. DG538 Bandwidth and Phase Response

Bandwidth is a measure of the ON-state performance and is defined as the frequency at which the signal falls -3 dB from the low-frequency insertion loss figure. Figure 10 shows the typical frequency characteristics of the DG538 measured on an HP8573A network analyzer.

Since a multiplexer channel exhibits ON-resistance, $r_{DS(ON)}$, and ON-state capacitance, $C_{(ON)}$, increasing signal frequencies are progressively attenuated. However, it is a common misconception that the bandwidth can be calculated from the $r_{DS(ON)}$ and $C_{(ON)}$ specifications given on the data sheet.

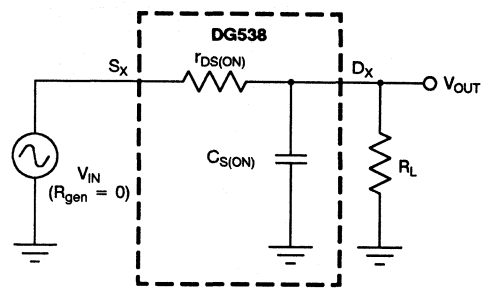
The -3 dB frequency for the model shown in Figure 11 is given by the formula:

$$-3\text{ dB} = \frac{1}{2\pi \left[\frac{R_L \times r_{DS(ON)}}{R_L + r_{DS(ON)}}\right] C_{(ON)}}$$

Substituting $R_L = 50\ \Omega$, $r_{DS(ON)} = 50\ \Omega$, and $C_{(ON)} = 23$ pF give an $f_{-3\text{ dB}} \approx 310$ MHz.

The measured frequency response for the same 50 Ω load (Figure 10) shows a -3 dB point of over 500 MHz. This apparent discrepancy results because the $r_{DS(ON)}$ and $C_{(ON)}$ are distributed among the five DMOS FETs that form the "T" and "L" switches.

A SPICE simulation of the model shown in Figure 12 gave a 510 MHz -3 dB point, which is much closer to the measured value (see Figure 13).



$$\text{Insertion Loss (dB)} = 20 \log \frac{V_{OUT}}{V_{IN}}$$

Figure 11. Erroneous Model for Frequency Response Calculations

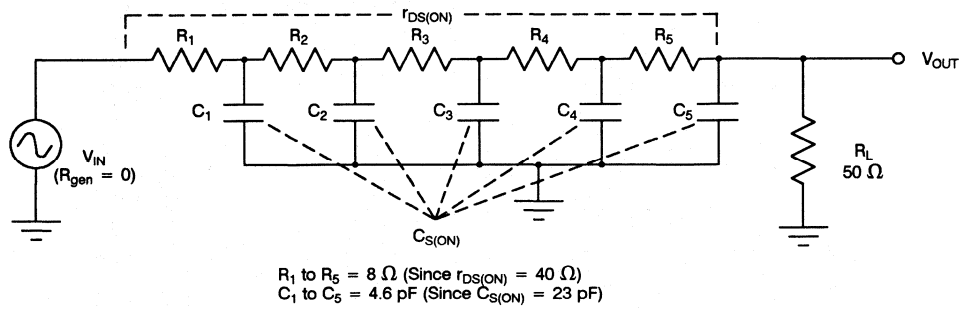


Figure 12. Five-Stage RC Model

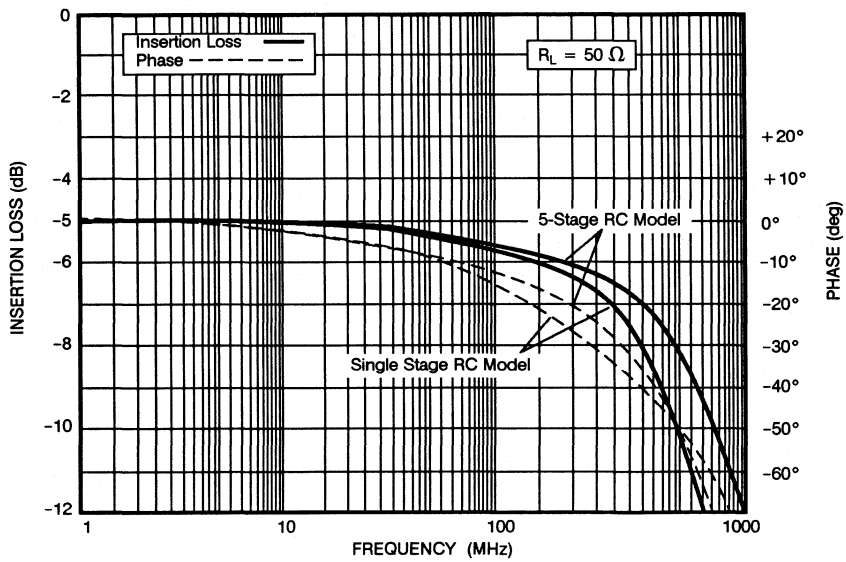


Figure 13. Bandwidth and Phase Response for the Models of Figures 11 and 12

Note that the equivalent five-stage RC circuit shown in Figure 12 is not a complete model of the DG538 transmission path. However, it does illustrate the effect of distributed parameters. An actual model would be far more complex, with other reactive elements that incorporate package capacitances, inductances, etc.

In the absence of a better model, the circuit shown in Figure 12 is useful for predicting bandwidths in crosspoint systems where the frequency response will be affected by paralleling devices (Figure 14).

A 10 Ω source impedance is included in Figure 14. This source impedance simulates the low-output impedance of a video buffer amplifier generally employed at the input to the matrix. The simulation results of the circuit, using single-stage and five-stage models for different numbers of parallel channels, are shown in Table 2.

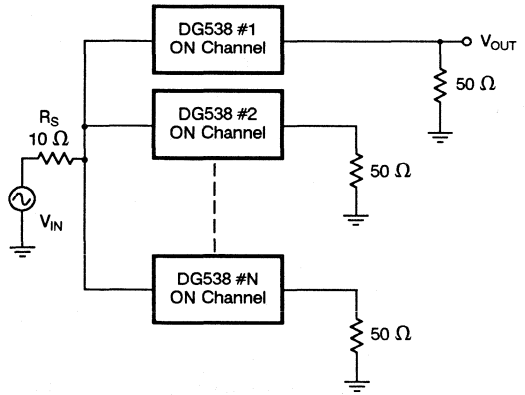


Figure 14. Equivalent Diagram of an 8 x N Crosspoint Using DG538s When One V_{IN} is Selected to All Outputs

Table 2.

Number of Parallel Channels	-3 dB Bandwidth (20 Log $\frac{V_{OUT}}{V_{IN}}$)	
	Single RC Stage (Figure 11)	5 Stage RC (Figure 12)
1	280 MHz	400 MHz
2	250 MHz	340 MHz
4	225 MHz	260 MHz
8	185 MHz	200 MHz
16	170 MHz	160 MHz

The "flat" response over the bandwidth of interest is an important requirement for video applications. The Independent Television Companies Association (ITCA) specifies the following gain/frequency limits for a video switching matrix.

Mid- to high-frequency response:

±0.1 dB between 100 kHz and 5.5 MHz

±0.25 dB between 5.5 MHz and 8 MHz

Above 8 MHz:

"Response shall fall continuously and smoothly"

Although this specification is for 625-line PAL systems used in the United Kingdom, it is a typical specification and similar to other standards, such as NTSC and sequential color and memory (SECAM).

High-definition TV has much tighter tolerances since it requires bandwidths to 25 MHz. The 0 to 30 MHz frequency response of the DG538 and DG534, shown in Figure 15, is well within the required limits.

Group Delay, sometimes called envelope delay or deviation from linear phase, is the phase-shift rate of change through a circuit or equipment with respect to frequency, or alternatively, non-linearity of the group frequency response. In a transient waveform which has a continuous spectrum, the group delay becomes the transmission time of a packet of spectral components. It follows, therefore, that if the group delay is constant for all the required bandwidth, there will be no difference in the arrival times of the various spectral components which make up the bandwidth.

Because many different frequency components make up a video waveform, this parameter is of particular relevance in video applications. The measured group delay response of the DG538 is shown in Figure 15. It satisfies the most demanding video requirements. The plot shows less than 500 ps over a 30 MHz frequency range.

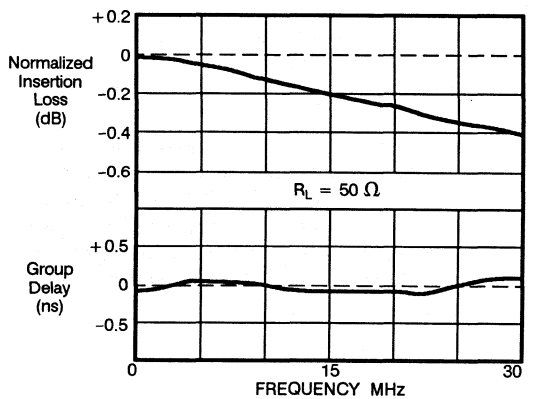


Figure 15. DG538/DG534 Group Delay and Normalized Insertion Loss Response to 30 MHz

Non-Linearity Distortions

Color video can be divided into two groups: component video [separate red (R), green (G), and blue (B) signals] and composite video, which contains color and brightness (chroma and luma) information in a single waveform.

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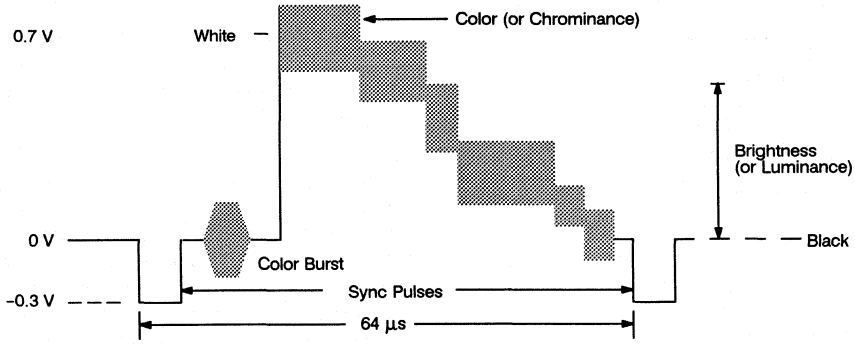

Figure 16. Basic Composite TV Signal

Composite video has various specifications that relate to the interaction of chroma and luma. In particular, differential gain and differential phase must be specified for video components or systems. To illustrate these distortions, consider the basic composite TV signal. Figure 16 shows a typical color TV signal. The sync pulses, occurring every 64 µs, synchronize horizontal line deflection. The color signal contains both luminance and chrominance. When this signal is processed by a domestic TV receiver, the red, green, and blue components are recovered and used to modulate three individual electron beams.

The amplitude of the chroma contains the color intensity (color saturation), and its phase difference with respect to the color burst determines the blend (hue) of color.

- **Differential Phase.** Measured in degrees, this is the phase shift of the color subcarrier resulting from a change in the amplitude of the associated luminance component. Differential phase shows up in NTSC pictures as a change in hue, a color change more noticeable in a shaded area of the picture.

  Frequency related phase shifts (as opposed to differential phase) will cause no change in picture quality since both color burst and chrominance are equally shifted.

- **Differential Gain.** Expressed as a percentage, this is a form of distortion resulting from changes in the amplitude of the chrominance signal as a function of luminance amplitude.

  The effect on NTSC and PAL pictures is a change in color saturation with changing luminance level. The eye is fairly tolerant to differential gain since the resulting picture changes are fairly subtle. For instance, a brightly colored car traveling from a sunny area of the picture to a shaded area would appear as though its body color intensity had suddenly changed.

Specialized equipment is employed to measure differential phase and gain. Specifications, such as ITCA, require standard test signals and dedicated test equipment and techniques. Recognized standard test waveforms are shown in Figure 17.

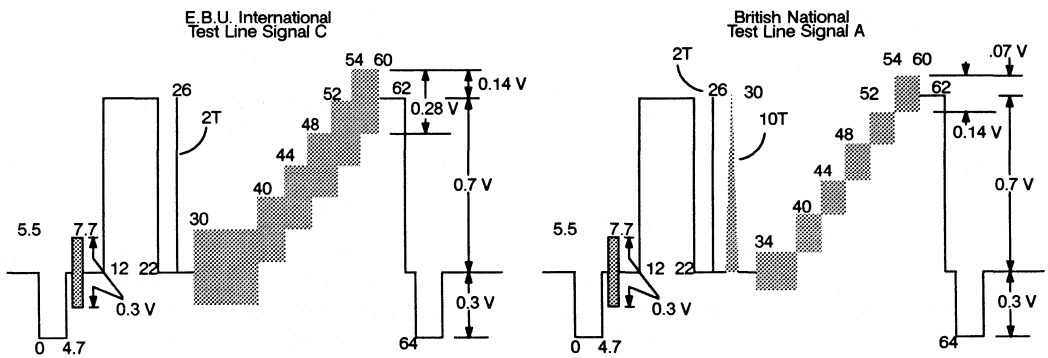

Figure 17. Standard Test Waveforms

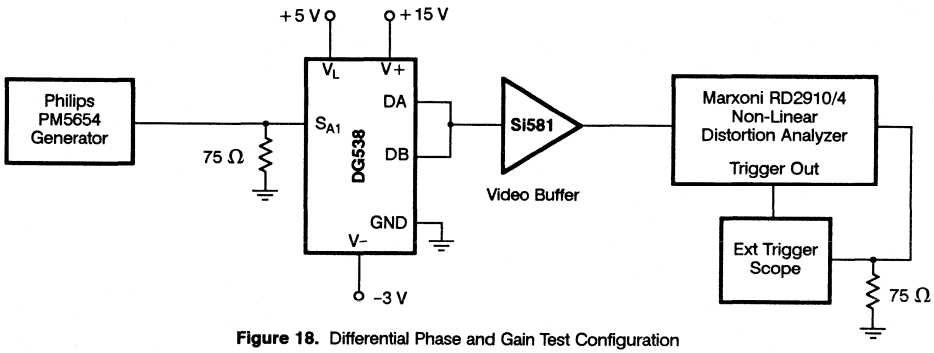

Figure 18. Differential Phase and Gain Test Configuration

Chrominance amplitude variation over the five Average Picture Levels (APLs) indicates differential gain. Differential gain is expressed as the greatest change (in %) of the chrominance amplitude with respect to its amplitude at black level. Similarly, differential phase is the greatest change in chrominance phase shift referred to the phase of the chrominance at black level. Test configuration and equipment used to characterize the DG538 for differential phase and gain are shown in Figure 18.

The equipment shown in Figure 18 must be correctly terminated, or signal amplitudes are affected giving erroneous results. A video buffer (Si581) provides a 75 Ω resistance to the signal generator, and the signal through the switch meets the standard 1 V_{p-p} amplitude. Since most applications use a video buffer following the multiplexer, this configuration is very realistic. The inherent non-linearity of the circuit (bypassing the DG538) is first measured, and then subtracted from the measured value when the device under test is inserted.

Supply Variation Effects on Non-linearity Distortion

Supply voltage variation causes various transmission impedance changes. Therefore, both differential phase and gain are heavily dependent on power supply values. Figures 19 and 20 show the typical variation of differential phase and gain versus positive and negative supply. These curves enable optimization of performance by careful choice of supplies.

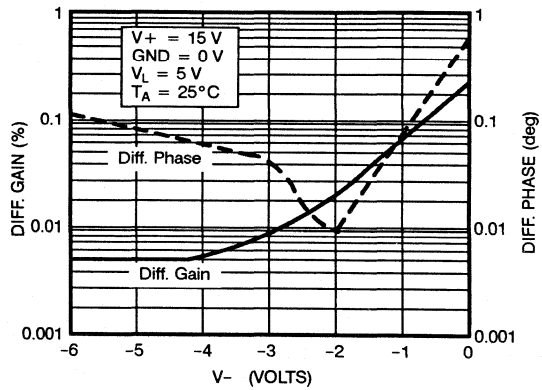

Figure 19. Differential Gain/Phase vs. V-

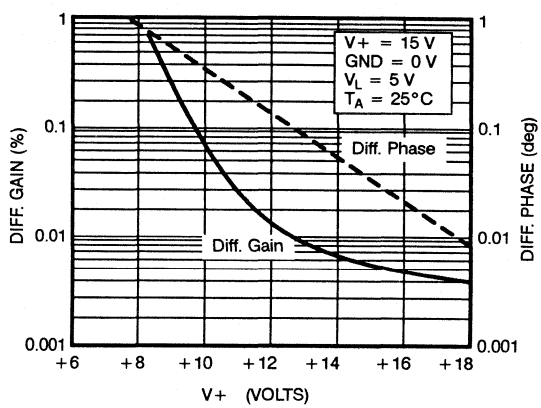

Figure 20. Differential Gain/Phase vs. V+

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Generally, high-performance video switching systems require less than 0.5% differential gain and 0.5° differential phase. Therefore, limits of 0.1% and 0.1° could be applied to a single switch component. Figure 21 shows the power supply operating area that achieves < 0.1% and 0.1° performance for DG538 devices.

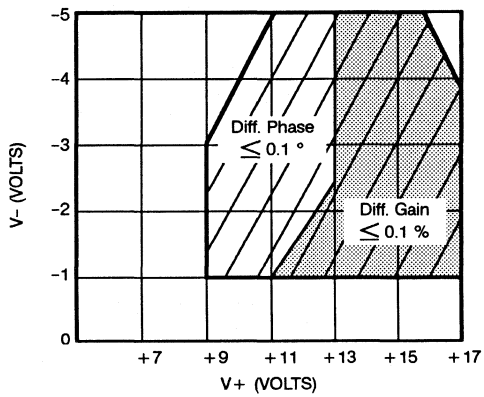

Figure 21. DG538 Supply Ranges to Maintain <0.1% and 0.1° Differential Gain and Phase

Handling Precautions

All MOS devices can be damaged by the presence of excessively high electric fields in the gate-oxide region. Such fields can cause the gate oxide to rupture, rendering the device unusable. Mishandling MOS devices may cause catastrophic damage from the build-up of static electricity in the human body, which can reach many thousands of volts.

To reduce electrostatic discharge (ESD) susceptibility in the DG534/DG538, all logic inputs are protected by the circuit shown in Figure 22.

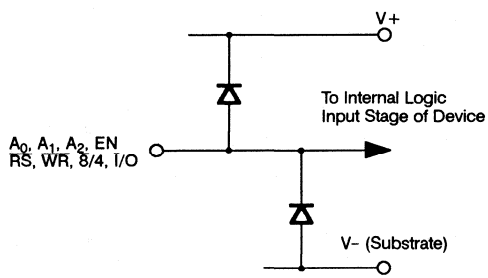

Figure 22. ESD Protection Circuit

Typically, the diode clamps provide ESD protection up 2 KV on any logic input pin. Standard static handling and assembly precautions should, nevertheless, be used to ensure maximum reliability. Anti-static clothing, conductive table-tops, grounded-tip soldering irons, and ensuring that all voltage sources are turned off during the insertion or removal of devices or PCBs are recommended.

Power-Up Sequence

A pn junction exists between V_L and V+, which, in the event of V_L being present before V+ (i.e. V_L > V+,), will become forward biased. Under these conditions, large currents may flow and damage the device. To avoid this condition, the power-up sequence should ensure that V_L does not come up before V+. Normally, this will not present a problem if V+ and V_L are derived from the same power supply.

Printed Circuit Board (PCB) Layout and Decoupling

Selecting components optimized for high-frequency signals does not guarantee adequate circuit performance. Good layout techniques are also very important. At high frequencies, stray capacitance between long adjacent signal lines can provide low impedance paths that couple with one another. Power supply lines can couple rf signals from one circuit to another. Components or sockets that protrude on a PCB surface may act as small antennas which pick up or radiate rf signals. To avoid these problems, be sure signal paths between components are as short as possible and make extensive use of ground planes and shielding between adjacent signal paths.

The DG534 and DG538 have ground pins isolating adjacent channels. These, when connected to grounded shielding paths, give excellent ac performance.

Power supplies should be bypassed by the use of decoupling capacitors mounted as close to the device supply pins as possible. This is of particular importance for the DG534/DG538 since the device substrate connects directly to V-. Two capacitors on each power supply are recommended. A ceramic capacitor of 0.01 to 0.1 μF, provides high-frequency signal bypassing, and a tantalum capacitor (1 to 10 μF) is adequate to bypass low frequencies. Further decoupling can be achieved by adding a low-value series resistor (e.g. 51 Ω) in the supply line.

Components should be assembled on a PCB in a low profile. The DG538, for example, is available as a 28-pin quad surface-mount package or a 28-pin dual-in-line package. The latter has poorer crosstalk performance because it has a larger lead frame and because the device pins are connected through the board. Using sockets should be avoided because they degrade device performance significantly.

Applications

Applications for the DG538 and DG534 are many and varied, ranging from high-frequency signal switching to lower-frequency, low-level signal routing.

Video Systems

The DG534 and DG538 multiplexers are ideal for many wideband switching applications, such as high-resolution financial data networks, forward-looking infrared (FLIR) detectors (night vision systems), CAT (computer aided tomography) scanners, and NMR (nuclear magnetic resonance) medical imaging.

Figure 23 shows the DG538 as an 8-to-1 video source selector. This circuit has many applications in industrial process monitoring systems or in security systems where eight separate video cameras connect to a single monitor in a sequence. The circuit uses three bits to automatically select each source in turn. An override feature can be incorporated to disable the counter and provide manual channel selection.

An example of a differential configuration application is shown in Figure 24. This circuit may be used in component video systems such as TV camera signal routing. Two devices are required for routing four separate RGB sources and their corresponding audio, sync, or timecode signals. Note that the channel select or address bus is common to all devices.

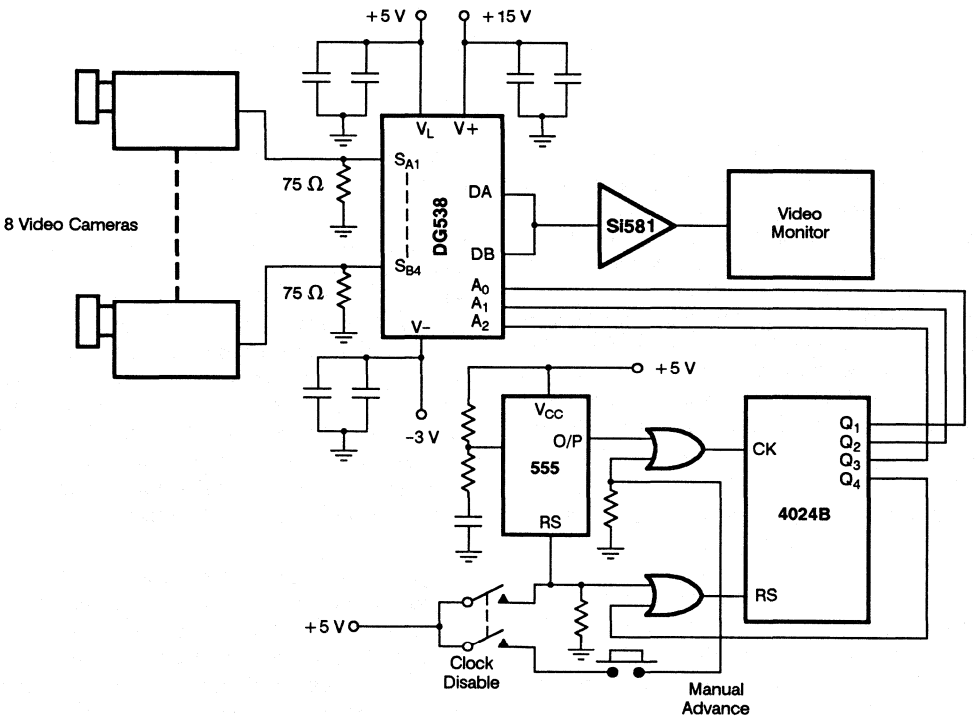

Figure 23. Basic Closed-Circuit TV System

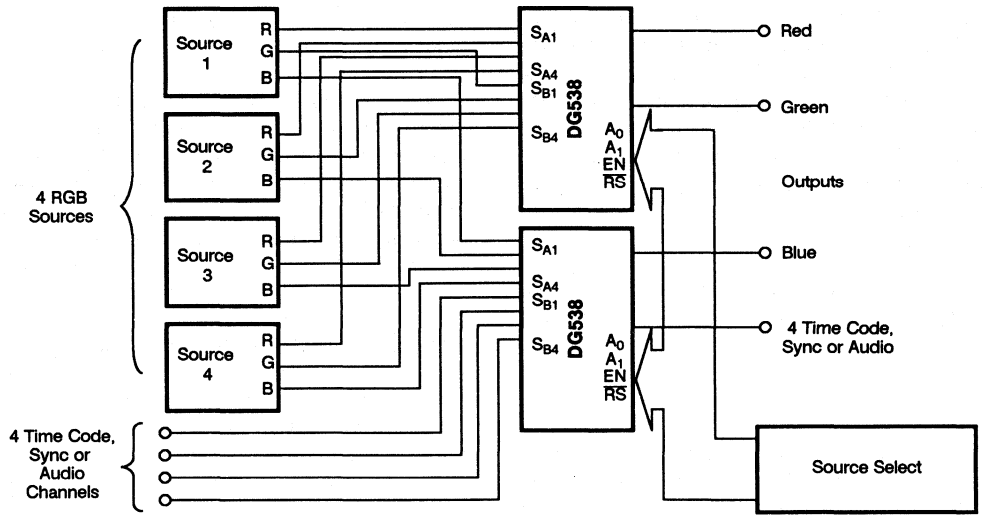

Figure 24. An RGB Plus Timecode, Sync, or Audio Switching System

A majority of video applications require crosspoint configurations, where a number of inputs must be switched to a number of outputs. Applications requiring this type of matrix switching (both analog and digital) range from PCM (Pulse Code Modulation) or telecommunications data switching to financial information routing. A basic crosspoint configuration (8 x 4) is shown in Figure 25. The data-write control strobes address information to each DG538. In turn, the actual address data (for the required route) is present on the address or route-assign bus. Video output buffers are normally used to drive lengths of 75 Ω coax cable.

In Figure 25, the loading of switch capacitances and buffer input impedances on a given video source will vary, depending on the number of outputs. For example, when a single source is switched to all four outputs, it is loaded by 4 x $C_{S(ON)}$ (~92 pF) plus 4 x C_{in} of buffer. This increased loading affects the frequency response and phase shift of the output signal. Note that R_1 is used to set the bandwidth/insertion loss relationship.

Figure 26 illustrates this effect by showing the frequency response of a single output signal for an increasing number of channels connected to the source. Additional channels (2, 3, and 4) are loaded with 10 kΩ to simulate the input impedance of video buffers.

Figure 27 shows measured frequency response of a typical crosspoint circuit using four DG538DJs and both an Si581 wideband buffer and an Si582 wideband op-amp. This circuit arrangement forms the nucleus of any video or wideband crosspoint system, and provides practically transparent switching of video signals to standards sufficient to meet broadcast or HDTV requirements. The data sheets for the Si581 and Si582 provide greater detail for individual performance characteristics, although the in-circuit performance under "real life" conditions is not so apparent.

The circuit employs a front-end input buffer (Si581) to provide the correct termination impedance and drive the crosspoint circuit. R_S is required to minimize gain peaking caused by the loading capacitance. The response shows an increased peaking at single "on" switch conditions due to the capacitance reduction. Although the value of R_S can be optimized to reduce the peak, the frequency at which it occurs is out-of-band in terms of video. Generally, low pass filtering is employed at some stage to eliminate any out-of-band effects.

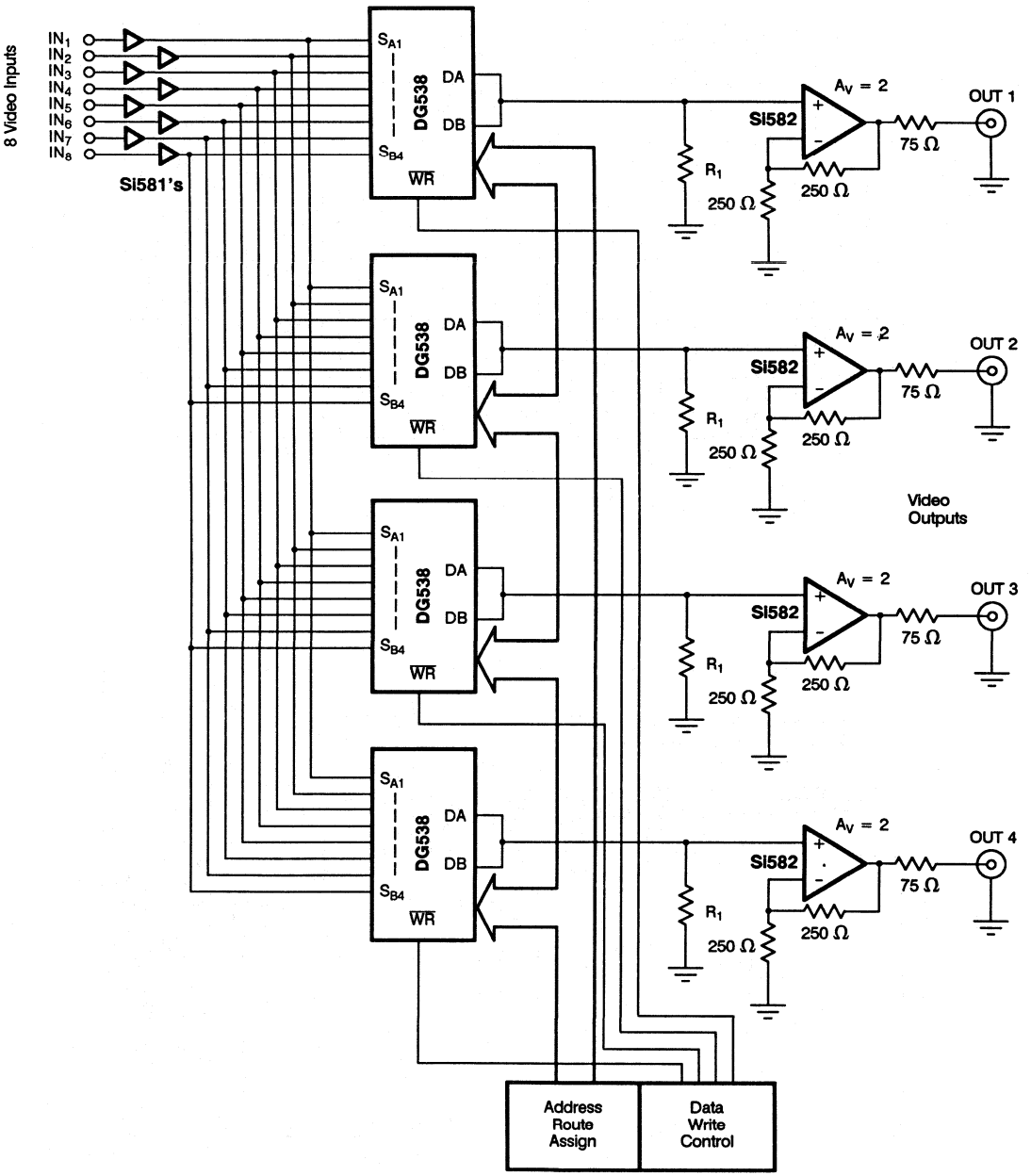

Figure 25. An 8 X 4 Crosspoint Switch

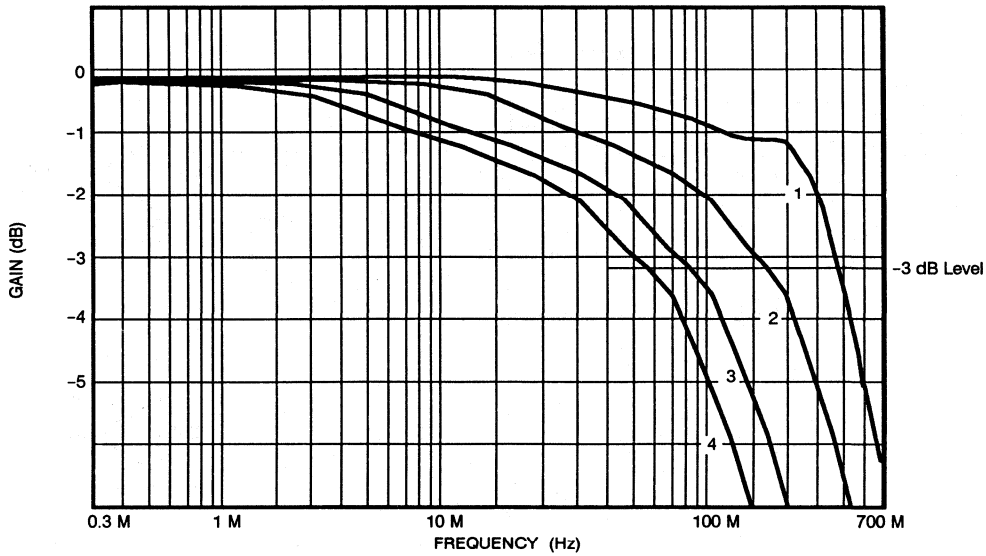

Figure 26. Frequency Response of 8 X 4 Matrix

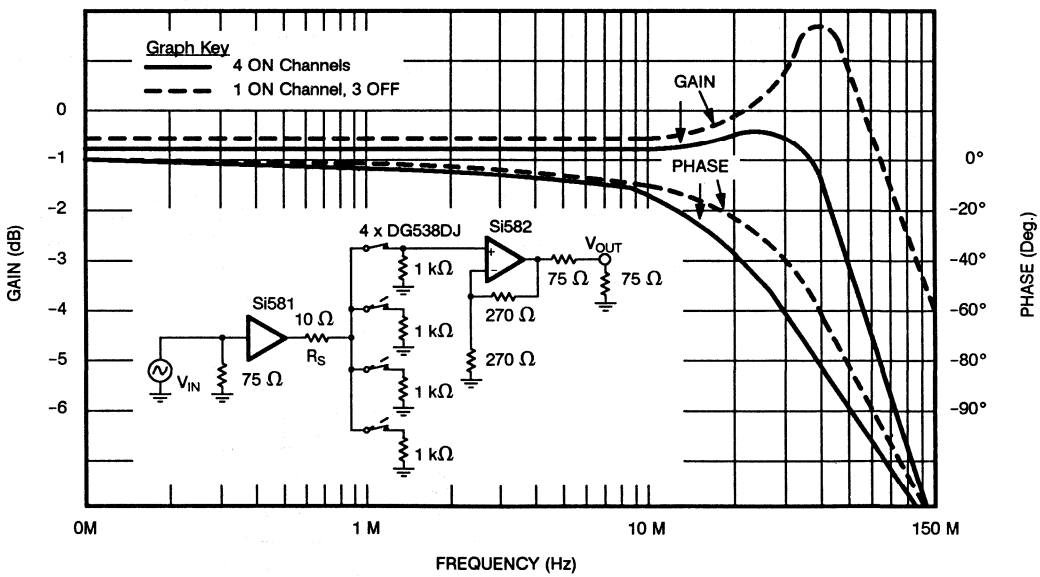

Figure 27. Frequency Response of Four DG538s Buffered with Si581 and Si582

The output amplifier (Si582) provides a gain of two, again for correct matching, since the 75 Ω output impedance driving a 75 Ω load gives a two to one division of the signal. Note that the non-inverting input to the Si582 is padded down to 1 kΩ to optimize switch bandwidth. It is feasible that reduction of this value could be employed to further increase switch bandwidth, although more output gain might then be required to compensate for losses, which in turn causes a reduction in the Si582 bandwidth. Circuit optimization would normally be practically performed in preliminary design stages.

The graph shows that even with worst case loading (i.e. 4 channels "on") the gain flatness and phase shift is well within the required limits of even the most demanding video standards.

It is conceivable that even more outputs could be driven by a single Si581, especially in less demanding applications.

Alternatively, discrete input buffer designs such as source or emitter follower circuits that require only a transistor (FET or bipolar) plus a few passive components could be used for front-ends, although the cost versus performance ratio is questionable, since the performance reduction could necessitate every individual DG538 channel buffered. This obviously increases component costs, board real-estate and power supply requirements.

Follower circuits can be as simple as shown in Figure 28 for certain applications. This circuit exhibits a dc offset which can be removed using the dc restoration (or black level clamp) circuit of Figure 30. This arrangement of buffering and clamping is used for capacitively coupled systems.

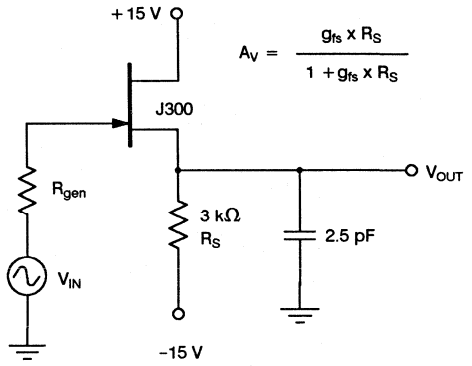

Figure 28. Single FET Source Follower

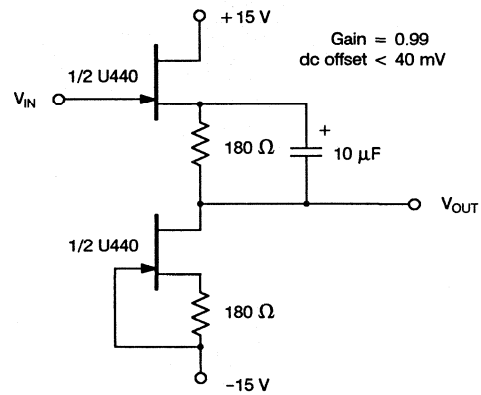

Figure 29. FET Buffer Uses Matched JFETs for Low dc Offset

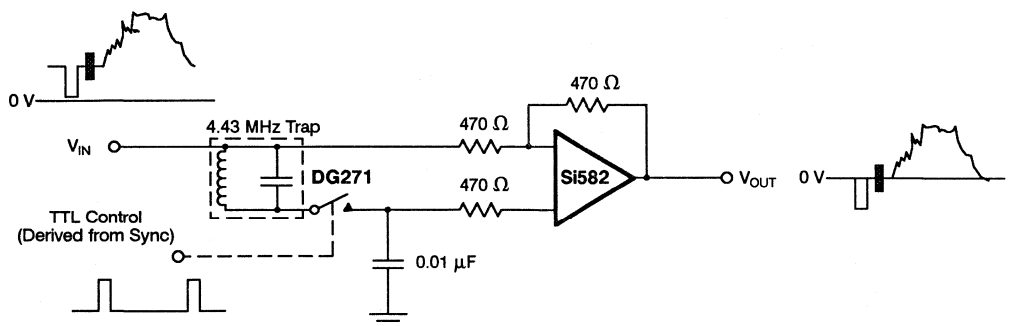

Figure 30. Simple Black-level Clamp Circuit

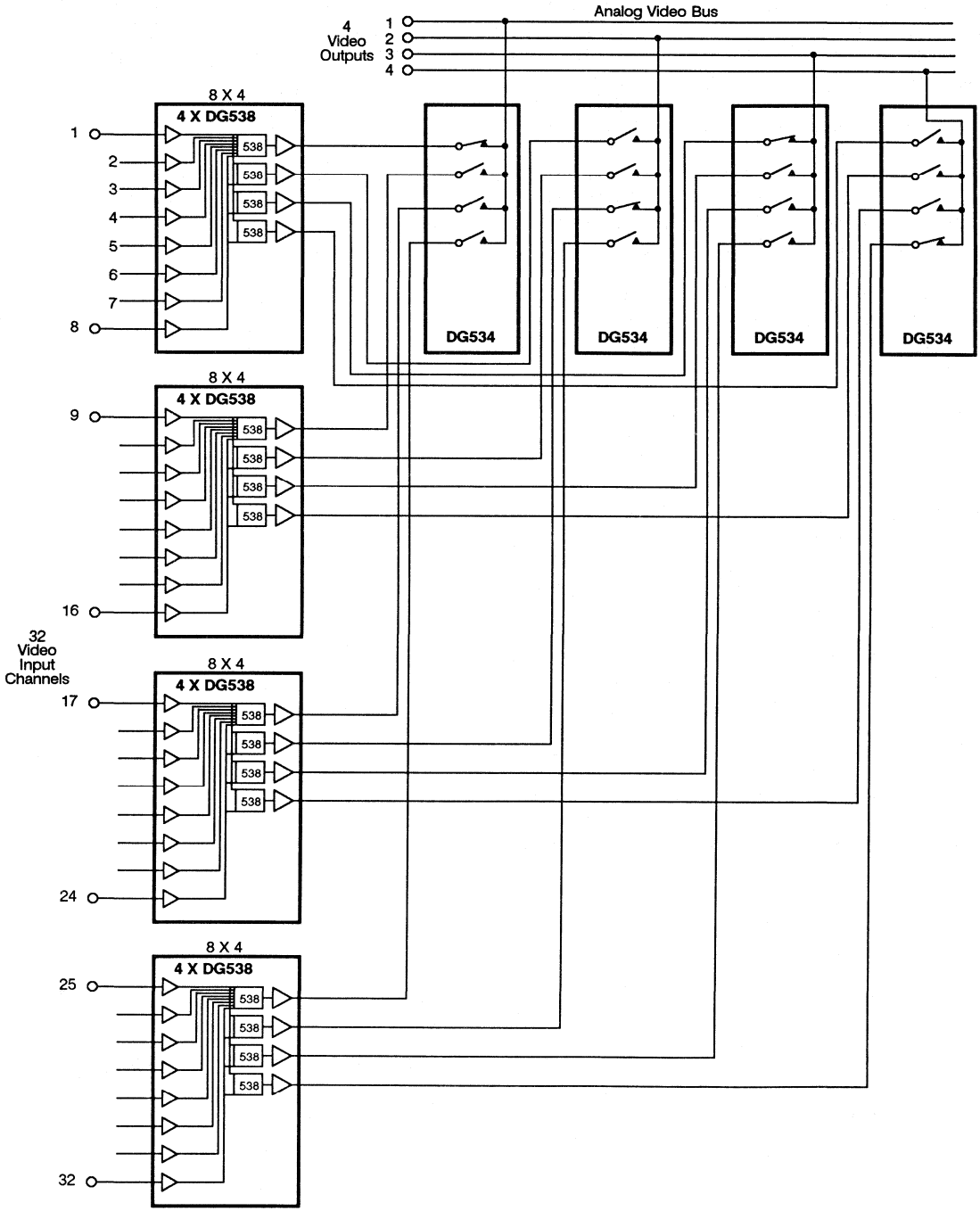

Figure 31. 32 X 4 Crosspoint with Bus Isolation

Some applications might demand a dc-coupled system that retains all the dc contents of the signal applied to the buffer. For these applications, the follower circuit shown in Figure 29 may be used. This circuit, which exhibits a low dc offset of < 40 mV, uses a Siliconix U440 dual FET to maintain simplicity and efficient use of board space. Lower offsets can be accomplished by using monolithic buffers such as Siliconix' Si581.

In the circuit shown in Figure 28, $f_{-3\ dB} \approx 300$ MHz for $R_{gen} = 75\ \Omega$, while offering a low input capacitance. The output signal for this circuit has some dc offset; however, this is not usually a problem because the output of the matrix is frequently ac coupled with a dc restoration (black-level clamp) circuit employed at a later stage. Figure 30 shows a simple black-level clamp circuit that employs a DG271 high-speed analog switch.

Figure 31 shows a large 32 x 4 crosspoint matrix. It is frequently better, in terms of system flexibility, to use a smaller crosspoint card (e.g., 8 x 4) as the basic building block. This 8 x 4 card must be designed to allow expansion of the total number of inputs or outputs required by the system.

Assuming each card has eight input buffers (Si581) and four output buffers (Si582) as shown, expansion of system outputs is easily accomplished by paralleling the inputs to the switch cards. Since each card has all its inputs buffered, many cards may be connected to provide multiple outputs without producing significant loading on the signal sources. However, expanding the number of system inputs is more difficult. Each card output has a low output impedance Si581 ($\approx 2\ \Omega$) that prevents simple paralleling, which would greatly overload the analog video bus. By using DG534 devices in a 4-to-1 mode as a submultiplexing configuration, as shown in Figure 35, each line of the video bus sees only one card output at a time.

Figure 32 shows a method for transmitting dc power down the video coax. This system can be adopted in remote switching locations where a power source is not available or in hazardous industrial environments where mains-derived power supplies are not permitted. Alternatively, this technique could be adopted in a cable TV application, where the channel switcher or selector could be powered from the incoming video lines. The dc power is coupled to the video coax lines using a 1 mH choke, and it is isolated or removed from the video signal using the capacitors (C_1, C_2, and C_3).

Another popular video-signal manipulation application is digitally controlled gain or attenuation circuits. For example, digitally controlled gain may be required for level trimming different video channels to be switched to a single processing path.

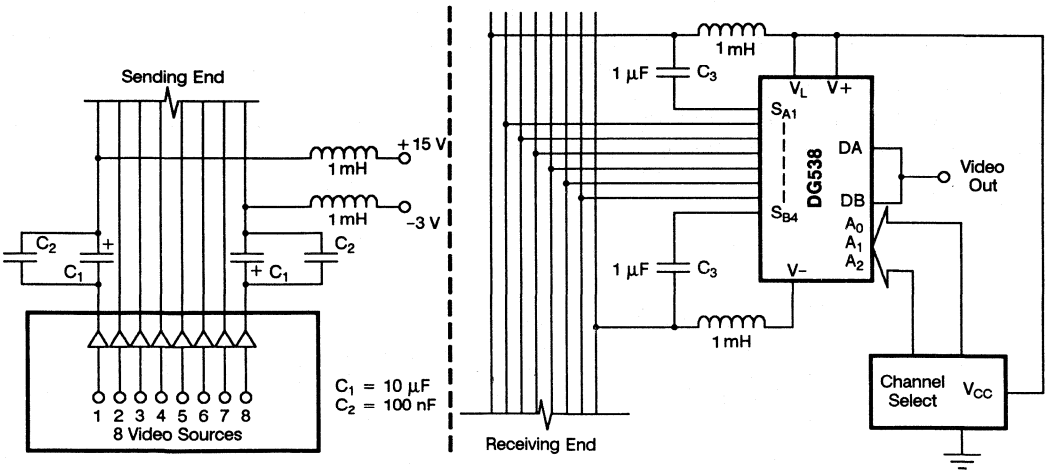

Figure 32. Phantom-Powered Remote Video Switch

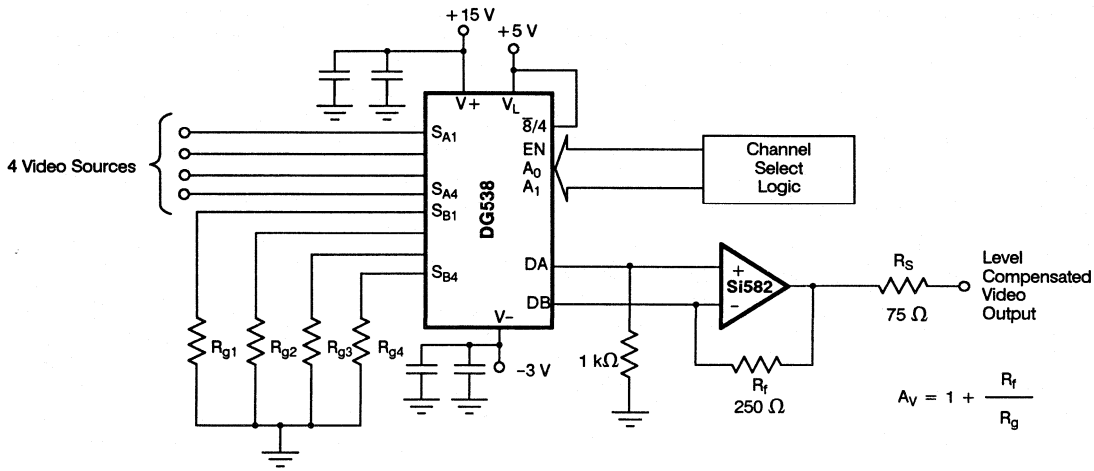

Figure 33. Programmable Gain Video Selector

Figure 33 shows a DG538 in a dual 4-by-1 arrangement designed to switch four video sources while providing level compensation and/or gain for each using an Si582 wideband op-amp. Note that this circuit has a fixed feedback resistor with R_g switches rather than the more usually adopted reverse. This is due to the fact that the Si582 is a current feedback op-amp. Generally, the devices give a different frequency response for different values of feedback resistor.

Data Acquisition Front-End Applications

A typical data acquisition system comprises front-end sensor stages followed by signal conditioning stages. The analog sensor signal, after being amplified and filtered, is sampled and digitized using a sample-and-hold circuit and an analog-to-digital converter. The digitized signal is then processed, usually under microprocessor control.

Usually, many analog channels must be processed. Due to the high cost of signal-conditioning, fast sample-and-hold, and flash analog-to-digital converter components, it is more feasible to employ a front-end multiplexer so that each channel can be processed in turn.

The circuit shown in Figure 34 uses a wideband multiplexer for accurate manipulation of the high-frequency input signals. The "user friendly" control and microprocessor-interface features of the DG538, combined with its proven high-frequency signal handling, make it ideal for this circuit.

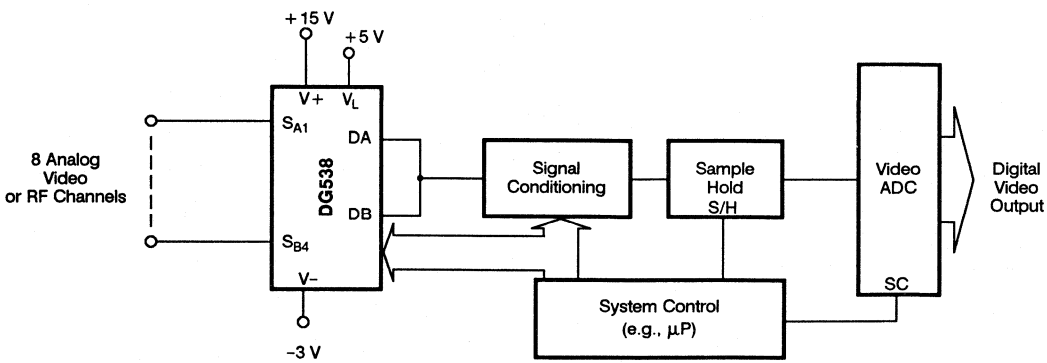

Figure 34. A Basic Multi-channel Video/rf Processing Circuit

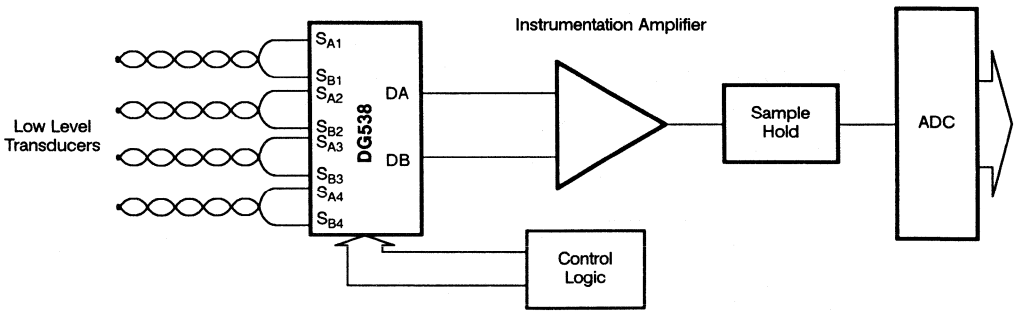

Figure 35. A High-accuracy Low-level Signal Processing System

The DG534 and DG538 are also effective devices for switching low-level signals. Commonly, data acquisition systems monitor a number of sensor signals that could be the output of various temperature, pressure, or vibration transducers. Generally, these are low-frequency (often dc), low-level signals. Thermocouples, for example, typically have millivolt outputs with tens of μV/°C resolution. To accurately monitor small temperature changes, the multiplexer must not introduce any dc offset or noise. Since the circuitry must handle small signal levels that are prone to noise/mains pickup, digital crosstalk, etc., apply the same layout rules used for high-frequency designs, such as sufficient grounding and shielding.

The DG538, with its interchannel ground pin and symmetrical on-chip layout, improves circuit accuracy. A differential signal handling system is an established means of low-level transducer interfacing. This system rejects noise pickup, switching transients, and metallic junction dc offsets as common-mode signals. A highly accurate low-level transducer interface circuit using a DG538 in its differential mode is shown in Figure 35.

Data Acquisition System Signal Conditioning

Before sampling and digitizing, an analog signal frequently requires "cleaning up" and ranging, a process known as signal conditioning. System front ends will invariably pick up unwanted signals. Signal carrying leads often pass areas that superimpose mains hum, radio-frequency interference, or digital noise on the analog signal to be processed. A well-designed and balanced differential twisted-pair system, such as the one illustrated in Figure 35, will minimize these common-mode signals.

Filtering

Filter circuits are widely used in the signal conditioning stage. Most often, they take the form of low-pass, high-pass, or band-pass configurations that remove unwanted signals outside the required bandwidth. Figure 36 shows a general configuration for an active first-order all-pass circuit that can be used for providing a digitally controlled variable-phase shift, where the phase shift is given by

$$\beta\ (\omega) = 2\tan^{-1}\ \omega RC$$

and the delay is found from $t_d = \dfrac{2\ RC}{(\omega RC)^2 + 1}$

Note: $-\omega C = 1/RC$ = cut-off frequency. For constant delay, $\omega < 0.1$ RC.

The circuit shown in Figure 36 may be employed as a phase correction system to equalize phase delays associated with different signal paths. A video crosspoint, for example, will exhibit a varying phase delay due to changing load capacitance on the transmission path when a single input connects to between 1 and n outputs (Figure 25).

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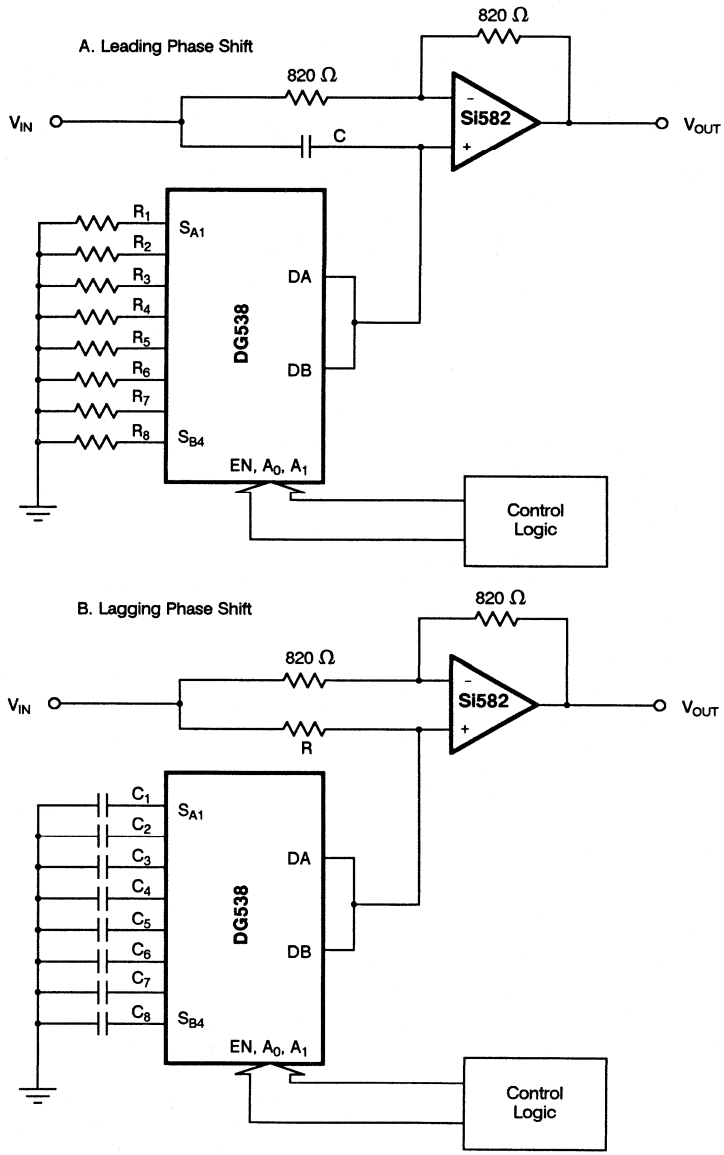

Figure 36. A Digitally Controlled Phase Shifter

Conclusion

This application note has provided information for video, audio, and data acquisition switching system designers. Using the DG534 and DG538 microprocessor-compatible multiplexers from Siliconix simplifies the design task and improves system performance.

THE DG535/536 WIDEBAND MULTIPLEXERS SUIT A WIDE VARIETY OF APPLICATIONS

Gareth Powell
Revised June 1989

INTRODUCTION

Analog switch IC's traditionally have found limited use in applications involving high-frequency analog or digital signals. Degradation of switch performance and intolerable signal cross-talk between channels has undoubtedly forced many designers to use bulky electromechanical switches or costly discrete designs.

At best, analog switch ICs configured in L or T arrangement could be adopted. However, increased board space and layout complexity became major problems in configuring systems with high channel density.

The DG535/536 are compact 16-channel, single-ended multiplexer ICs, primarily designed as a cost-effective solution to video and wideband switching problems. Other applications that benefit from the devices' superior performance characteristics are:

- Digital switching
- Audio Switching
- PCM routing networks
- ATE systems
- High-channel-density multiplexing or demultiplexing systems
- High-speed multiplexing systems
- Low-level signal multiplexing

PRODUCT DESCRIPTION

A functional block diagram of the DG535/536 is shown in Figure 1 and the switch configuration is shown in Figure 2. The device is fabricated using self-isolated, silicon-gate D/CMOS technology. This process enables the logic interface and driver circuitry, the gating and latching stages, and the switching elements to be combined in a monolithic structure.

Ease of design for large switching matrices and interface with microprocessors is accomplished with comprehensive logic gating and latching functions available on the chip. The DG536 is housed in a small, 44-pin J-lead package, thus minimizing board size requirements. The DG535 is packaged in a 28-pin DIP. Chip select pins (CS and $\overline{CS}$) permit easy stacking of devices for multi-channel multiplexing systems (see Applications Section, Figure 19).

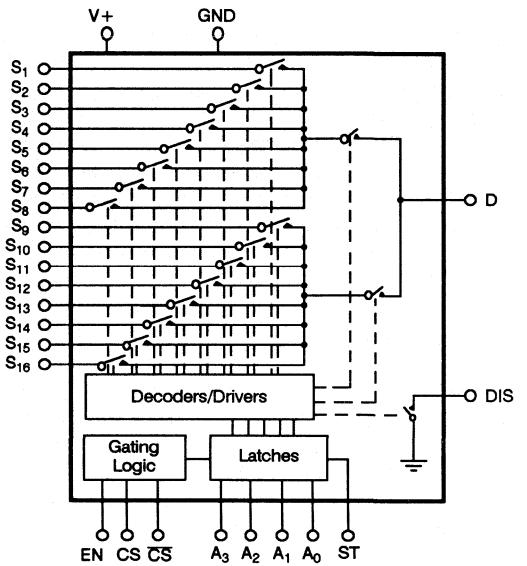

Figure 1. DG535/536 Functional Block Diagram

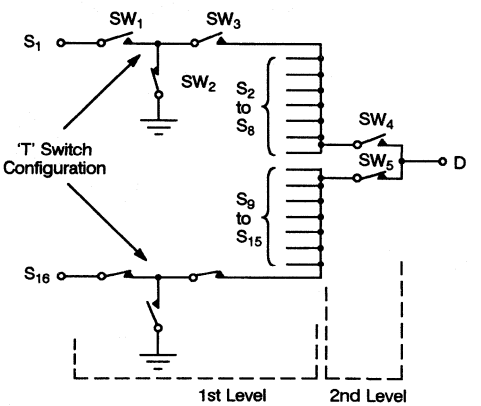

Figure 2. Switch Configuration

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An additional feature, a DIS pin, is an open drain terminal with the source tied to the device substrate. The DIS terminal represents a high impedance to the substrate (normally ground) when the DG535/536 is disabled and a low impedance to ground when the DG535/536 is enabled. This output can be used to indicate which device in a large matrix has been enabled (see Figure 18), or it can be used to switch off circuitry following the multiplexer stages.

MINIMIZING PARASITIC EFFECTS

The insertion loss and bandwidth of the switch are improved with DMOS transistors that offer a low on-resistance and low intrinsic capacitance (see Siliconix SD5000 data sheets). On the DG536 channel-to-channel crosstalk is minimized by physically separating each input channel with a GND pin which extends to the device substrate. This, in conjunction with careful PC board layout (see Figure 11), can yield channel-to-channel crosstalk figures better than -92 dB at 5 MHz.

Further ac performance benefits are obtained through the n-channel DMOS transistor T configurations (Figure 2). This maximizes the off-isolation, since SW_2 provides a shunt path to ground for any signals fed through the parasitic capacitance associated with SW_1. SW_3 (working in phase with SW_1) provides an extra stage of off-isolation and prevents the shunt switch (SW_2) from affecting consecutive channels.

TWO-LEVEL SWITCHING

The two-level switching system of the DG535/536 (SW_4 and SW_5) works in antiphase, effectively isolating half of the switch outputs from the drain (output) of the multiplexer. These series switches serve several functions:

- They provide an extra stage of off-isolation.
- They reduce the drain output capacitance significantly and increase the multiplexing transition speed.
- They reduce the off-leakage current, which reduces the offset voltage that develops from the total off-leakage current flowing through the load resistance and/or switch ON-resistance. This enables lower analog signal levels to be handled accurately.

SILICON GATE

Polysilicon is used as the transistor gate material for the DG535/536, as opposed to more conventional metal-gate designs. This technology minimizes the charge coupling of the control-logic signals to the switch output due to the self-aligning properties of the process. Metal-gate technology relies on photolithographically aligning the gate metal with the channel diffusions, resulting in greater overlap tolerances.

As shown in Figure 3, a PN junction exists between the p-type substrate and then n-type channel diffusions. This junction should not become forward biased by the analog signal going more negative than the substrate potential (normally ground).

Device damage could result from the current flow through the forward biased substrate-channel junction, exceeding the aluminum current handling capacity (i.e. 20 mA). Analog signal dc biasing or offsetting the device power supplies can prevent this problem. These methods are discussed in the applications section of this paper (Figure 12 and Figure 13).

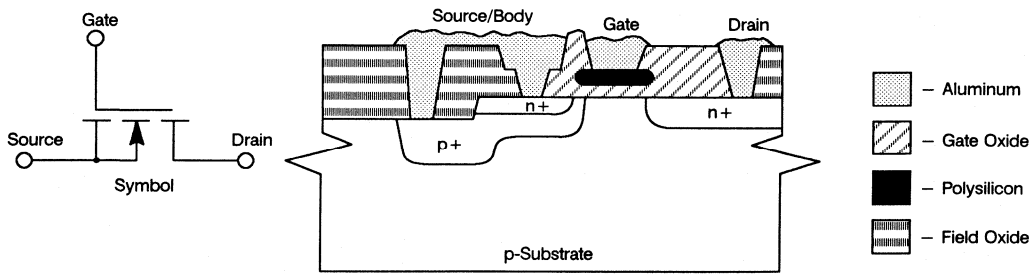


Figure 3. Cross-section of an n-channel, Silicon-gate DMOS Transistor

DG535/536 DC CHARACTERISTICS

ON-resistance

ON-resistance must be low to ensure low insertion loss, especially when the switch drives low load resistances. As shown in Figure 3, the ON-resistance remains low and fairly constant over the usable analog signal range. This makes the DG535/536 useful for audio applications that require low harmonic distortion.

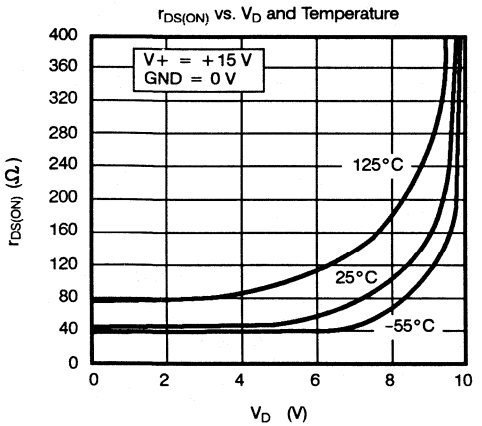
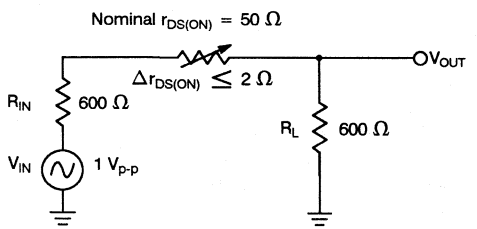


Figure 4. ON-resistance vs. Analog Signal Characteristics



$$\text{Insertion Loss} = 20\ \text{LOG}_{10}\ \frac{V_{OUT}}{V_{IN}}$$

Figure 5. 600 Ω Audio System

In a 600-Ω audio system, such as the one represented in Figure 5, the percentage of ON-resistance change relative to the load resistance is only 0.33%. The insertion loss due to the switch ON-resistance is 0.7dB.

Leakage Current

The DG535/536 features low OFF and ON leakage currents, reducing low switching errors.

Power Supply Current Consumption

Until now, most available video multiplexers or digital crosspoint switches relied on high-level supply currents for operation. The DG535/536 requires a total supply current of only 5 μA, typical. This feature makes the DG535/536 ideal for systems with high channel density, such as 32-channel crosspoint matrices used in video mixing consoles or as ECL digital crosspoint replacements in large data transmission systems.

The total supply current for a 32-channel crosspoint system using the DG535/536 is approximately 320 μA, much lower than other video multiplexers.

DG536 AC CHARACTERISTICS

(Refer to the DG535 data sheet for the 28-pin DIP performance.)

Bandwidth

This "ON" frequency response, as shown in Figure 6, is expressed as the frequency at which the insertion loss (at dc) increases by 3-dB. The measured bandwidth of the DG536 is greater than 300 MHz.

Crosstalk

Crosstalk is the amount of unwanted signal apparent at a particular node due to the parasitic capacitance of the device. As the most important parameter for many applications, crosstalk is specified in a number of ways.

1. **Single-channel crosstalk** (Figure 7) is the ratio of the signal seen at the drain (output) to the signal applied to a single OFF-channel input. This is expressed by

$$\text{XTALK}_{(SC)}\ (\text{dB}) = 20\ \text{LOG}_{10}\ \frac{V_{OUT}}{V_{IN}}$$

Most conventional multiplexers specify this parameter on the data sheet as off-isolation. This value for the DG536 is more than twice as good as other 16-channel analog multiplexer ICs, proving the effectiveness of the T switch.

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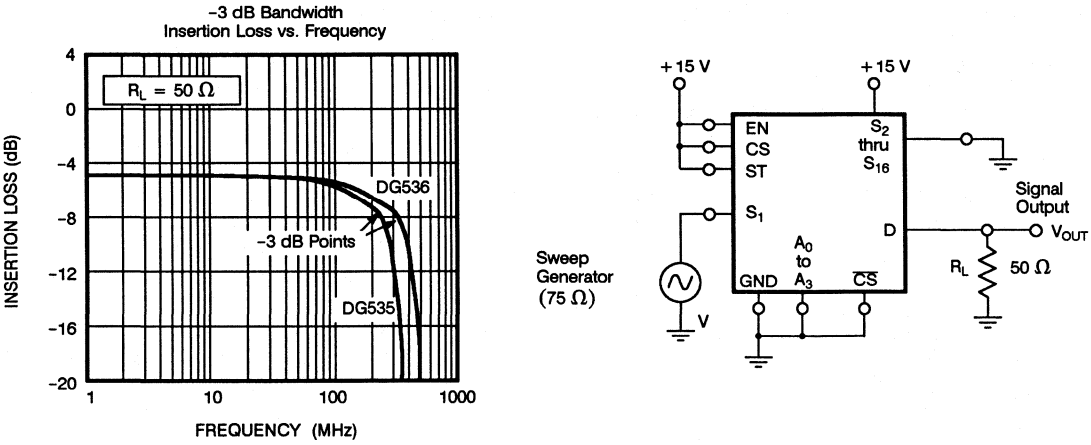

Figure 6. Bandwidth

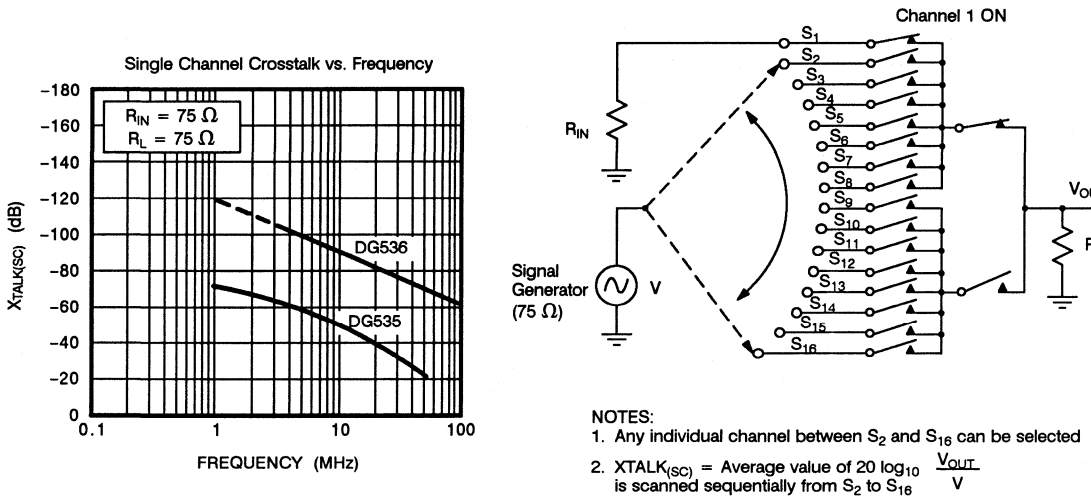

Figure 7. Single-channel Crosstalk vs. Frequency Graph and Test Circuit

2. **All hostile crosstalk** (Figure 8) is the ratio of the signal measured at the drain to the signal applied simultaneously to all 15 channels (i.e., with one channel ON).

3. **Chip-disabled crosstalk** is the drain output to signal input ratio. The input signal is applied to all 16 off channels simultaneously.

4. **Adjacent input crosstalk** (Figure 10) is the ratio of the signal applied to a source (input) to the signal measured at any adjacent source. A low adjacent input crosstalk is required for video applications to avoid ghosting effects that may appear on video monitors or TV screens.

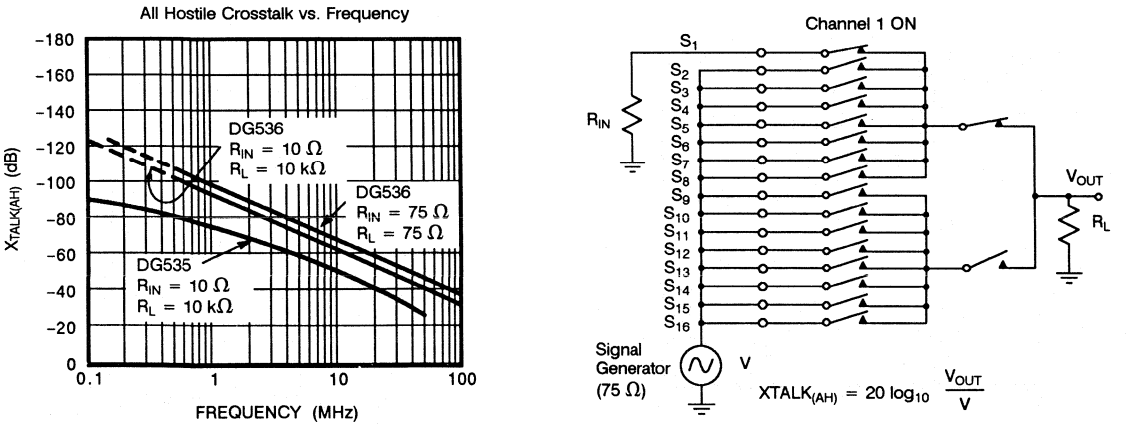

Figure 8. All Hostile Crosstalk vs. Frequency Graph and Test Circuit

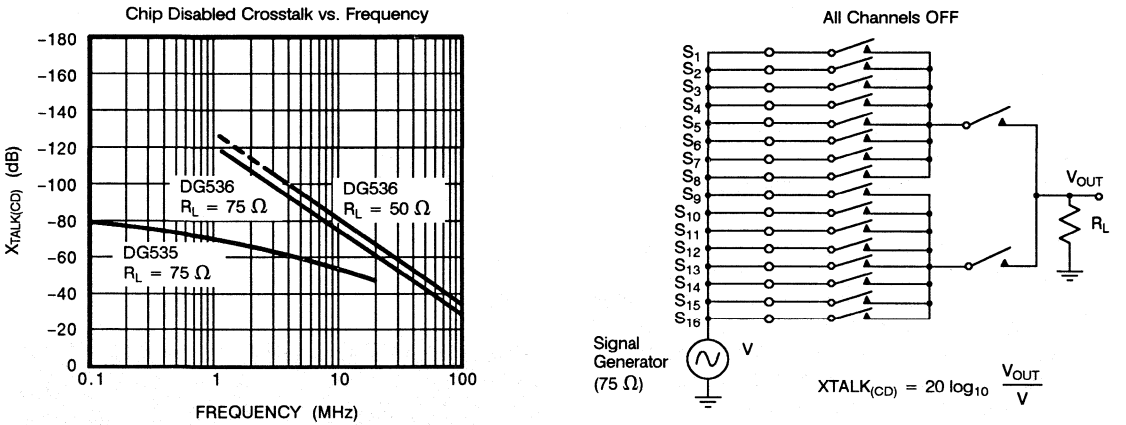

Figure 9. Chip-Disabled Crosstalk vs. Frequency Graph and Test Circuit

Switching Time

The DG535/536 switching time enables use of the device at high multiplexing rates. The low transition times (t_{ON} = 300 ns maximum and t_{OFF} = 150 ns maximum) make it ideal for fast multi-channel analog or digital multiplexing.

True break-before-make (BBM) switching action is guaranteed by design. This prevents shorting (crosstalk) of time adjacent input channels during transition.

Capacitance

Capacitance determines the loading effect of the multiplexer on signal sources and affects transition times, as well as system bandwidth.

1. **OFF-state input capacitance** gives the loading of the device (in the OFF-state) to a signal source. With a typical value of 2 pF, this allows efficient paralleling of many device channels in multi-channel crosspoint matrices with negligible loading effects.

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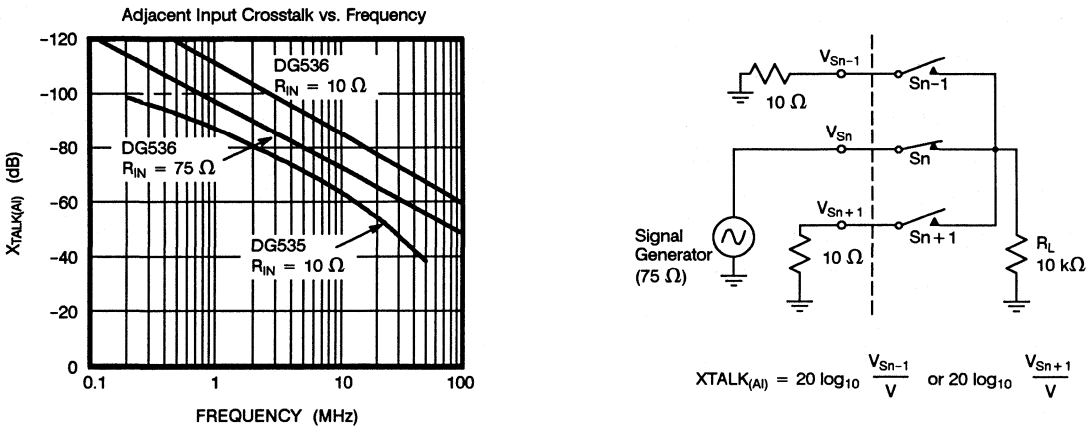

Figure 10. Adjacent Input Crosstalk vs. Frequency Graph and Test Circuit

2. **ON-state input capacitance** also determines the loading effects of the device ON-signal sources and limits the number of parallel on channels allowed in a large matrix. In large matrixes buffering of the input signals is recommended.

3. **OFF-state output capacitance** affects the transition speed of the multiplexer. The output capacitance must be charged and discharged in turning on and off a device; thus, a low value of capacitance enables rapid transition times. Table 1 shows a comparison of DG536 capacitance to comparable 16-channel multiplexers.

CIRCUIT BOARD LAYOUT

To optimize the high-frequency characteristics of the DG536, care must be taken in circuit board layout and interconnections. Parasitic stray capacitances caused by poor layout could degrade performance significantly. As shown in Figure 11, use of guard planes and traces between signal paths is a good layout practice. Other layout considerations include:

- short signal paths
- sufficient power supply decoupling
- coaxial interconnect of leads, plugs, and sockets.
- sockets should be avoided

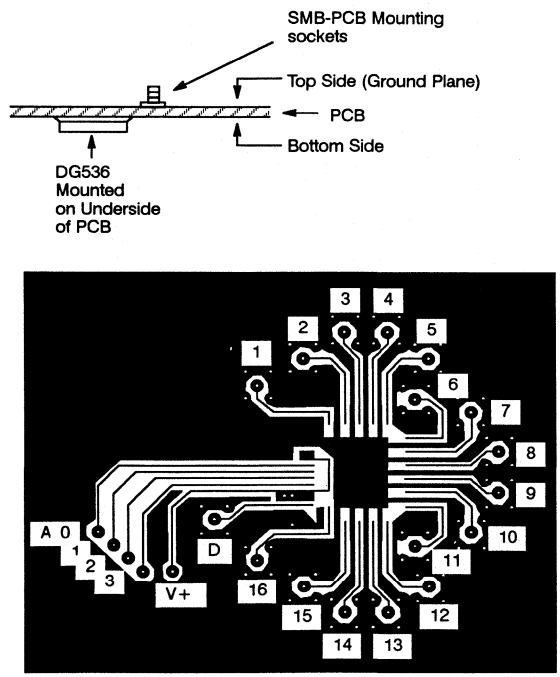

Figure 11. Circuit Board Layout for Optimal Performance (DG536)

TABLE 1. Capacitance Value for 16-Channel Multiplexers

Parameter	DG526	DG506A	DG508A	CD4051/2/3	DG536
$CS_{(OFF)}$ (pF)	10	6	5	10	2
$CD_{(OFF)}$ (pF)	65	45	25	60	8

NOTE: These are typical values taken from data sheets.

APPLICATIONS

Many applications for the DG535/536 will be in video related systems. Some examples of circuit configurations are included in this section.

VIDEO

The DG536 was designed primarily for handling broadcast quality video signals. Optimum performance is achieved with a bias between +2.5 V and +3 V. Differential phase linearity is best at this bias level.

A general-purpose 16-channel wideband multiplexer is shown in Figure 12. Dc biasing is achieved with the divider network R_1 and R_2. A wideband op-amp (Si582) is configured to give an inverting unity gain, while removing the +3 V dc by setting the voltage on the non-inverting input to +1.5 V dc. The use of trimpot R_7 and precision resistors allows accurate elimination of any dc bias. This arrangement results in faster multiplexing rates than capacitive decoupling while providing black-level clamping, impedance matching for 75 Ω loads, and greater drive for transmission stages, with no major compromise on signal quality (distortion, frequency response, etc.)

Alternatively, the device supplies can be offset to eliminate the need for 16 separate bias circuits. Such an arrangement, shown in Figure 13, could be used in a security system or in a remote industrial monitoring system. The DG535/536 positive supply and ground pins (at -3 V) should be heavily decoupled to the video camera ground connections.

The switching threshold of the device at a supply voltage of +15 V is approximately between +6 V and +8.5 V above the substrate potential (Figure 14). Since the substrate is held at -3 V, the effective switching threshold referenced to ground is between +3 V and +5.5 V. Thus, the device can still be controlled from CMOS logic signals (provided that the logic 0 (V_{AL}) is less than 3 V and logic 1 (V_{AH}) is greater than +5.5 V).

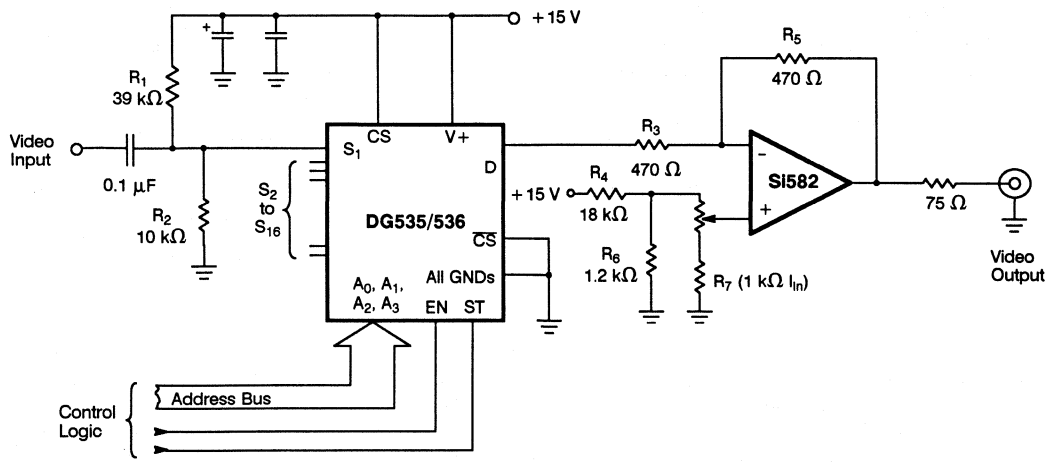

Figure 12. General-purpose 16-channel Wideband Multiplexer

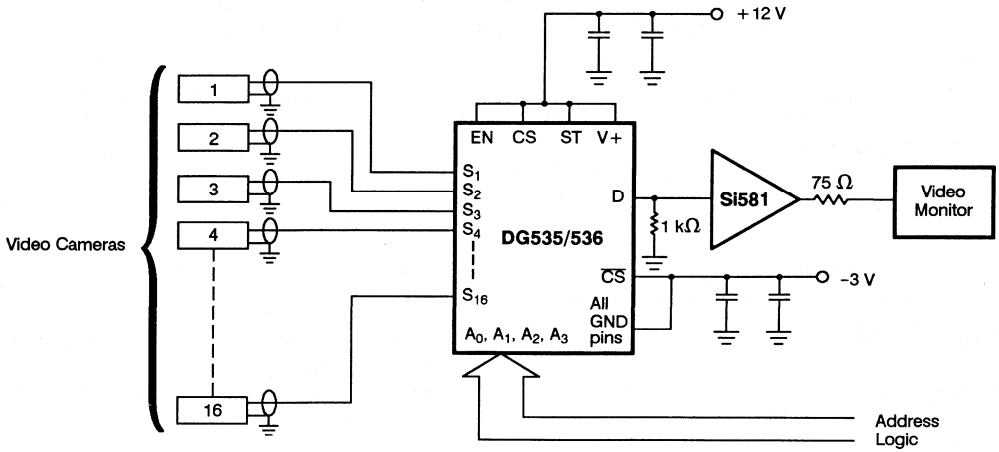

Figure 13. A Closed-Circuit Monitoring System

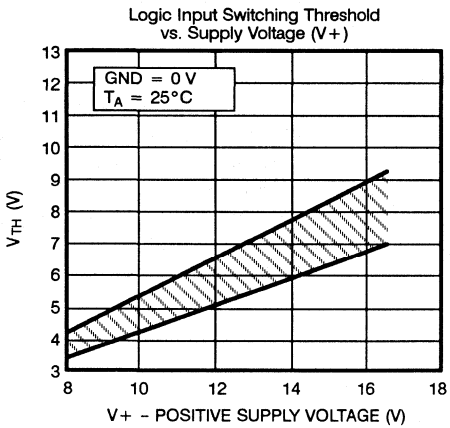

Figure 14. Logic Input Switching Threshold vs. Supply Voltage

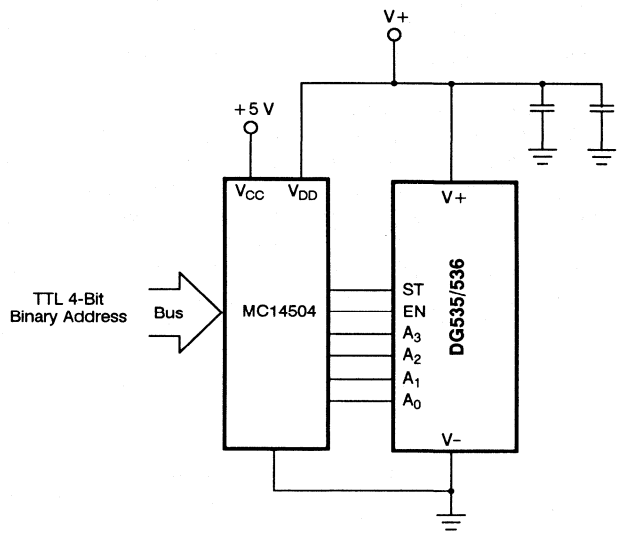

Figure 15. Using the MC14504 for Address Logic Level Shifting

In applications involving reduced supply voltages and offset conditions, the input switching threshold (V_T) may be reduced below the CMOS logic "0". This may cause the address inputs to appear permanently as logic "1" regardless of the control logic states. Therefore, control logic level shifting may be needed.

TTL to CMOS level shifting can be easily accomplished using inexpensive CMOS level shifters such as the MC14504 or CD40109.

CROSSPOINT SWITCHING

Many analog and digital systems, such as a central router used in a video studio console (Figure 13), require crosspoint switching functions. In this application, many channels route signals to many different outputs. Due to its small outline PLCC package and low power consumption, the DG536 leads itself easily to multi-channel crosspoint functions.

Figure 16 illustrates how the DIS (disable) pin can be used to indicate which output is selected. When logic 1 is applied to output select, device 1 is enabled and device 2 is disabled. With device 1 enabled, the DIS pin is connected to signal ground, thus turning LED 1 on. With device 2 disabled (due to $\overline{CS}$ being 1), its DIS pin represents a high impedance to ground and LED 2 is off.

Any one of sixteen inputs can be connected to either output. This is achieved by applying the appropriate CMOS logic address to the address inputs (A_0 to A_3) and applying the appropriate logic level to output select simultaneously.

The circuit in Figure 16 also illustrates how the chip select inputs can be used. As shown in Figure 17, a 32-channel single-ended multiplexer can be configured without external chip select circuits. This circuit makes use of the CS and $\overline{CS}$ inputs which allow device selection from a single control line.

The basic circuit shown in Figure 16 can be extended and elaborated to give a 16 x 16 matrix for video crosspoint applications such as central routers used in video studios. This circuit, shown in Figure 18, allows source (or video input) to be connected to any video output (or any number of outputs). The strobe input (ST) on each device is used to latch the appropriate address into that particular device. By strobing the required address into each device sequentially, any crosspoint connection can be made.

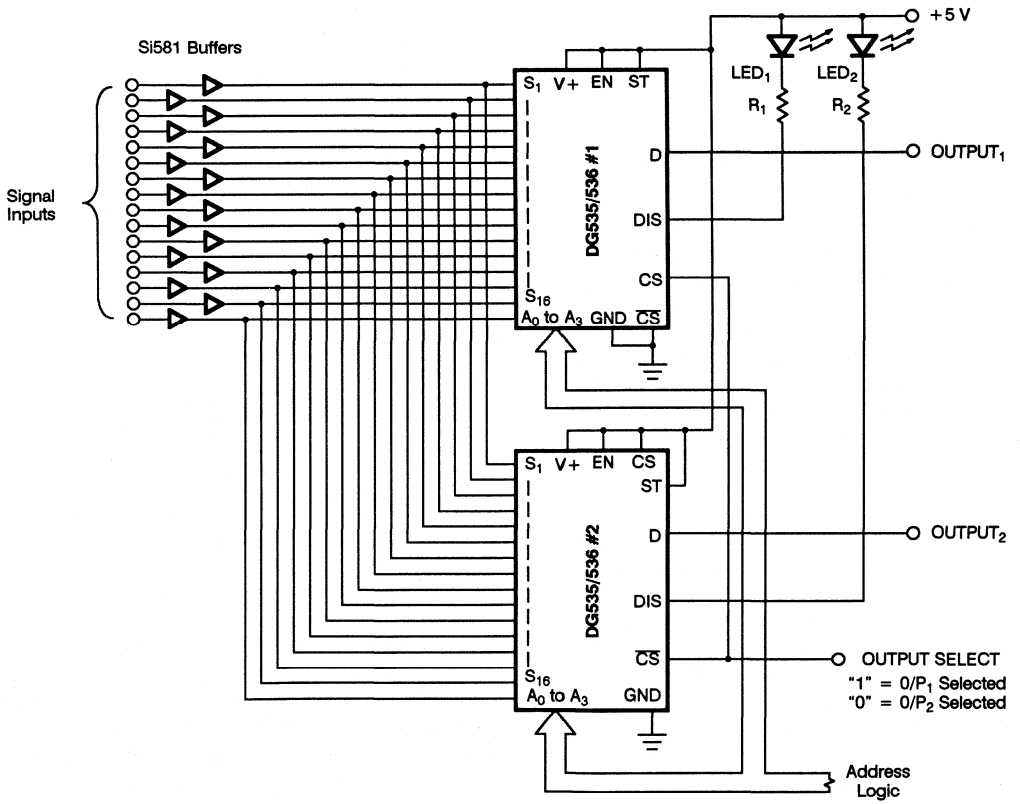

Figure 16. The DG535/536 as a 16 x 2 Matrix Switch

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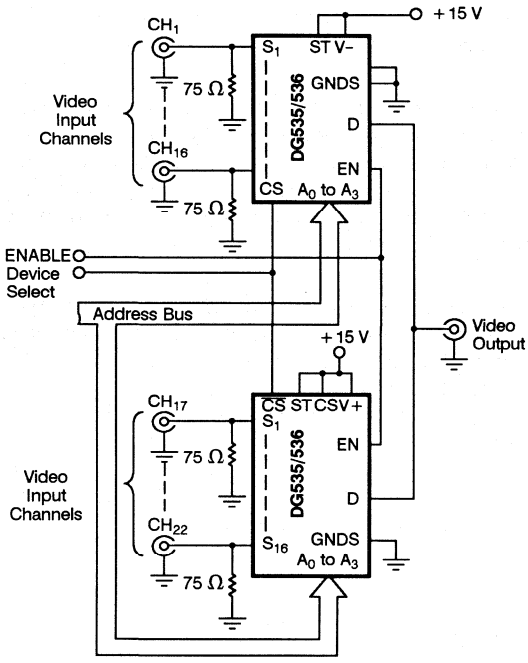


Figure 17. 32-Channel Multiplexer

The DG535/536 makes an excellent digital switch due to its low channel-to-channel crosstalk, high off-isolation, and wide bandwidth specifications. In digital data transmission systems, the DG535/536 can easily handle data rates in excess of 100 Mb/s.

The circuit shown in Figure 18 can be used as a digital cross-point to replace expensive, power consuming ECL crosspoint ICs. Besides handling raw digital data, the DG535/536 can also be used for other forms of data transmission, such as FSK and PCM systems.

FSK

Frequency shift keying (FSK), commonly used in data transmission networks, relies on representing the digital code with frequency sine wave bursts. An FSK multiplexing system block diagram is shown in Figure 19. Each digital level has a specific signal frequency. The DG535/536 can be used to multiplex 16 different digital channels into a single transmission line or into a transmitter. Similarly, a DG535/536 may be used to demultiplex the data at the receiving end. Since the device can manipulate higher frequency sine waves, data can be transmitted at a higher rate than with a conventional multiplexer.

PCM

A more commonly used and faster form of digital data transmission is known as PCM (pulse coded modulation). Used in telecommunications systems, PCM converts analog speech signals into 8-bit digital words for serial transmission. The data transfer rate used (for 4 kHz bandwidth voice signals) is up to 274.176 Mbps.

The DG535/536 can be used to route PCM signals in main telephone exchanges, replacing bulky hard-wired distribution frames. PCM highways can thus be rerouted remotely, under computer control, rather than manually.

RZ (returns to zero) PCM data consists of three discrete (ternary) levels to overcome long periods of zeroes (Figure 18). Digital signals can degrade beyond legibility after only a few hundred yards of travel down a transmission line. Therefore, the PCM signals must be regenerated at regular distances to avoid excessive distortion.

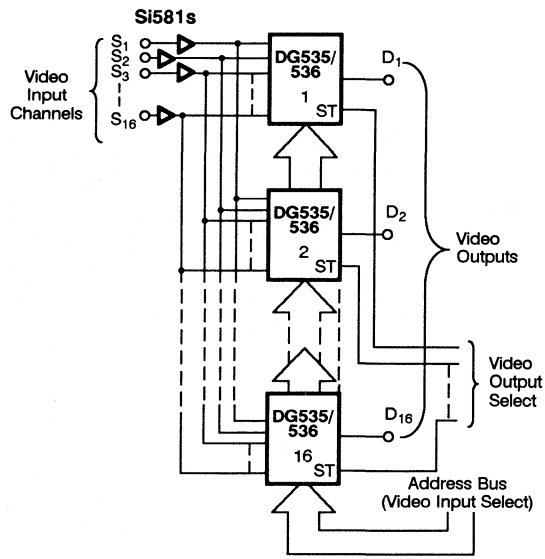


Figure 18. 16 x 16 Video Crosspoint Circuit

Figure 21 shows the architecture of a conventional binary distribution frame in a telephone exchange. Signal regeneration is applied to handle degradation during transmission and routing. Code converters are required to change the ternary PCM into binary PCM for routing within the distribution frame. Similarly, code converters are required to reconvert the binary PCM into ternary PCM for transmission.

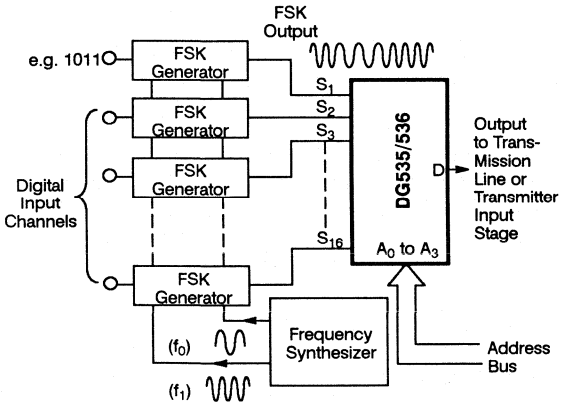


Figure 19. FSK Multiplexing System Block Diagram

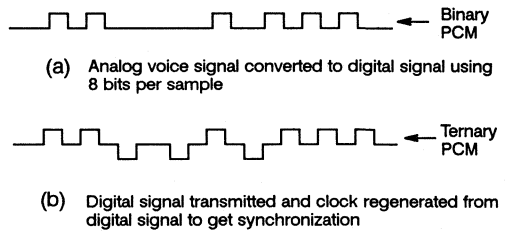


Figure 20.

Unlike digital switches which require specific digital signals, using the DG535/536 in the distribution frame (Figure 22) eliminates the need for code conversion and meticulous regeneration because it can handle analog signals.

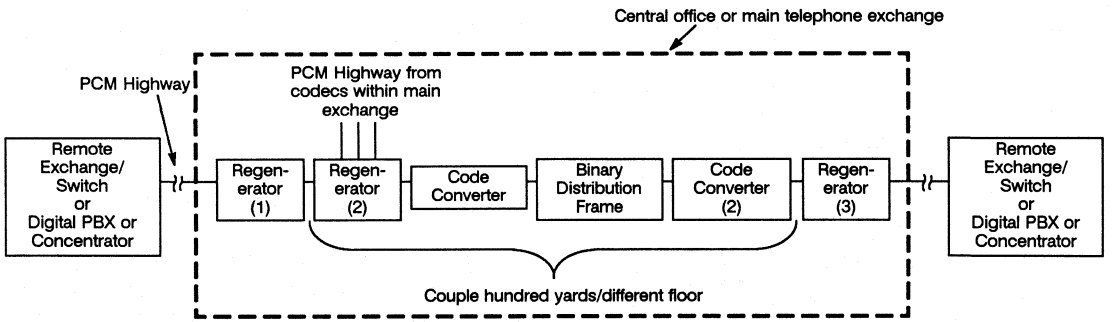


Figure 21. Binary PCM Routing Network

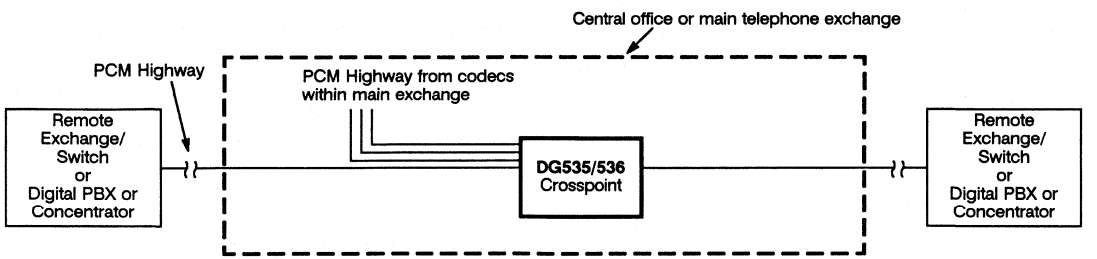


Figure 22. DG536 PCM Distribution Frame

PROGRAMMABLE GAIN VIDEO AMPLIFIER

The circuit shown in Figure 23 uses the DG536 as a binary gain select for a video/wideband op-amp (Si582).

The gain of the Si582 is set by:

$$A_V = 1 + \frac{R_f}{R_g}$$

For example, when R_f = 470 Ω, the results are

Table 2: Gains for the Circuit of Figure 23

Logic Input	R_g	Gain (A_V)
0000	47 kΩ	1.0
0001	4.7 kΩ	1.1
0010	2.4 kΩ	1.2
0011	1.6 kΩ	1.3

The low ON-resistance of the DG535/536 gives good gain stability, and the resistor tolerances mainly determine the gain error of the circuit.

The wideband qualities of the Si582 allows this circuit to be employed for digital level correction in any video systems including broadest quality specifications.

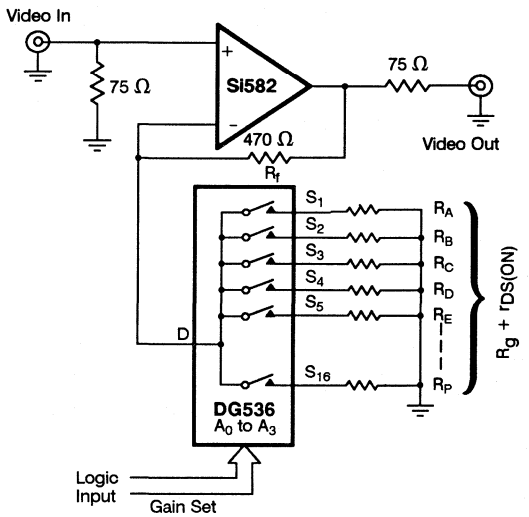


Figure 23. Programmable Gain Video Amplifier

ATE

A simple but accurate ATE system, as shown in Figure 24, can be designed for testing digital processing boards.

The propagation delay time for each of the 16 digital signal paths can be tested individually, with negligible errors due to the very small propagation delay through the DG535/536. Also, the variation of delay times from channel to channel is less than 0.25 ns.

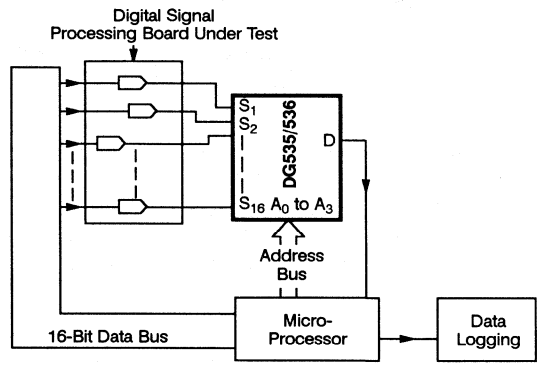


Figure 24. ATE Applications

MICROPROCESSOR INTERFACE

On-chip data latches in the DG535/536 simplify interface with a microprocessor data bus. This eliminates the need for peripheral memory devices (such as I/O ports or D-type latch ICs) to maintain switch addressing while the processor uses its data bus for other functions.

The data latches are activated by the DG535/536 strobe input (ST). The latch is transparent when ST= logic 1, thus the device responds to changes of data at the address inputs. When ST = logic 0, the previous data is latched into the device, regardless of new data appearing at the address inputs.

The DG535/536 timing arrangements meet the requirements of popular microprocessors, such as the 8085A, 6800, and Z80. The 8085A to DG535/536 interface is shown in Figure 25, and Table 3 illustrates the timing compatibility of the DG535/536 with the 8085A and the faster 8085A-2 devices.

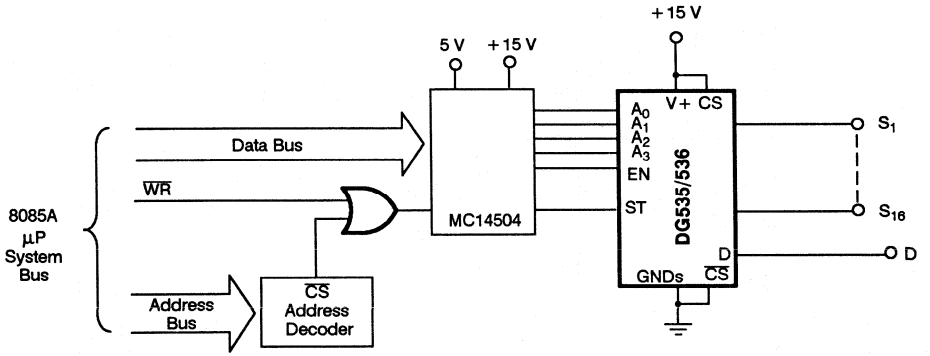


Figure 25. 8085A to DG535/536 Interface

Figure 26 shows the complete 6800 to DG536 interface circuit. In order to have a data valid signal, it is necessary to nand the R /$\overline{W}$/$\overline{CS}$ gate output with the Φ_2 clock (usually connected to the DBE pin). This makes the interface circuit functionally compatible with the 8085A interface shown in Figure 25.

Note that open collector gates and buffers could be used to level shift the TTL logic levels from the microprocessor to the CMOS levels required by the DG535/536 logic inputs.

To achieve the correct ST signal in a Z80 processor system, the $\overline{WR}$ and $\overline{MREQ}$ signals must be gated with the standard $\overline{CS}$ signal, as shown in Figure 27.

Table 3.
Timing Compatibility of the DG538/536 with Popular Microprocessors

Specification	8085A ns/min.	8085A-2 ns/min.	DG536 ns/min.
t_{SW} (strobe pulse width)	400	230	200
t_{DW} (data valid to strobe)	420	230	100
t_{WD} (data valid after strobe)	100	60	50

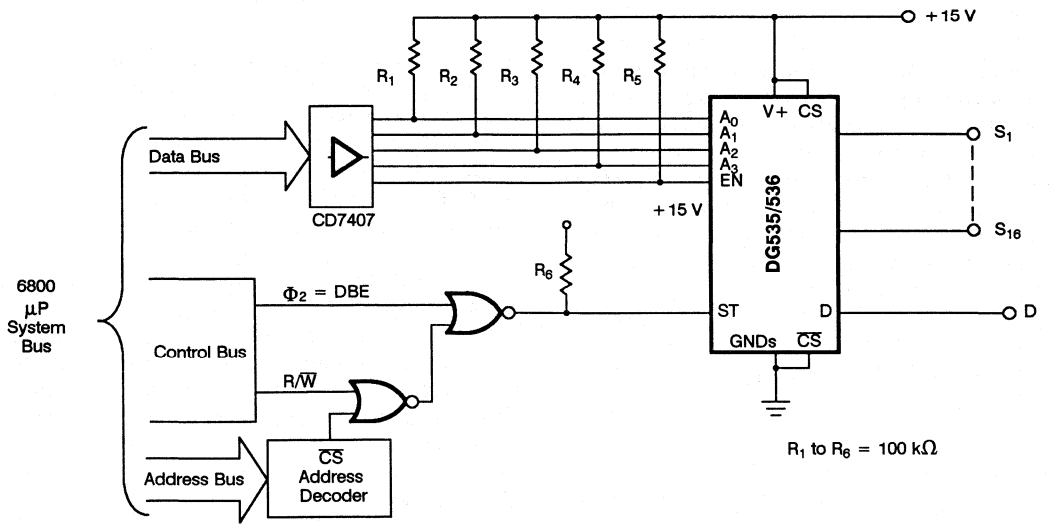


Figure 26. 6800 to DG535/536 Interface

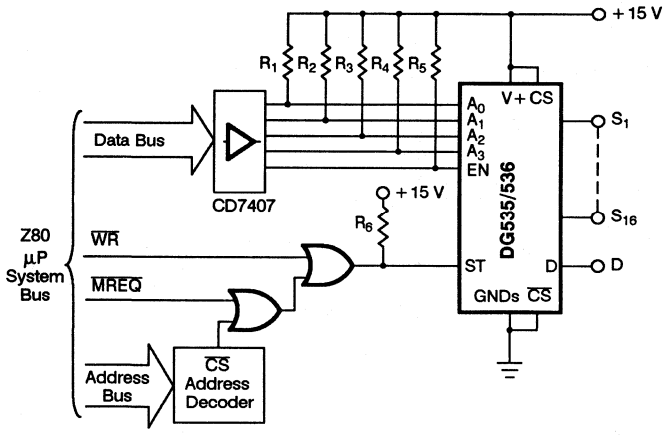


Figure 27. Z80 to DG536 Interface

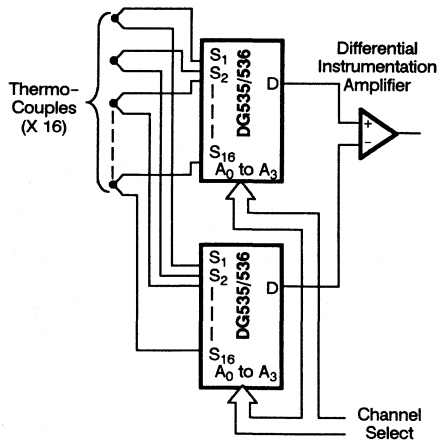


Figure 28. Thermocouple Multiplexing System

LOW ANALOG SIGNAL SWITCHING/MULTIPLEXING

The DG535/536 has several uses in handling low-level analog signals (such as in medical equipment or ultrasound transducer multiplexing) because the device exhibits inherently low noise and offset voltages. Two factors affect offset voltage:

1. Thermoelectric offset voltage is produced by the incidental thermocouples that exist within the integrated circuit. There are many intermetallic junctions within an IC. These junctions act as individual thermocouple has an identical reversed counterpart. That is, from source to drain, we have gold-aluminum/aluminum/aluminum-silicon and silicon-aluminum/aluminum-gold. Therefore, if the temperature surrounding each junction is constant and equal, the thermal EMFs cancel each other, giving a zero net offset voltage. Since a thermal gradient always exists across the chip, then there is always a net thermoelectric offset voltage. For the DG535/536, the thermal EMFs produced on chip are small since the device exhibits a low power consumption (75 µW), producing a low temperature on the die.

2. Leakage current offset is caused by leakage current flowing through the r_{DS} of an ON-switch and/or the load resistance.The offset voltage developed due to leakage current is negligible since the device has very low leakage currents (a benefit incurred by the two-level system) coupled with very low ON-resistance.

For example:

$$V\ (offset) = I_{D(ON)} \times r_{DS(ON)}$$
$$= \pm 100\ pA\ (typical\ @\ 25°C)$$
$$\times\ 55\ \Omega\ (typical)$$
$$= \pm 5.5\ nV\ (typically)$$

The circuit shown in Figure 28 can be used to remotely monitor up to 16 different thermocouples with high accuracy. The output of the thermocouples is in the form of a small dc voltage, on the order of millivolts, with typical voltage changes on the order of tens of microvolts per °C. Thus, voltage offset developed by the switching devices can frequently limit system accuracy.

Using the differential multiplexing technique shown in Figure 28, high resolution can be achieved since the thermal EMFs produced by each DG535/536 are canceled as common mode voltages at the instrumentation amplifier inputs. To minimize pick-up and noise effects, the same PC board layout rules apply for this type of circuit. Best accuracy is achieved by ensuring that the multiplexers are kept close together in a thermally stable environment.

THEORY AND APPLICATIONS OF THE Si7660 AND Si7661 VOLTAGE CONVERTERS

Doyle L. Slack
Revised February 1990

INTRODUCTION

Many times a simple digital circuit design can be greatly complicated by the needs of just one or two of the onboard devices. For example, analog devices often used along with digital circuits (such as op amps and data acquisition systems) are notorious for negative voltage requirements of −5, −10 or −15 V when everything else in the circuit needs only positive voltages. Until recently, the only answer was to either buy a dc-to-dc converter module (expensive) or redesign the power supply to generate the negative voltages (expensive and wasteful in parts count and space). This Application Note presents the best alternative to this problem: the Si7660 and Si7661 monolithic voltage converters. With the Si7660 and Si7661, negative voltages from 1.5 to 20 V can be generated from a positive supply with minimum parts count and minimum cost.

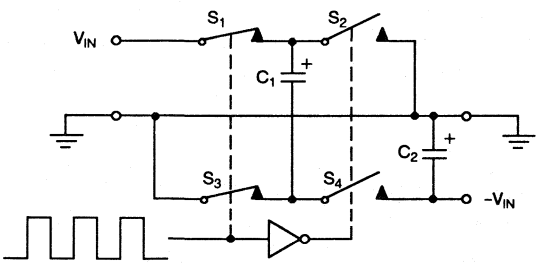


Figure 1. The Ideal Voltage Doubler

Theory Of Operation

The basic theory behind the Si7660 and Si7661 is the same and is based on the ideal voltage doubler shown in Figure 1. Capacitor C_1 is the pump capacitor, and C_2 is the reservoir capacitor. The pairs of switches (S_1 with S_3, and S_2 with S_4) are driven by an oscillator/toggle circuit, providing charge and transfer cycles of equal length.

During the charge cycle, S_1 and S_3 are closed, and current flows into C_1, charging it to the value of V_{IN}. The oscillator toggle then changes state, and the transfer cycle begins. S_1 and S_3 are opened while S_2 and S_4 are closed, allowing C_1 to dump charge into C_2 until the potential across them has equalized. The oscillator/toggle then switches again, and the process starts over.

For no load conditions, the voltage inversion will be virtually perfect since the amount of charge that must be transferred from C_1 to C_2 will be limited to losses due to leakage from C_2 and any parasitic capacitances. As the load increases, C_1 must transfer more and more charge to make up for the depletion of C_2 as it supplies current to the output during the charge cycle. This action causes the output voltage to drop, making the circuit appear to be a perfect inverter in series with an output resistor that varies in magnitude with the input voltage. Figure 2 shows this concept in a two port diagram of the device, and Figure 3 illustrates the typical output characteristics of both devices configured in the inverter mode.

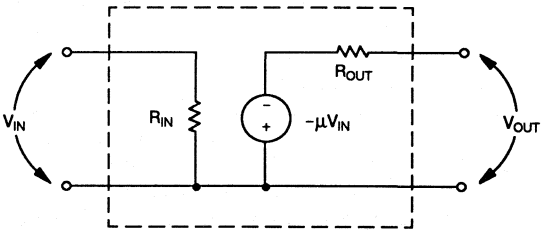


Figure 2. Two-Port Diagram of the Voltage Converter Circuit

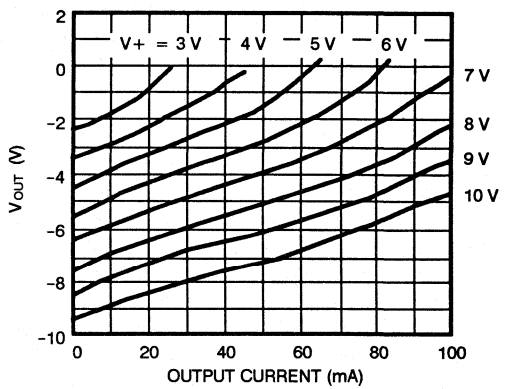


Figure 3(a). Output Characteristic of the Si7660 Voltage Converter.

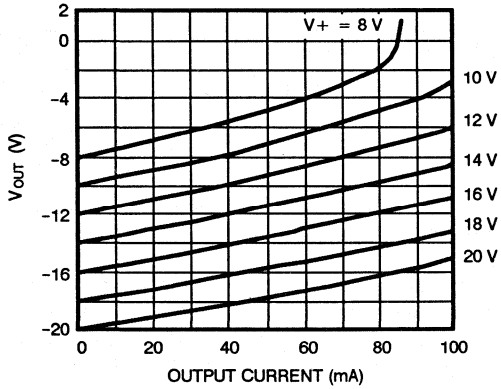


Figure 3(b). Output Characteristic of the Si7661 Voltage Converter.

Circuit Operation

With the Si7660 and Si7661, the only parts of the doubler not included inside the package are the pump and reservoir capacitors. The internal switches are made with p-channel and n-channel MOSFETs. The main difference between the Si7660 and Si7761 is the breakdown voltage of the MOSFETs which in turn dictates the maximum input voltage. Also, the design of the Si7661 offers a much greater resistance to device latchup, which is discussed later. Since the internal sections of the two devices are very similar, description of the operation of the Si7660 and Si7661 is combined. The internal sections of the circuit are the oscillator, divider, regulator, level translator, and substrate logic. Figure 4 shows a block diagram of the internal sections of the inverter circuit.

The oscillator supplies the signal to the divider section which in turn drives the rest of the circuit. The OSC input has an input impedance of approximately 1 MΩ. This allows the internal oscillator to be overridden by an external clock or to be slowed down by the addition of an external capacitor.

The internal regulator is a series voltage regulator with a zener reference to insure that low voltage components of the circuit are provided with no more than 5 V when the input voltage is greater than 5 V. It also provides current limiting for the oscillator and divider circuits. When the input voltage is less than 3.5 V for the Si7660 (less than 9.0 V for the Si7661), the LV pin is grounded, bypassing the internal regulator. However, when the Si7660 is operated above 3.5 V, the LV pin must be left open to provide latchup protection. For the Si7661, LV should be left open above 9.0 V for proper operation.

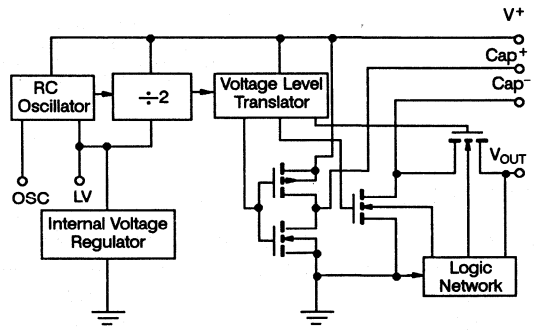


Figure 4. Block Diagram of the Voltage Converter Circuit

The divide-by-two counter provides complementary outputs. Q and $\overline{Q}$ drive the inputs of the level translators, which in turn provide the necessary switching voltages to drive the MOSFET switches. The built-in delay of the translators guarantees that break-before-make action occurs.

The substrate logic network insures that two things happen. First, it makes sure that the substrate-source/drain junctions of Q_3 and Q_4 are never forward biased, and that the ON-resistance of each of the output transistors will be as low as possible for all operating conditions. Second, the network determines the most negative voltage in the device and uses it to supply power to the level translator.

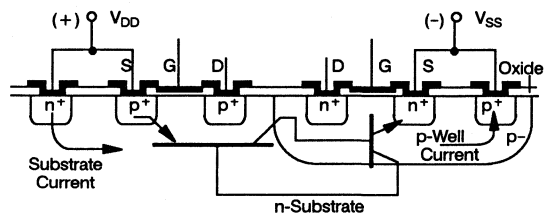


Figure 5. Intrinsic SCR Superimposed on a CMOS Gate Structure

Latchup

Because of the basic internal four-layer geometry of CMOS devices, an SCR action can sometimes occur. Figure 5 depicts the SCR structure. This SCR action can, under certain conditions, cause the Si7660 device to latch up. As Figure 5 shows, the source of the n-channel device becomes the SCR cathode; the source of the p-channel is the anode; and either drain can act as a gate. Since an SCR does not trigger until certain conditions occur, it can sometimes cause no problems at all, yet sometimes it may be fatal to the CMOS device.

The intrinsic SCR needs three conditions to cause latchup: the betas of the two parasitic transistors must be greater than one; the current flowing through the channels of the devices must be greater than the holding current of the SCR; a pulse must be applied to one of the gates to trigger the SCR action.

The trigger can come from several sources: the power-up sequence may cause problems if the SCR gate receives power before the other terminals. Another possible trigger source is a high slew rate across the intrinsic SCR. When the SCR is triggered, the CMOS devices are suddenly shorted out, and the output impedance of the device becomes very low.

Q_4 of the Si7660 can sometimes experience the conditions to cause SCR latchup when operating at the upper end of the input voltage range. The nearby p-channel substrate logic transistors form the complementary part of the intrinsic SCR. When the SCR action does occur, the circuit suddenly appears to be a short circuit between V_{IN} and V_{OUT}. The reservoir capacitor (C_2) rapidly discharges through this path. After C_2 has discharged, the current through Q_4 drops below the SCR holding value, and the circuit resets. If the conditions that originally caused the SCR action remain present, the device will latch up repeatedly. If the circuit input is not current limited, this action can sometimes dissipate too much power through Q_4 and the substrate logic, resulting in damage to the device.

To prevent damage to the Si7660 when conditions for latchup occur, older versions required a diode in series with the V_{OUT} pin to block the discharge of C_2 and keep the current below the holding value of the SCR. This diode was used whenever the input voltage could exceed 6.5 V at room temperature. Figure 6 shows the operating range of the improved Si7660.

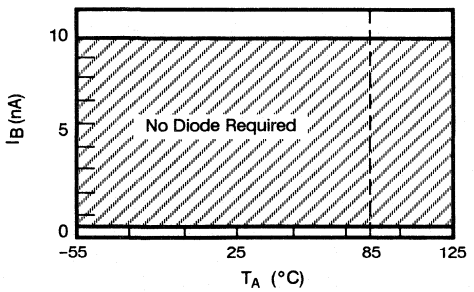


Figure 6. Range of Input Voltage and Operating Temperature for the Si7660

The Si7661 is a higher voltage device than the Si7660, and is designed on a different process. This high voltage silicon gate process reduces the parasitic betas in Q_4 to a value that makes it extremely difficult to produce the conditions for latchup. Because of this, the series diode is not needed for proper operation.

General Applications

The Si7660 and Si7661 are intended for use as voltage inverters. However, with a few added components, the inverter circuit can be rearranged to provide many different voltage levels. In some configurations, they can even provide more than one voltage output at the same time. The possibilities include voltage inversion, voltage multiplication, and even simultaneous inversion and multiplication.

Basic Voltage Inversion

With no load, the output voltage magnitude of the basic voltage inverter circuit shown in Figure 7 will typically be within 0.1% of the V+ (input voltage) magnitude for the Si7660 and within 0.3% of the input voltage magnitude for the Si7661. As the load current increases, the output will drop as shown in Figure 8(a). The effective output resistance will vary with input voltage as given in Figure 8(b). Once the load current reaches its limit (30-40 mA for the 5 V case), the inverter can no longer regulate the voltage properly and shuts down to protect itself from extreme power dissipation.

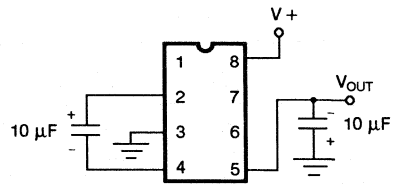


Figure 7. Schematic Diagram of the Basic Inverter Circuit

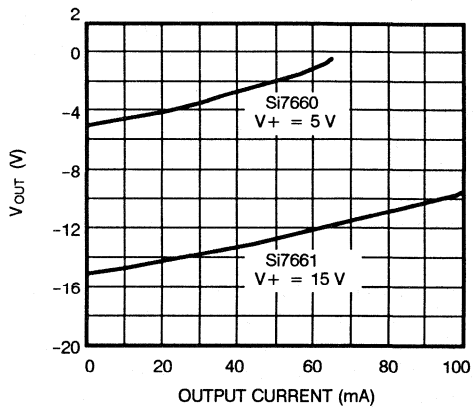


Figure 8(a). Variation of Output Voltage as a Function of Output Current

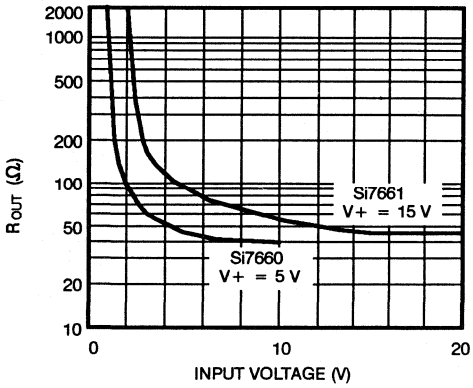


Figure 8(b). Variation of Output Resistance as a Function of Input Voltage.

CAUTION: At higher input voltages (for either device), the output maximum limit can cause the power dissipation to exceed the maximum rating of the package (especially plastic). Always calculate the maximum power dissipation for your design.

TABLE 1

Effect of Varying the Pump and Reservoir Capacitor Size on Output Ripple Noise.

	Capacitors (μF)	V_{OUT} (V)	VR (mV_{p-p})
Si7660	10	-3.838	150
Inverter Mode	22	-3.862	75
(see Figure 7)	47	-3.873	30
V+ = +5 V	100	-3.874	26
I_{OUT} = 10 mA	470	-3.879	10
	1000	-3.880	5
Si7661	10	-13.849	175
Inverter Mode	22	-13.872	80
(see Figure 7)	47	-13.882	38
V+ = +15 V	100	-13.883	29
I_{OUT} = 10 mA	470	-13.885	10
	1000	-13.890	5

The output ripple of the inverter is a function of the oscillator frequency as well as the size of the pump and reservoir capacitors. The nominal oscillator frequency is 12 kHz for the Si7660 and 10 kHz for the Si7661. Because the output ripple is important in some linear applications where supply noise is critical, Table 1 provides ripple values for different pump and reservoir capacitor values.

It is important to note that increasing the capacitor size can lead to other difficulties. The main problem is that the large capacitors may draw excessive amounts of current at turn-ON. If the current is too great, the power dissipation of the device can be exceeded causing destruction of the converter. Even when the device is running, the charge transfer under heavy loads can push the switches to their limits.

As stated before, the LV pin shorts out the internal regulator at low voltages when it is tied to ground. The LV pin should be grounded for operation below 3.5 V for the Si7660 and 9.0 V for the Si7661. However, it is necessary to leave the LV pin floating for high voltage operation, as shown in Figure 9. Failure to do so could permanently damage the device. Figure 10 shows the inverter configured for low voltage operation.

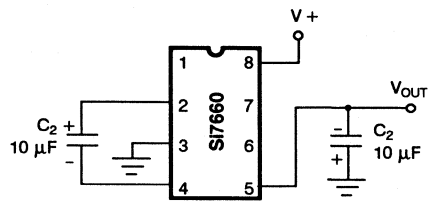


Figure 9. Inverter Circuit Connections for High Voltage Operation

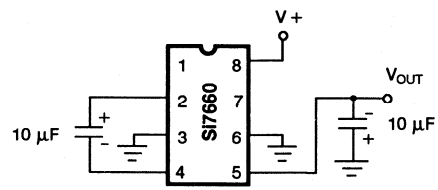


Figure 10. Inverter Circuit Connections for Low Voltage Operation

Voltage Multiplication

Figure 11 gives the schematic diagram of the voltage doubler. This circuit requires only two additional diodes and will provide positive voltage multiplication at the expense of the voltage drops of the two diodes in series with the output. This means the positive multiplier will not be able to provide the near perfect output function like the basic inverter circuit does. The output voltage of the multiplier will be:

$$V_{OUT} = 2\,(V+) - 2\,V_{diode} \qquad (1)$$

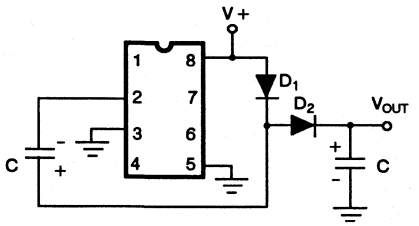


Figure 11. Voltage Doubler Schematic Diagram

The circuit of Figure 11 can also be used as a negative-to-positive voltage converter. To do so, set Pin 8 to Ground and Pins 3 and 5 to the negative input voltage, V–. The output voltage will then be:

$$V_{OUT} = |V-| - 2V_{diode} \quad (2)$$

Simultaneous Inversion and Multiplication

The circuit shown in Figure 12 will provide both positive multiplication and inversion at the same time. The output voltages will be the same as those given in equations 1 and 2. This configuration is limited by the load current that can be drawn out of either output before the circuit becomes overloaded.

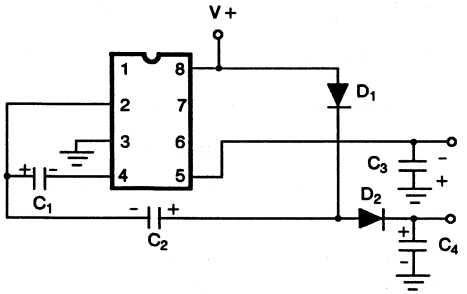


Figure 12. Combination Inverter/Multiplier Circuit

Parallel Connection

Although a single Si7660 and Si7661 cannot supply very large amounts of current, higher currents can be provided when several devices are connected in parallel. As shown in Figure 13, two or more inverter circuits can be paralleled to provide a lower output resistance, providing a smaller output voltage drop for a given current. This circuit will also expand the operating output current ranges slightly. Each device must have its own pump capacitor, but the reservoir capacitor is shared between all of the devices.

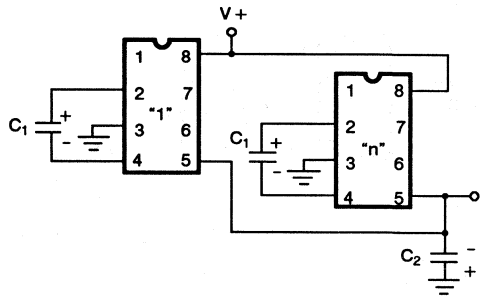


Figure 13. Paralleling Multiple Voltage Converters for Increased Current Capability

When two or more devices are paralleled, the output noise (ripple) will contain not only components at frequencies of each of the oscillators, but also at sum and difference frequencies due to a mixing action at the inverter outputs. If such noise cannot be tolerated, the OSC pin of one of the devices can be driven by an exclusive NOR gate that compares the oscillator frequencies of the two devices as shown in Figure 14. This forces the two devices to alternate their charge and transfer cycles, which will not only reduce output noise but also maximize efficiency.

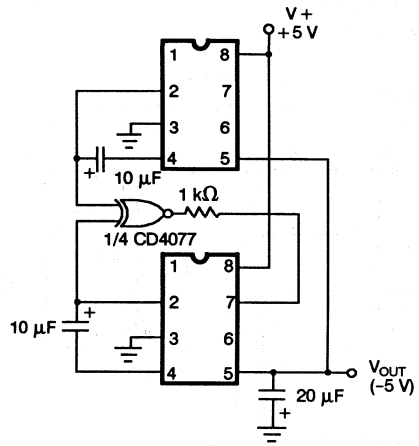


Figure 14. Synchronizing Two Si7660's or Si7661's with a Single Exclusive NOR Gate

Series Connection

When high voltage inversion is desired, inverter circuits can be placed in series to produce voltage outside of the operating range of a single Si7660 or Si7661. Figure 15 shows two inverters cascaded to double the input voltage magnitude while inverting the voltage at the same time.

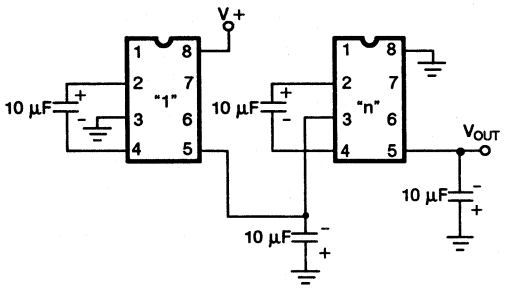


Figure 15. Cascading Devices for Greater Output Voltage Range

When cascading devices, however, the power dissipation of each device must be considered. As each new stage is added, the previous stages will be subjected to more and more load current, from both the quiescent current of the new stage and the multiplying action of the load current through each of the stages, as shown in Figure 16. As the number of cascaded devices increases, the effective output resistance also increases which will severely reduce the output voltage for a given current level when compared to a single inverter. This effect can be reduced by paralleling devices in the first stages, though the cost in parts increases twofold for every added stage.

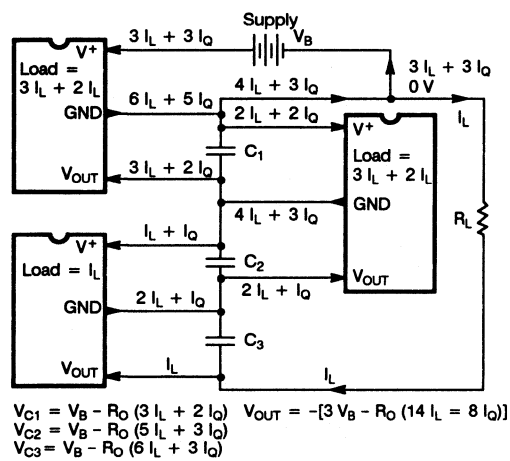


Figure 16. Current Model of Cascaded Voltage Converters

Changing The Oscillator Frequency

The typical oscillator frequencies were given in the description of the basic inverter circuit. However, Figure 17(a) shows that the maximum power efficiency is not achieved at the typical oscillator frequency. If maximum power efficiency is desired, an external capacitor can be connected between the OSC pin and ground. Figure 17(b) illustrates the effect of added capacitance on the oscillator frequency. A resistor connected from the OSC pin to V+ may be used to increase the oscillator frequency. This will reduce ripple amplitude at the expense of reduced efficiency. Values above 2 MΩ are usually adequate.

If synchronization with an external driver or clock is needed, the OSC pin can be driven either by a TTL or CMOS logic gate. Figure 18 provides the proper circuits for interfacing to either logic standard. Note that the TTL interface can only be directly connected to the OSC pin if the circuit is using a 5 V supply. If the input voltage is other than 5 V, some type of buffer circuit will be required. The charge/transfer transitions will occur on each rising edge of the clock.

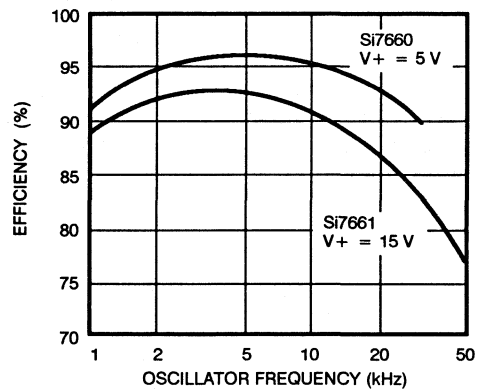


Figure 17(a). Graph of Efficiency Versus Oscillator Frequency

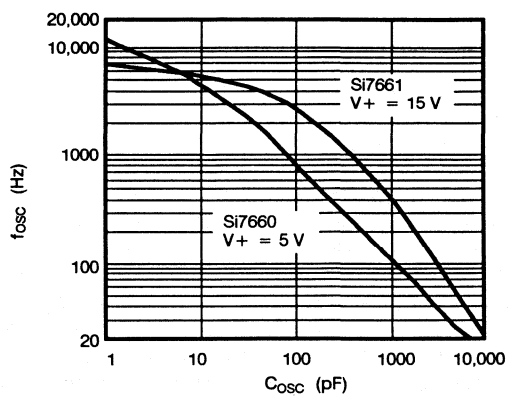


Figure 17(b). Graph of Oscillator Frequency Versus Added Capacitance

Specific Applications

When looking at possible applications for the Si7660 and Si7661, it must be remembered that these devices are VOLTAGE sources, not CURRENT sources. Therefore, any heavy load will either greatly reduce output voltage (possibly out of the desired range) or cause the device to go into power shutdown. If the concept of VOLTAGE conversion is kept in mind, many problems will be avoided.

There are many places where a low current negative supply made with an Si7660 or Si7661 would do just as well as a full conventional negative supply or dc-to-dc converter module. Some examples of possible uses are power sources for operational amplifiers, dynamic RAM's, microprocessors, and data conversion products. Several examples of these systems are given below.

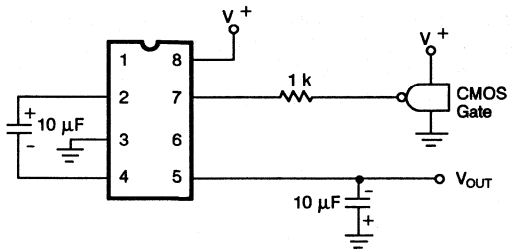


Figure 18(a). CMOS Drive Circuit for the Si7660 or Si7661

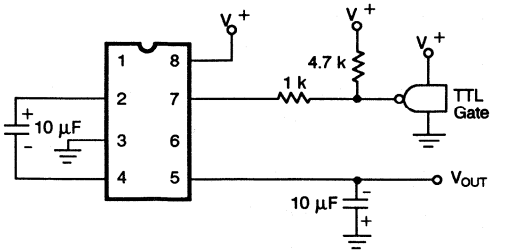


Figure 18(b). TTL Drive Circuit for the Si7660 Si7661 (5 Volt Input Only)

Memories

Several different memory manufacturers produce 16 K x 1 dynamic RAM's that have a need for a -5 V low current supply to provide substrate biasing. The National MM5290, AMD AM9016, and THOMSON MK4116 all use this type of arrangement. Table 2 gives the -5 V supply current requirements for each of these devices.

The only constraint in using the Si7660 or Si7661 for this application is when calculating the voltage fluctuations that will occur when a location is read from or written to.

TABLE 2
Current Requirements of Several Different Dynamic RAMs.

Device	Operating Current (µA)	Standby Current (µA)	Refresh Current (µA)
MM5290 (0 to 70 °C)	200	100	200
AM9016 (0 to 70 °C)	200	100	200
AM9016 (-55 to 85 °C)	400	200	400
MK4116 (0 to 70 °C)	200	100	200

Make sure that the ABSOLUTE MAXIMUM current is considered so that the negative supply for the dynamic RAM will not be pulled down more than 5% (below 4.75 V) during a memory read or write. Even with the maximum current taken into account, the Si7660 or Si7661 could easily provide the negative supply voltage supply for an entire 16 K x 8 dynamic memory bank.

Op Amps

Operational amplifiers are one of the most commonly used integrated circuits and often use negative supply voltages. Although some op amps can supply high current loads, more often the current requirements involved are well within the capabilities of the Si7661.

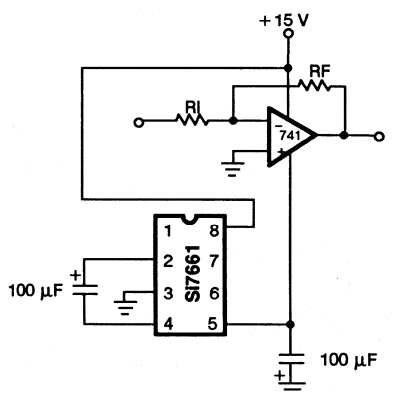


Figure 19. Using the Si7661 to Generate the Negative Rail for a 741 Op Amp

Figure 19 shows the Si7661 supplying the negative voltage to a 741 op amp configured as an inverting amplifier. As the current drain through the negative supply terminal of the op amp increases, the output voltage of the Si7661 will decrease. However, this will not affect the output capability of the op amp at its rated output current. Figure 20 illustrates this with a photograph of the input and output of the circuit in Figure 19 when a 1 kΩ load was placed on the amplifier output. The output was undistorted to 26 V peak-to-peak.

9

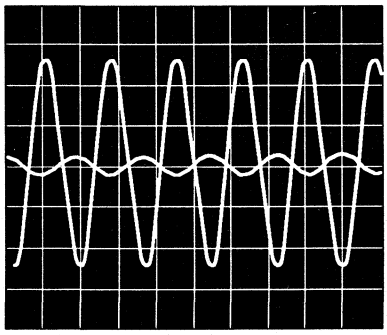


Figure 20. Input and Output of the 741 Inverting Amplifier at Maximum Undistorted Output

The output ripple of the Si7661 must be taken into consideration when using it as an op amp supply. Some op amps do not have adequate power supply rejection to withstand the ripple noise level of the Si7661. The pump and reservoir capacitors can be chosen to minimize this noise condition (see Table 1). The ripple should be measured at the maximum negative supply current (i.e., rated load) to determine if the Si7661 can be used to supply the op amp.

Analog Switches

Although in most cases the Si7660 or Si7661 cannot supply sufficient current for analog switch applications, there are some exceptions. For example, Figure 21 gives the schematic diagram of a circuit that was used to interface a Northern Telecom telephone set to an ICOM 2AT2-meter amateur radio transceiver. New designs should use the silicon-gate DG402 SPDT switch.

The analog switch provides isolation for the microphone and speaker connections of the transceiver since the telephone set uses a single path for both transmission and reception. The telephone was operated at 12 V for direct interface to the DG305A, and the supply current from the Si7661 was <1 mA.

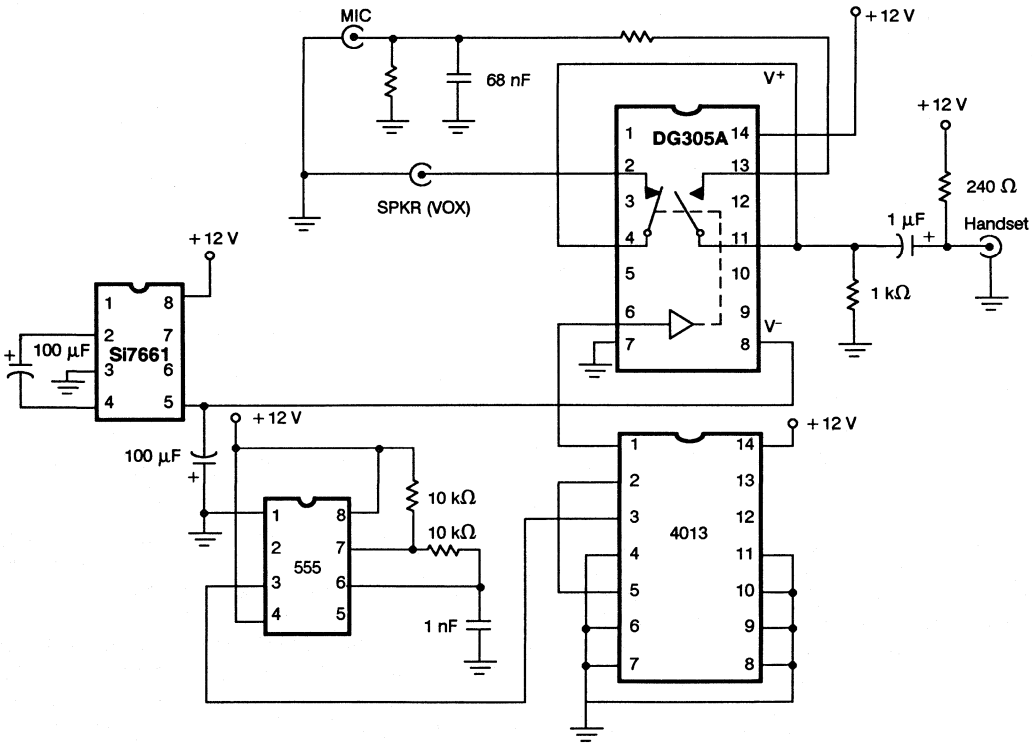


Figure 21. Using the Si7661 to Supply a Low-current Analog Switch Current

Microprocessors

Some of the older standard microprocessors need a negative supply for substrate biasing. The Intel 8080 microprocessor is a good example of this. It is an inexpensive 8-bit CPU that has many different support chips available. To provide the negative supply voltage (-5 V), a basic inverter circuit (such as in Figure 7) using an Si7660 is connected to Pin 11 of the microprocessor. The 8080 negative supply draws a maximum current of 1 mA which will not pull down the supply voltage to any great degree.

Regulator Circuits

This section discusses some of the possible methods for using the Si7660 or Si7661 in constant-voltage output circuits over a given output current range. For low current inverter applications, the circuit shown in Figure 22 can be used. The output impedance of the circuit can be as low as 5 Ω with regulation up to approximately 20 mA. Note that if converters are paralleled on the output of this circuit, they should be synchronized to minimize output voltage fluctuations and output noise.

Another regulator application uses the Si7660 or Si7661 in a positive voltage regulator. Conventional three terminal voltage regulators have a voltage drop of greater than 1 volt between the input and output when operating with fairly heavy load currents. The circuit given in Figure 23 uses an Si7660 or Si7661 voltage converter to double the voltage which is then regulated by the op-amp and FET. This configuration allows regulation without the voltage drop as long as the input voltage does not drop below the Zener voltage plus the product of I_D times $r_{DS(ON)}$.

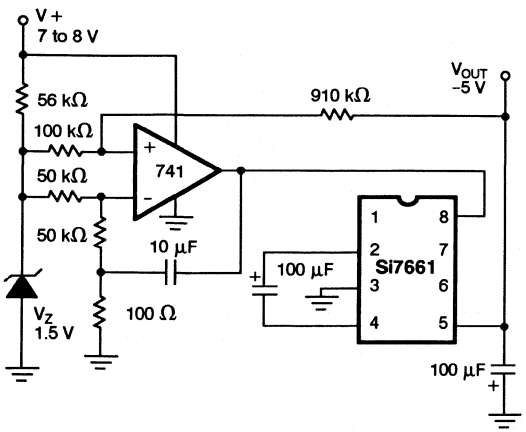
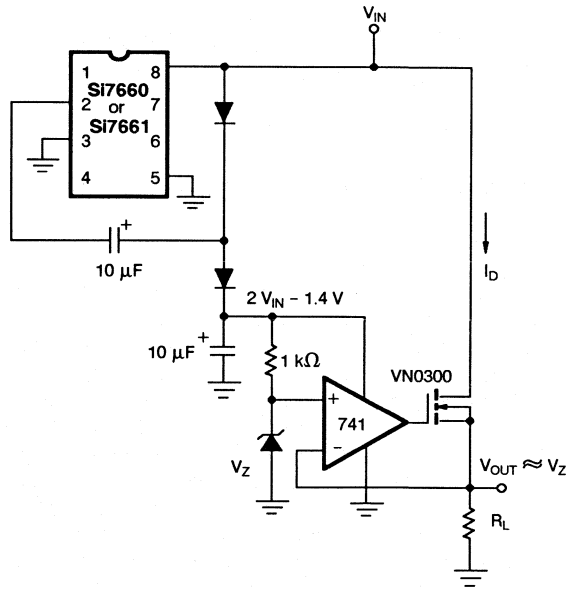


Figure 22. Low Current Inverting Regulator Circuit



For I_D = 50 mA:

$V_{IN} > V_Z = (I_D \times r_{DS(ON)})$

$V_{IN} > 5.2\ V + (50\ mA \times 1.2\ \Omega)$

$V_{IN} > 5.26\ V$

Figure 23. Schematic Diagram of the Positive Regulator Circuit

Therefore, as long as the input voltage does not drop below 5.26 V, the input is guaranteed to be regulated as close to the zener voltage as can be attained by the common mode offset voltage of the op-amp. By selecting the correct Zener diode, this circuit can supply more than 100 mA and can be adjusted for varying voltage outputs up to the input voltage limit of the voltage converter.

CONCLUSION

The Si7660 and Si7661 are inexpensive alternatives to full negative supplies in many different low cost applications. Although they are designed for generation of negative voltages, many different voltage levels can be generated with a few additional parts. The examples given here are only a few of the many possible applications that could utilize the benefits of reduced board space and cost that the Si7660 and Si7661 provide.

9

12-VOLT TTL-COMPATIBLE ANALOG SWITCH BREAKS THE 50-ns BARRIER

Steve Moore

DG601: The First PolyMOS Switch

High-speed analog switching has always been the domain of discrete FETs combined with fast bipolar drivers. Monolithic analog switches have either been too slow for sampling below 50 ns or they have lacked 5-V logic compatibility. The DG601 is a new quad analog switch which meets both the speed and logic compatibility requirements for high-speed sampling. Built with 18-V silicon-gate CMOS (PolyMOS) technology, the DG601 is excellent for single 12-V supply applications, such as disk drives, where 5-V logic compatibility is required with a 12-V analog range. This article describes the operation of the DG601 and how its unique design features are applied in high-speed sampling, signal conditioning, and level translation applications with 12-V, ±5-V, and single +5-V supplies.

PolyMOS: Silicon-Gate CMOS for High-Speed ICs

The DG601 is built on the Siliconix proprietary PolyMOS process: a 5-µm silicon-gate CMOS process developed for mixed analog and digital integrated circuits. Traditional TTL-compatible analog switches, such as the DG201A, are built on a 44-V, 10-µm metal-gate CMOS process. This process is required for ±15-V operation. PolyMOS has four advantages for high-speed, reduced-power-supply analog switch design:

1. Thinner Gate Oxide

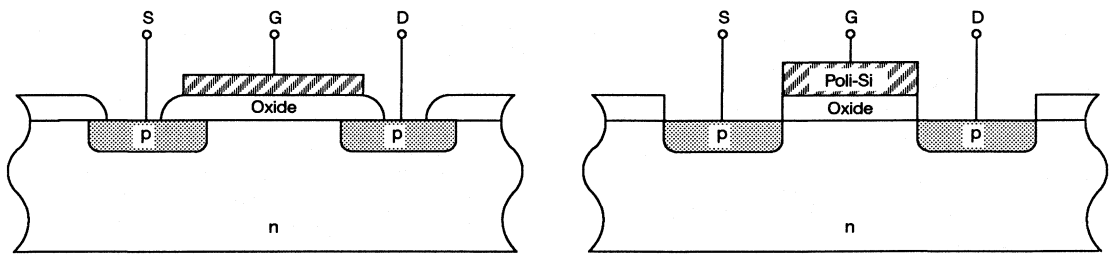
   PolyMOS gate oxide thickness is nominally 800 Å, compared with 1800 Å for the 44-V devices. This difference provides higher gain for a given device area and faster switching.

2. Smaller Feature Size

   The 5-µm feature size (compared to 10-µm) allows for a smaller gate length at the expense of the operating voltage range. The smaller gate length also results in higher gain, lower capacitance devices.

3. Silicon-Gate Technology

   Figure 1 compares a metal-gate MOSFET to a silicon-gate MOSFET. In metal-gate devices, the gate area overlaps the source and drain diffusions. This overlap is eliminated on the silicon-gate device. Self-alignment is accomplished in the silicon-gate process by forming the gate as the source and drain diffusions are made. In metal-gate technology, the gate area is defined by a separate masking step. This process results in inferior definition of the gate area. Eliminating the gate overlap reduces parasitic capacitance and allows faster switching.



a) Metal-Gate MOSFET

b) Silicon-Gate "Self-Aligned" MOSFET

Figure 1. Comparison of Metal- and Silicon-Gate Structures

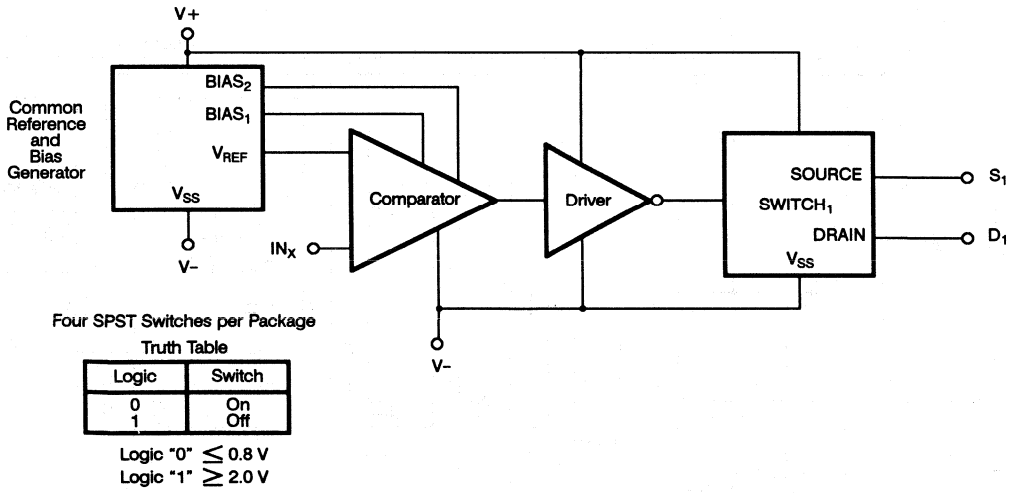


Figure 2. Functional Block Diagram and Truth Table for the DG601 Quad Analog Switch

4. Lower Thresholds

   The PolyMOS process device thresholds are lower than the thresholds on the 44-V analog switch processes. PolyMOS thresholds are typically 0.8 V, compared to 1.8 V. This results in better low-voltage operation and allows increased gate enhancement with 5-V supplies. Increased gate enhancement results in faster device switching as well as lower ON-resistance.

The DG601 Device Description

Figure 2 shows the functional diagram for the DG601. A CMOS analog switch -- consisting of an input amplifier, a switch driver, and a CMOS switch -- is repeated to create four independent analog switches. A common reference generator sets up the logic trip point for the logic input differential amplifier. Each input comparator detects a high or low level at the logic input and provides level translation from TTL-logic levels (V_{IL} = 0.8 V, V_{IH} = 2.0 V) to rail-to-rail drive levels to turn the CMOS analog switch on or off. Please refer to the truth table in Figure 2 for switch-state logic.

Figure 3 shows the individual switch channel in more detail. The individual stages shown in Figure 2 are outlined in dotted lines in Figure 3. These stages are the input logic level comparator, the logic threshold reference, the switch driver, and the CMOS switch.

The Input Comparator

The input comparator consists of a differential amplifier, that compares the input logic voltage to the reference level, and a level shifter, that translates the output of the differential pair to a signal that swings from rail to rail. This level translation allows a TTL-logic input, which is specified with V_{IL} = 0.8 V and V_{IH} = 2.0 V, to control the switch output state.

The Logic Threshold Reference

The logic threshold reference circuit provides two functions. First, it generates bias voltages that set the differential amplifier source current and the level shifter pull-up current. Second, it generates the TTL-level reference voltage to all switches. The TTL reference consists of a Zener diode buffered by an emitter follower. The Zener is biased with a current source to provide a stable voltage (nominally 6 V). It is level-shifted down by a V_{be} (0.7 V) and then divided down with a voltage divider to provide a stable logic threshold of 1.5 V.

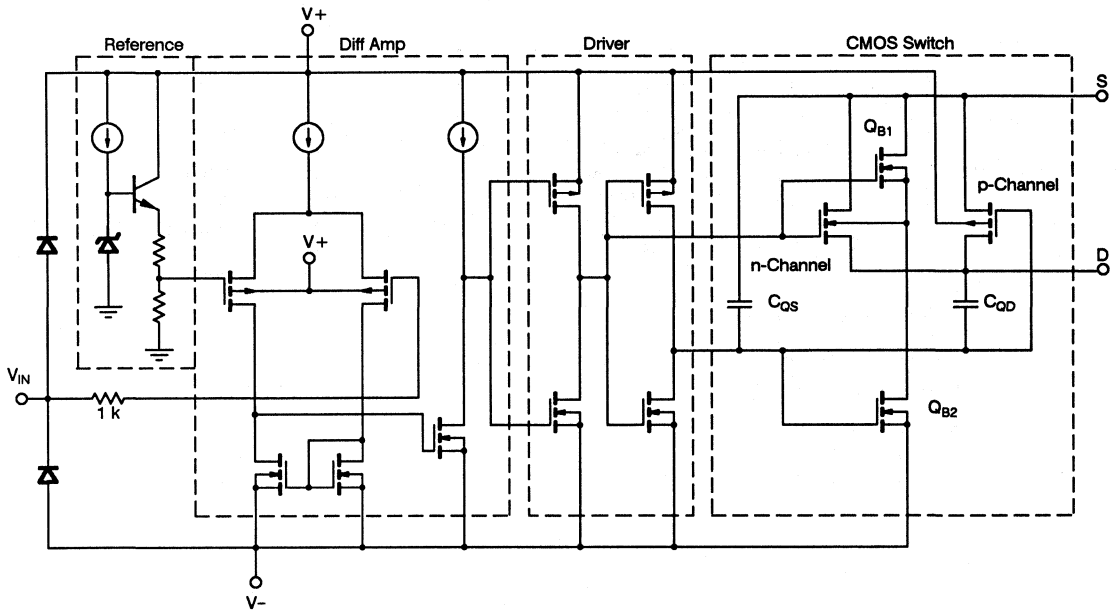


Figure 3. Detail of One Channel of the DG601 Analog Switch

The Switch Driver Stage

The switch driver stage consists of two CMOS inverting buffers. They provide the current gain needed to quickly charge and discharge the gates of the large output FETs, and they also provide the complementary drive phases that are required to drive the output p- and n-channel FETs simultaneously.

The CMOS Switch Stage

The CMOS switch stage has a p-channel enhancement-mode MOSFET connected in parallel with an n-channel enhancement-mode MOSFET. To turn the switch on, the gate of the p-channel device is pulled to V- and the gate of the n-channel is pulled to V+. The opposite conditions are required to turn the switch off. The parallel combination of p- and n-channel devices reduces the effect of the increasing ON-resistance ($r_{DS(ON)}$) of each device with decreasing gate enhancement. When the analog signal nears either supply rail, the gate-source voltage (or enhancement) of one FET is reduced to zero, and the other FET remains on to maintain low switch $r_{DS(ON)}$ across the full analog range.

The Body Snatcher Circuit

Q_{B1} and Q_{B2} in Figure 3 form the "body snatcher" for the n-channel switch FET. When the switch is turned on, the body snatcher connects the body of the device to its source via Q_{B1}, thus reducing the ON-resistance modulation which results from the "body effect" of the n-channel device. The other half of the body snatcher reduces switch leakage by connecting the body to V- via Q_{B2} when the switch is turned off.

Charge Injection Compensation

Two capacitors shown in Figure 3 (C_{QS} and C_{QD}) provide charge injection compensation on the drain and the source of the switch FETs. These capacitors are actually arrays of binary-weighted devices that have been trimmed at the mask level to provide optimal charge compensation to minimize charge injection.

12-V, ±5-V, and Single 5-V Operation

A unique feature of the DG601 is the variety of power supply voltages that are specified and guaranteed for operation. Many switch manufacturers claim single-supply operation, but the switches are not actually tested or guaranteed for operation with anything but ±15-V supplies. The DG601 data sheet has three separate specification tables. This guarantees TTL-compatible operation with a 12-V single supply, ±5-V dual supplies, and a 5-V single supply. However, switch performance is affected by changing the supply conditions. Table 1 compares the ON-resistance and switching time performance under three conditions.

Table 1. Performance Variation with Supply Voltage Change

Supply Voltage V+, V- (V)	Maximum $r_{DS(on)}$ (Ω)	Typical t_{ON} (ns)
+12, 0	35	30
+5, -5	40	34
+5, 0	100	32

Application Examples

Analog switches are found in a variety of applications. The DG601 is useful in applications that require low-supply voltages, high-speed switching, and/or low ON-resistance. Computer peripherals, such as disk drives, are an example of single-supply (12-V or 5-V) systems that use analog switches for sampling, signal conditioning, signal routing, and level translation. High-speed data acquisition systems typically use ±5-V supplies for the flash converters, and they require very fast, accurate switches for the input sample-and-hold amplifiers.

Sample-and-Hold Amplifiers

Figure 4 shows a sample-and-hold amplifier that provides a very fast sample acquisition time with the ±5-V power supplies that are required for high-speed A/D converters. The circuit is controlled by the sample-and-hold input, which is a TTL (5-V CMOS) control line. When a logic "0" is applied to the sample-and-hold input, the switch is turned on. A sample of the input signal is acquired by charging up the hold capacitor (C_H) to the value of the input signal. When a logic "1" is applied, the switch is turned off. The value of the input signal at the time the switch is turned off is held in C_H. The sample-and-hold amplifier is designed for the following features:

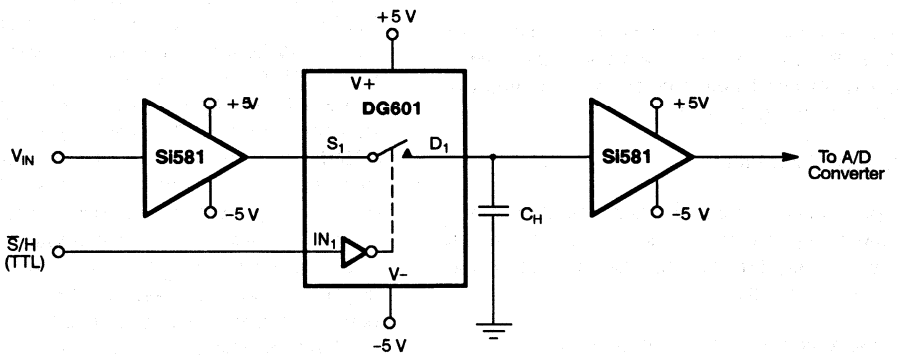


Figure 4. Simple High-Speed Sample-and-Hold Circuit for Data Acquisition System Front Ends

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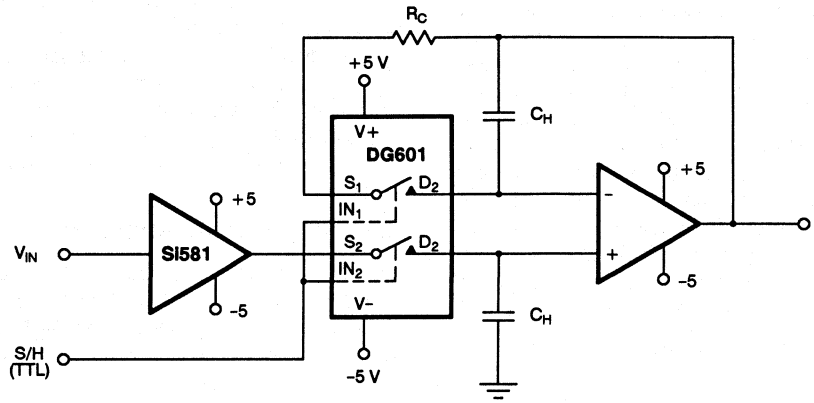

Figure 5. Using On-Board Switches to Cancel Out Charge Injection

1. ±5-V Operation

   The DG601 and Si581 buffer are both rated for ±5-V operation.

2. Low Pedestal Error

   This is a result of the low charge injection of the DG601. Pedestal error can be reduced even further by using other switches in the quad to cancel out the injected charge (Figure 5).

3. Fast Acquisition Time

   Sample-and-hold amplifiers take advantage of the fast switching time of the DG601 with a (+5-V supply, t_{ON} is typically 50 ns) and the high slew rate (800 V/µs) of the Si581.

   The 20-µA bias current for the Si581 will result in a 20-mV/µs droop rate, which is adequate for 8-bit operation at a 1-MHz sampling rate. Better droop rate can be achieved with a lower input-bias current buffer, such as a FET input device.

4. TTL-Compatible Operation

Precision Signal Routing

The low ON-resistance of the DG601 makes it an ideal choice for digitally controlled analog signal conditioning applications, such as channel selection and gain ranging in low-voltage systems. High-voltage switches (like the DG201A) suffer increased ON-resistance and logic incompatibility when operated at lower supply voltages like +12 V. The 30-Ω ON-resistance of the DG601 helps to maintain low impedance levels and reduce switch resistance-induced offsets and noise. Figure 6 shows a DG601 used as a read/write selector in a disk drive head amplifier circuit. One of the switch pairs directs the write signals from the output head drive amplifier to the head, and another pair connects the output of the head to the read amplifier inputs. This same application works with single 5-V supplies, used for 2.5-inch drives, with an increase in ON-resistance from 25 Ω (typically, with V+ = 12 V) to 85 Ω (typically, with V+ = 5 V, V− = 0 V).

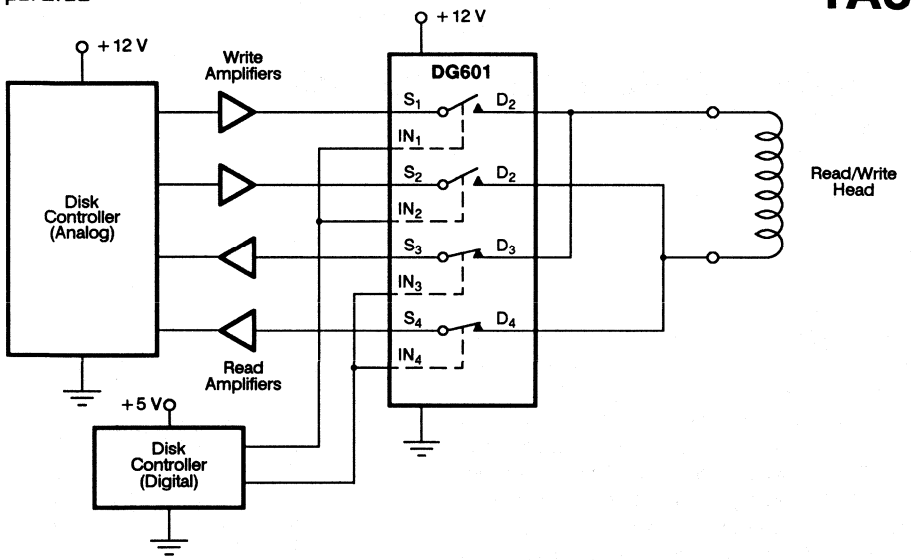

Figure 6. Disk Drive Read/Write Selector

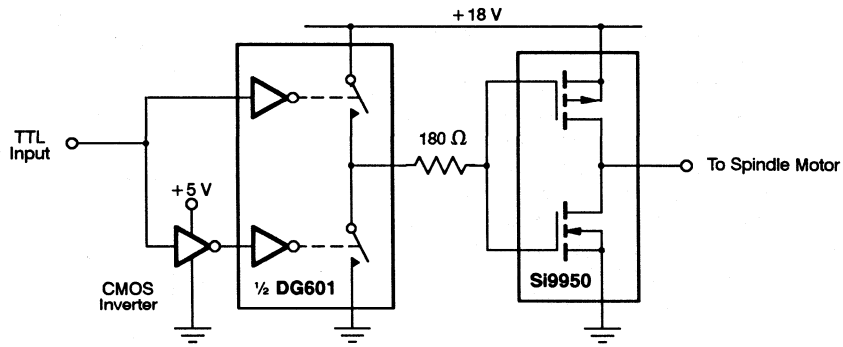

Figure 7. DG601 Provides Level Translation for MOSFET Gate Drive.

Level Translation Applications

The DG601 makes an excellent level translator for use with MOSPOWER drivers, relay drivers, JFET drivers, GaAs FET drivers, DMOS drivers, and other circuits that require high-speed 5-V logic compatibility and an output range up to 18 V. Figure 7 shows one-half of a DG601 acting as the interface between the TTL and the Si9950 half-bridge driver. The Si9950 has a 1000-pF input capacitance, which is difficult to drive from a standard logic gate. The DG601 delivers a fast level translation from a TTL signal to provide 18 V of enhancement on the Si9950. A 180-Ω resistor is placed in series with the Si9950 input to limit the current through the DG601 to 100 mA (worst case). This prevents the current from exceeding the absolute maximum current rating. Increased gate drive current can be handled by connecting two sets of switches in parallel.

Conclusion

The DG601 has many applications in low-voltage systems, having been designed and specified for 12-V, TTL-compatible operation. It is also excellent in ±5-V and single 5-V supply applications where fast switching speed, low charge injection, and low ON-resistance are required. This technical article has examined how the switch works and has highlighted some typical applications to assist the design engineer in getting optimum performance in low-voltage mixed analog/digital systems.

HIGH-PERFORMANCE MULTIPLEXING WITH THE DG408

Steve Davies

The DG408 and DG409, new multiplexers from Siliconix, represent a new generation of high-performance multiplexers and demultiplexers with many specific improvements over existing products available today. Built with the company's high-voltage silicon-gate technology, these new ICs offer *significantly* reduced ON-resistance ($<100\ \Omega$), leakage currents ($I_{S(OFF)} < 0.5$ nA), power dissipation (2.25 mW), and much faster switching (250 ns) over older industry standards. These improved specifications allow designers to greatly reduce system errors and improve system performance.

The DG408 and DG409 will enhance two primary multiplexer and demultiplexer applications: communications and telemetry. Important multiplexer specifications depend on the application and the accuracy required by the system. For example, in communications, switching speed is important; whereas, in telemetry, ON-resistance, charge injection, and output capacitance are critical because they determine the accuracy of the system. This article will present examples of these types of applications and discuss the benefits that these new multiplexers bring to their system performance.

Communications

The digital telephone exchange is a communication multiplexed system. In this type of system (see Figure 1), a number of telephone channels carrying speech are sequentially switched (i.e., multiplexed) for fixed periods of time into an analog-to-digital converter. Once converted to a digital form, the different speech signals can be processed and routed within the exchange.

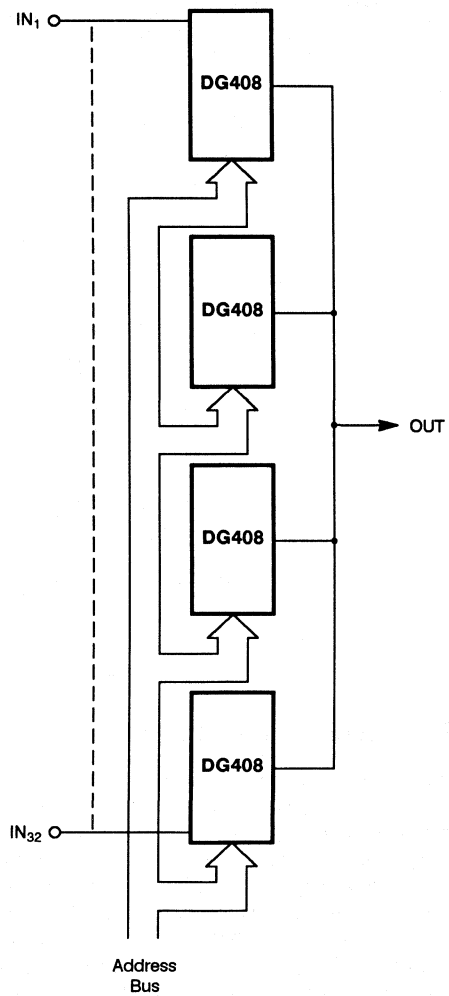

Figure 1. 32-Channel Multiplexed System

A typical specification for the voice bandwidth in a telephone exchange is 3.3 kHz. For this bandwidth, an 8-kHz sampling rate is sufficient (i.e., sampling rate > 2 times the bandwidth). Therefore, each sampling period is 125 µs, during which time, each of the 32 channels of the multiplexer must be addressed. This means that each channel will be turned on for 3.906 µs (125 µs/32). This figure is ideal, since the multiplexer cannot switch in zero time. Depending on the particular multiplexer used, there will either be an overlap between sampling pulses (i.e., make-before-break switching), which leads to crosstalk between channels, or a separation between samples (i.e., break-before-make switching), which reduces the sampling time of a particular channel and results in lower multiplexer efficiency. The DG408 has switching times (250 ns) guaranteed to be more than four times faster than previously available (1 µs) multiplexers. Its guaranteed break-before-make time (10 ns) prevents crosstalk during switching transitions.

Telemetry

Telemetry offers many applications for multiplexer and demultiplexer combinations. A telemetry system uses transducers (a device which converts a physical variable, such as pressure, flow, temperature, etc. to an electrical equivalent) to measure variables, which are fed back via a multiplexer, monitored, and acted upon if necessary.

Figure 2 shows the position of a multiplexer in a high-performance, closed-loop telemetry system. The transducer output generally produces an analog output (which may need preamplification and filtering prior to multiplexing). With a wide variety of transducer types available, the inputs to the multiplexer may take many forms, including high-frequency, dc, high-level, low-level, voltage, current, and differential signals. Whether a signal requires preconditioning before being multiplexed depends on the total accuracy required of the system.

Because the multiplexer follows the transducer output, the multiplexer specification will have a significant bearing on the system accuracy. For example, a low-level signal can, potentially, require preamplification. A primary source of error with a low-level signal may be the switching transients present in the multiplexer. These transients are the result of charge injection from the switches, producing an error voltage (usually positive for a CMOS switch) which appears at the multiplexer output. Hence, the lower the signal level, the greater the error introduced by the charge injection of the switch.

For example, the DG408 with its 20-pC (typical) charge injection will create a 20-mV offset error when switching into a 1000-pF load. For low-level signals, this offset may be excessive. Using a differential multiplexer, such as the DG409, will provide at least an order of magnitude improvement in the total offset error.

High-level signals become a potential problem at different values, depending on the technology used to manufacture the multiplexer. For a CMOS multiplexer, high-level signals greater than the positive and negative supplies must be avoided to prevent permanent damage to the device. If the supplies are exceeded by the analog signal, the inherent source/drain-to-supply diodes (Figure 3) will become forward biased.

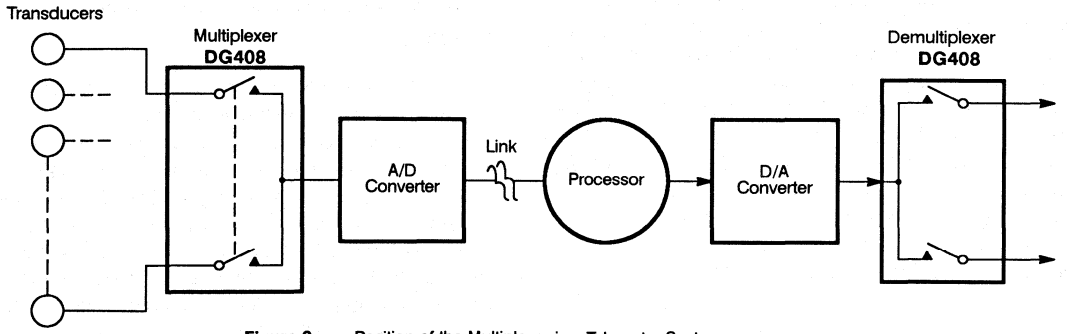

Figure 2. Position of the Multiplexer in a Telemetry System

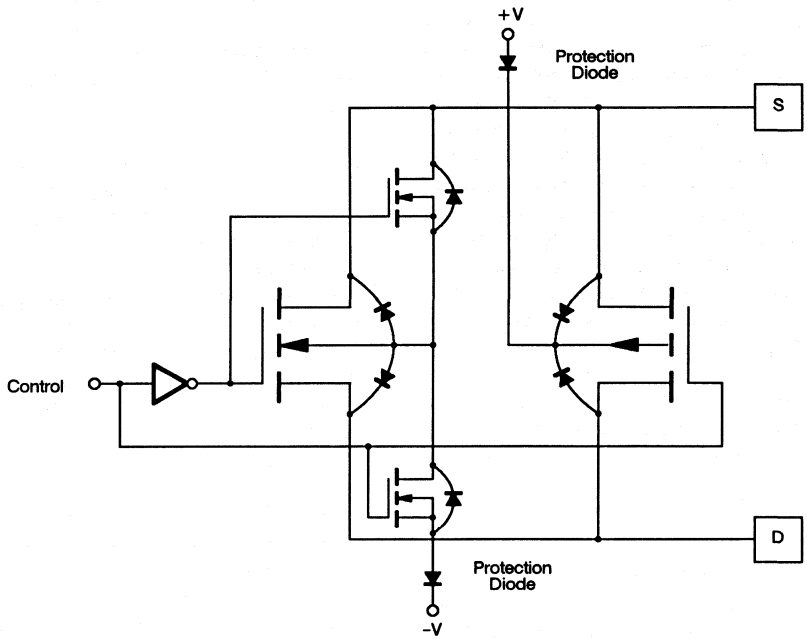

Figure 3. CMOS Switch Showing Inherent Diodes

When the expected overloads have a short duration, usually a couple of switching diodes used in series with the supply leads will prevent permanent damage by blocking the flow of reverse current.

Differential signals can be generated by bridge-type transducers. These devices will produce a signal of two components: a common-mode signal which is large and a small difference signal. It is the difference component that conveys the measurement information. Figure 4 shows the DG409 differential multiplexer being buffered by a full differential amplifier which rejects the unwanted common-mode voltage. The amplifier output consists solely of the differential signal. The ability of the differential multiplexer to reject unwanted common-mode voltages makes it especially useful in systems where pick-up of electrical noise is a concern.

High-frequency signals above a couple of MHz can limit system accuracy, whether its specific channel is on or off. When the device is turned on, the signal is filtered to some degree by the distributed resistance and capacitance of the signal path through the multiplexer. When the device is turned off, the high frequency couples with adjacent channels through the "off" channel to the output, thereby adding to the system error.

What Makes the DG408/409 a Good Multiplexer?

Choosing a technology for a multiplexer can depend on many factors, including the environment, its ruggedness, the accuracy required, and the cost. The choice is often a compromise between these factors. The DG408/409 is fabricated with high-voltage CMOS technology developed specifically by Siliconix to enhance the analog switch/multiplexer range. The processing steps include a buried layer which prevents the formation of the inherent SCR found in CMOS structures. This immunity to latch-up makes the DG408/409 particularly insensitive to transient conditions which could occur in a remote multiplexer environment.

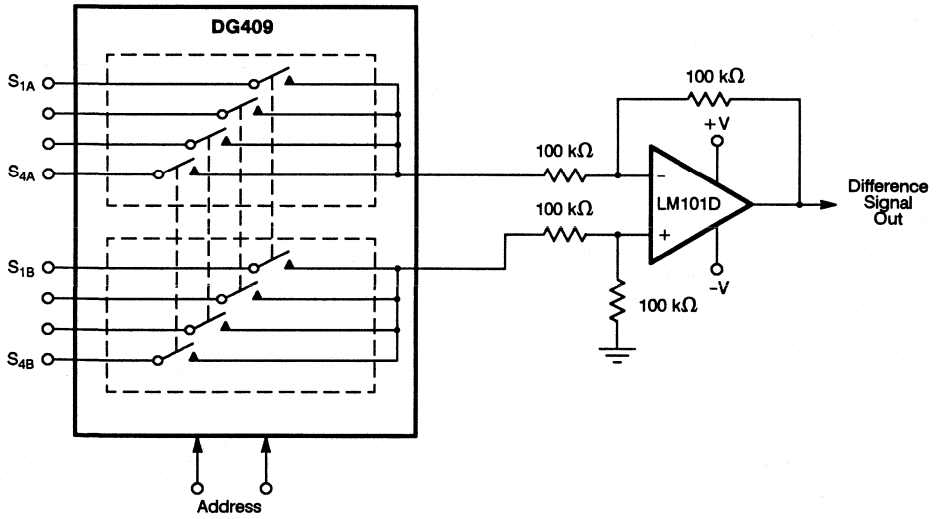

Figure 4. Differential Multiplexer

Figure 5 shows a typical profile, including the inherent parasitic components. Under specific conditions (inputs exceeding the supplies), one or more of the pn junctions becomes forward biased and, under normal conditions, would result in the pnpn structure turning on. This would appear as a short circuit across the supply and would persist until the power was removed or the device burned up.

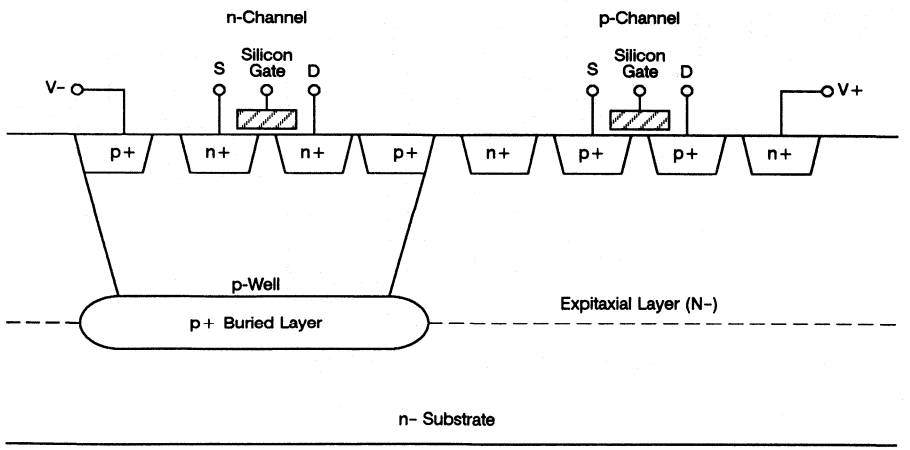

Figure 5. Cross Section of a High Voltage Silicon Gate CMOS Device

Using the "buried layer", the gain of the pnpn structure has been reduced to less than unity. This effect makes device latch-up virtually impossible.

Another feature of the DG408/409 is its protection to static damage. All inputs are specified with a Class 3 ESD rating (≥ 4 kV).

Accuracy

Errors introduced by a multiplexer can be split into dc and ac components. Steady-state errors in a multiplexer are due to the ON-resistance and finite leakage of the switch. Two sources of dc error can be quantified by

$$\text{input offset} = R_S \times I_{S(OFF)}$$

where

R_S = source resistance
I_S = source leakage
$r_{DS(ON)}$ = ON-resistance
$I_{D(ON)}$ = drain on-state leakage.

Figure 6 shows a typical data multiplexing system. Because the multiplexer feeds a very high impedance, its input offset is a function of its ON-resistance and the on-state leakage of the switch plus the amplifier bias current.

$$V_{OFFSET} = r_{DS(ON)} \times (I_{D(ON)} + I_{(BIAS)})$$

For the DG408/409 typical specifications, this offset will be

$$V_{OFFSET} = 100 \times (500\ pA + 30\ pA) = 53\ nV$$

This typical offset (at 25°C) should be compared with the signal level to determine whether the error introduced by the offset is acceptable.

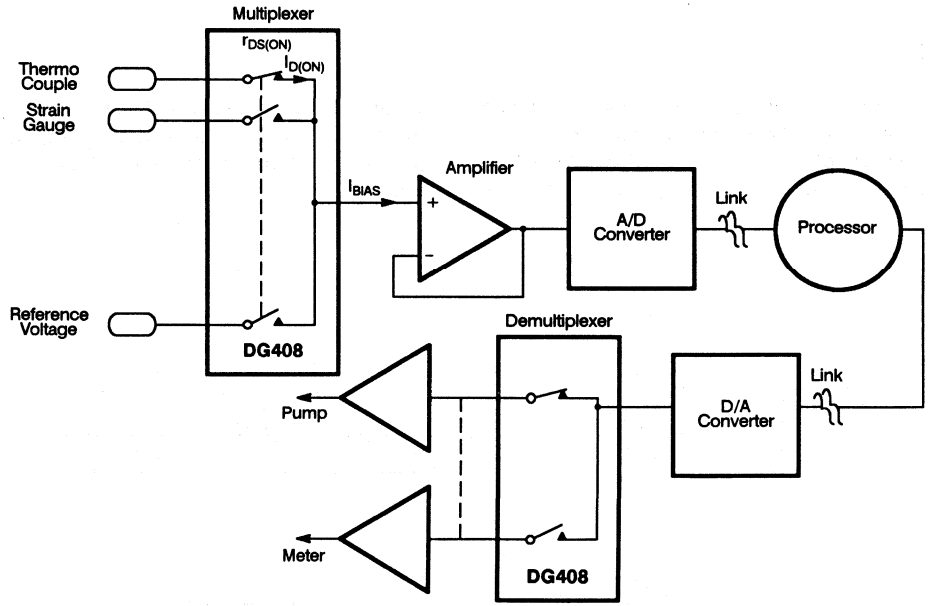

Figure 6. Typical Data Acquisition System

Another source of error that may be introduced by the switch occurs when the switch changes state. Transients (due to capacitive coupling between the drivers and drain) can be manifested as an error voltage appearing on the output node. The effect of charge injection is measured in volts and is given by

$$V = Q_i/C$$

where

Q_i is the injected charge in picocoulombs

C is the load capacitance at the output

The DG408/409 devices have been internally compensated to minimize the effects of the injection. This is achieved by including compensation capacitors on the output switch. These capacitors are sized to produce an equal and opposite transient which tends to cancel out the effect of the switch injection. Typical charge injection for the DG408/409 is 20 pC for the test configuration shown in Figure 7.

Switching Speed

Multiplexers operate in real time (i.e., samples are taken sequentially and represent the analog input signal). Obviously, the quicker a multiplexer changes state, the more samples can be taken in a given time. Fast switching operation is often difficult to achieve using larger multiplexing devices. That is, the greater the number of channels, the slower the speed due to additional capacitance at the common output node.

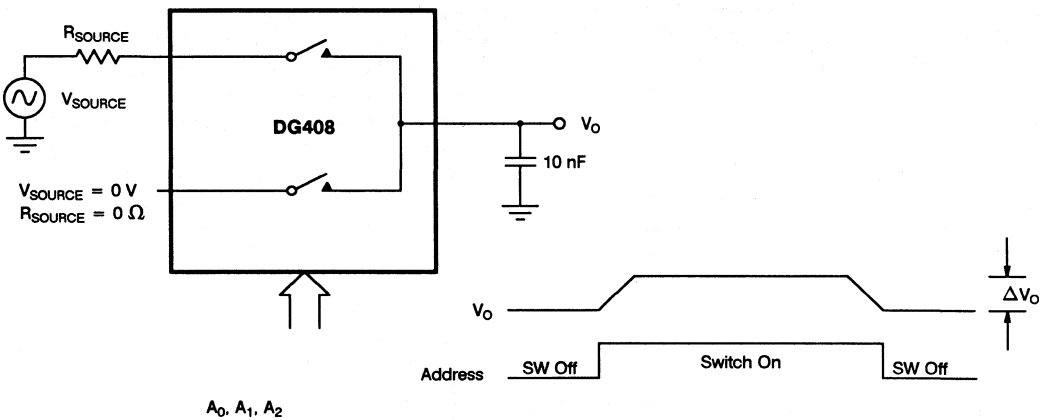

Figure 7. Charge Injection Test Circuit

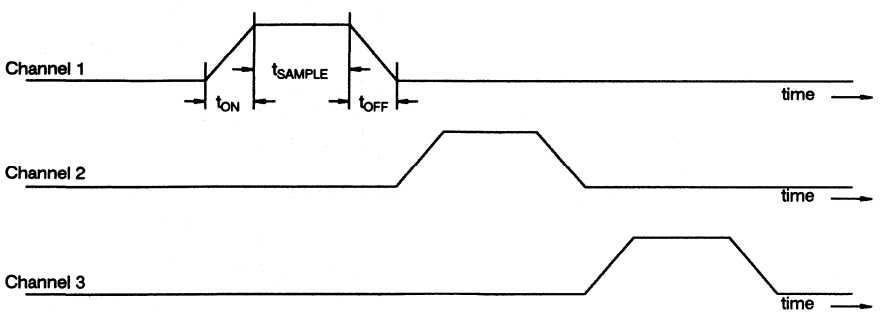

Figure 8. Channel Switching Rate

The DG408/409 switching speed (t_{TRANS}) is 250 ns maximum at room temperature with a 10-ns minimum break-before-make time. While this break-before-make time prevents overlap or "alias" between channels, it reduces multiplexer efficiency and, therefore, is kept as short as possible.

A channel-switching rate (Figure 8) is defined for the DG408/409 by t_{ON}, t_{OFF}, and t_{SAMPLE}, where t_{SAMPLE} is dependent on the application.

Assuming a t_{SAMPLE} of 1.2 µs, the maximum switching rate for the DG408/409 (with no pulse-edge overlap) is once every 1.5 µs or a frequency of 666 kHz. This example shows that the switching speed of the DG408/409 is not a significant factor unless the t_{SAMPLE} time becomes much smaller. For multi-channel systems, if the sampling theorem is obeyed, the maximum switching rate will limit the number of channels and/or the maximum frequency components of any of the channel inputs. Techniques are available to improve the switching rate, and an example using the DG408/409 and DG400 will be shown later.

Versatility

With CMOS switches, signal conduction is the same in either direction. Therefore, as shown in Figure 9, it's possible to use the DG408 as a *demultiplexer* with one input from the digital-to-analog converter and 16 outputs (using two DG408s).

This versatility allows the same advantages at the "back end" of the system -- that is, a single wire can be used to carry all the control signals to the remote site. Then the control signals may be converted back to analog form and demultiplexed for controlling the system.

Logic Compatibility

The compatibility of the multiplexer is a measure of how easy it is to interface with other system components, such as transducers, A/D converters, power supplies, the environment, etc.

The DG408/409 has many features which make this interfacing as easy as possible. For example, a regulator has been included on the chip to provide stability against power supply and temperature variations. The regulator maintains TTL compatibility over power supply variations, while the dynamic specifications can be met over the full military temperature range. The regulation also guarantees a low current consumption of ±75 µA, making it suitable for battery/portable applications. The DG408/409 electrostatic protection of ±4 kV (Class 3) at a 44-V maximum rating and the military temperature range specification make it an extremely rugged and reliable device to use in the field.

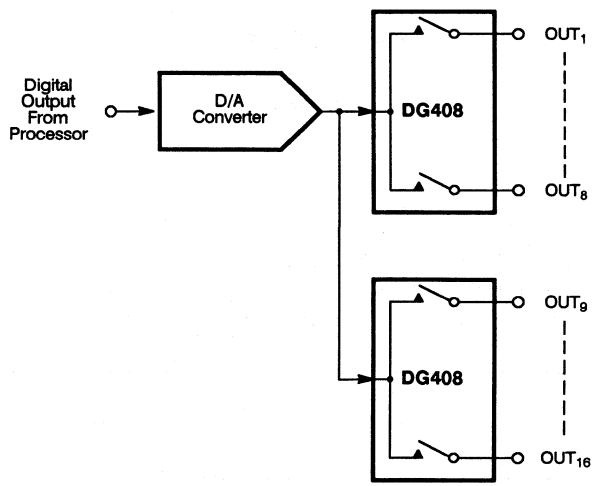

Figure 9. Using the DG408 As a Demultiplexer

Application Enhancements

The following examples of applications using the DG408/409 are intended to highlight some specific improvements over their predecessors.

Sample-and-hold circuits using analog multiplexers are widely used in analog signal processing and data conversion systems to store analog voltages accurately over time periods ranging from nanoseconds to several minutes. This ability finds many applications, including data distribution systems, simultaneous sample-and-hold designs, sampling oscilloscopes, digital volt meters, signal reconstruction filters, and analog computational circuits. Although they are theoretically simple, these high-speed, high-accuracy circuits need careful consideration in their design. Figure 10 shows the DG408 in a sample-and-hold circuit. During the sample phase, one switch in the analog multiplexer is closed and the hold capacitor is charged to the input voltage via the on-state switch. Once the capacitor is charged to its final value, the hold mode is entered by opening the switch. During the hold mode, the capacitor voltage can be examined via the low-leakage buffer. By repeating this with other switches in the multiplexer, many analog inputs can be sequentially examined.

In a high-speed system, an important specification for the circuit designer is the acquisition time of the sample-and-hold system – that is, the time delay between the sample command and the capacitor reaching its final value.

Figure 11 shows that the acquisition time is dependent on two factors. The first factor is the time from when the sample command is given to when the switch is turned on (i.e., the t_{ON} of the switch). For the DG408, the t_{ON} is guaranteed as 250 ns maximum at 25°C; this translates to a 4 times improvement over existing pin-compatible devices.

The second contribution to acquisition time is the time taken for the hold capacitor to charge to its final value. The charging time is determined by the source impedance of the analog source, the ON-resistance of the switch, and the hold capacitor. Hence, for low-impedance analog sources, the ON-resistance of the switch will play an important part in determining the time constant. The ON-resistance of the DG408/409 is guaranteed at 100 Ω over the whole analog voltage range, making a 500% improvement over existing pin-compatible parts.

To illustrate the improvements in acquisition time made possible with the DG408/409, consider the following comparison with the DG508A pin-compatible multiplexer. The acquisition time is

$$t_A = t_{ON} + n \times (R_S + r_{DS(ON)}) \times C_H$$

where

n is the number of time constants (determined by the accuracy required)

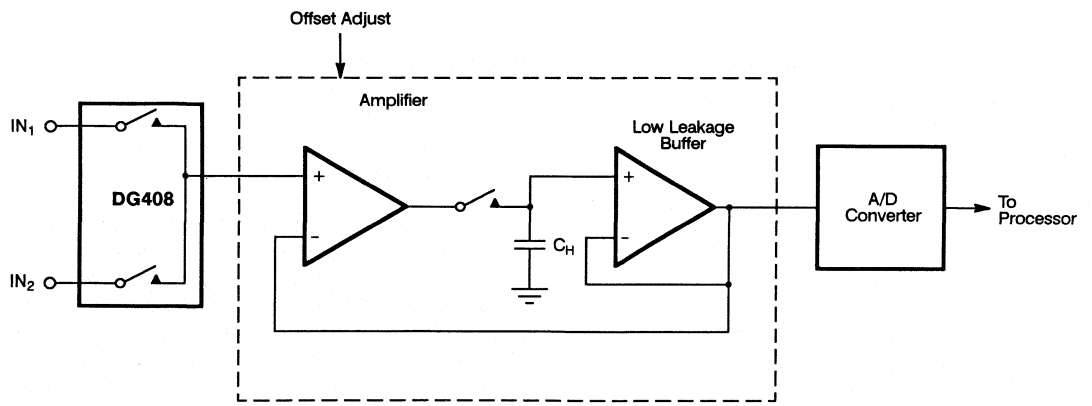

Figure 10. High Performance Sample/Hold Circuit

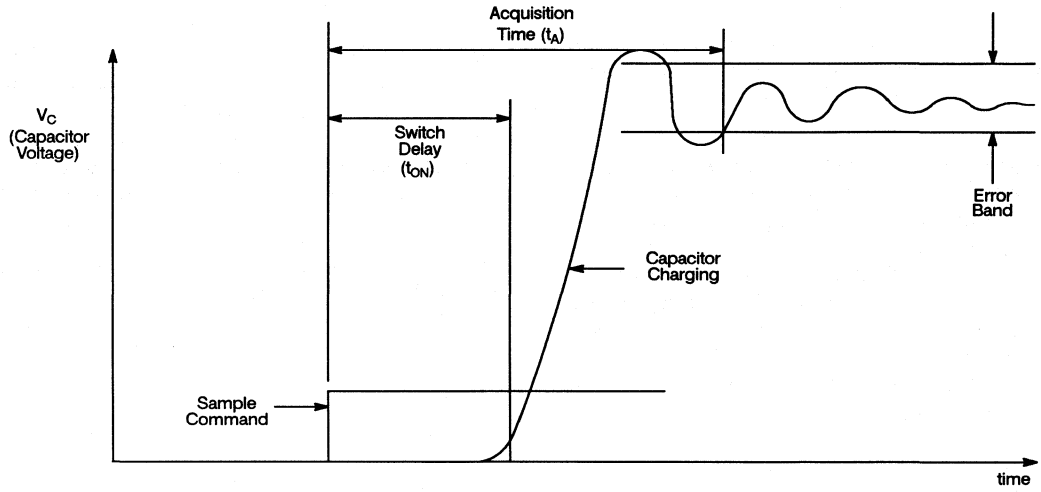

Figure 11. Acquisition Time of a Sample/Hold System

R_S is the source resistance of the analog input
C_H is the hold capacitor

If

C_H = 100 pF
R_S = 50 Ω
n = 10

then for the DG508A,

t_A = 1.5 µs + 10 x (50 + 450) x 100 pF
t_A = 1.5 µs + 500 ns
t_A = 2 µs

Using the same conditions for the DG408,

t_A = 250 ns + 10 x (50 + 100) x 100 pF
t_A = 250 ns + 150 ns
t_A = 400 ns

Thus, by using the DG408, the acquisition time is improved by 5 times.

For high-accuracy systems, an important consideration is the sample-to-hold offset error. This error arises when the switch turns off and charge is injected by the switch onto the hold capacitor, adding an error to the stored analog voltage. The error is related to the hold capacitor by

$$V_O = Q_i/C_H$$

where

V_O is the offset error
Q_i is the injected charge
C_H is the hold capacitor.

As an example of the possible improvement with the DG408, a comparison is drawn with the DG508A. Assuming a 1-nF hold capacitor, for the DG508A,

$$V_O = 50\ pC \div 1\ nF = 50\ mV$$

and for the DG408,

$$V_O = 20\ pC \div 1\ nF = 20\ mV$$

Thus, a 2.5-fold improvement in error voltage is provided by using the DG408.

The ability of the system to store the analog sample when the switch goes off is referred to as the droop rate. It is measured as the change in voltage versus time while in the hold mode. The droop rate depends on bias current of the amplifier, the leakage of the capacitor, and the off-state leakage of the multiplexer. The low-leakage performance of the DG408/409 allows a lower droop rate (i.e., a more accurate storage of the analog sample).

High-Speed Switching

In large segments of the electronics industry, speed is a primary concern in product design. Computer graphics, video equipment, and medical electronics are a few examples where high-speed switching is required. The activation frequency of a multiplexer (i.e., the frequency at which the switch can be toggled) is directly related to the switching speed of the device (i.e., the faster the switching speed, the higher the activation frequency). The DG408 has guaranteed maximum of 250 ns switching speed, thus making it theoretically possible to toggle the switch up to 2 MHz. Figure 12 shows how a two-level multiplexer can be used to increase the data transmission rates in an analog multiplexed system.

Use of the two-level system gives improved performance over a single-level system. Examples of these improvements are listed below.

- Output capacitance results only from the second-level device and not from the sum of the first-level devices.
- The leakage currents at the output node will be reduced from the sum of the second-level devices to that of the second-level device.
- In a design where one multiplexer is sampled while the other is switched, the switching speed of the system is increased to that of the DG400.
- Crosstalk and isolation are improved because one-half of the system will have two off switches in series to the output node at any given time.

Differential Multiplexing of Low-Level Signals

When multiplexing low-level signals, careful choice of a multiplexer and handling of the system layout helps avoid signal masking by ac noise pick-up and dc voltages generated by thermocouple effects. To transmit the signal effectively, several factors must be considered.

- single-ended or differential signal paths
- low-level transmission or preamplification
- the type of conductor

The choice between a single-ended (DG408) or differential (DG409) multiplexer is really a function of the system. Cost will dictate a single-ended connection, and for a high signal level, the shorter distance should provide a stable-environment system. For a system that has a significant signal path length and is potentially being routed in a noisy environment (e.g., motors), common-mode signals can be picked up. For low-level signal transmission, this common-mode signal will provide a significant error. To minimize the effect of the common-mode signals, a twisted pair of wires feed a differential multiplexer, such as the DG409, which is buffered by a differential amplifier that rejects the unwanted common-mode portion of the signal (see Figure 13).

The advantages of low-level or high-level transmission is again dictated by system configuration and cost. Preamplification at the transducer will provide low source impedance and voltage gain, but it introduces the problem of supplying power to the amplifier.

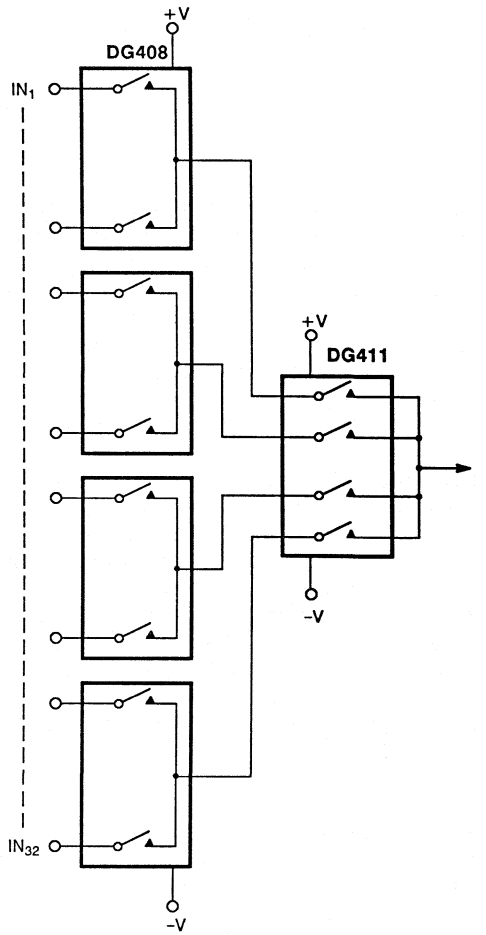

Figure 12. Two-Level Multiplexing with the DG408

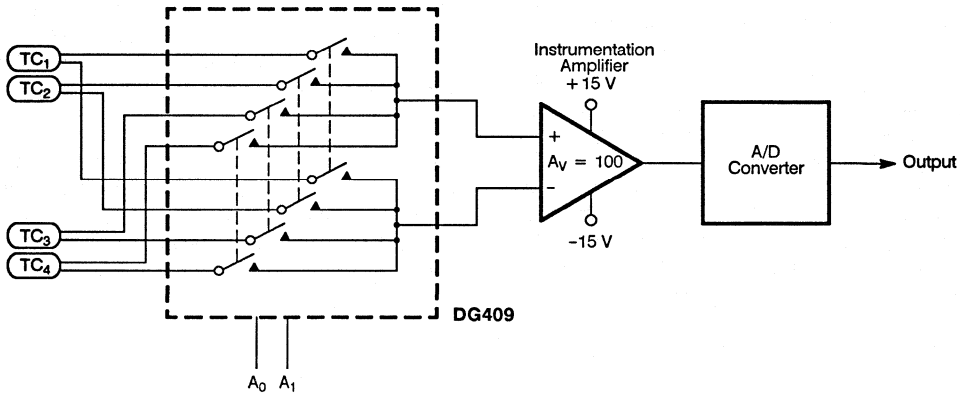

Figure 13. Differential Multiplexing of Thermocouples

The transmission cable carrying the transducer signal is critical in a low-level system; it should be as short as practical. Signal conductors should be tightly twisted for minimum enclosed area. This technique guards against picking up electromagnetic interference and shields the twisted pair of wires against capacitively-coupled (electrostatic) interference. A key requirement for the transmission cable is that it presents a balanced line to the source of noise interference. This requires an equal series impedance in each conductor and an equally distributed impedance from each conductor to ground. The result should be that noise will be coupled in phase to both conductors and rejected as common-mode voltages. Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also ground loops are produced if the shield is grounded at both ends by standard baby "N" connector sockets. If coaxial cable is used, the signal should be carried on the center conductors of two equal-length cables whose shield is terminated only at the transducer end.

Silicon in contact with aluminum creates a thermocouple voltage. In a typical multiplexer, the source voltage will be exactly canceled by the drain voltage, but large thermal gradients between source and drain contacts can produce a net offset voltage. The low current consumption of the DG409 (± 75 μA) translates into minimal errors due to thermocouple offsets.

Programmable Amplifier

Figure 14 shows a programmable amplifier with selectable inputs. This configuration is used in auto-ranging digital volt meters, signal conditioners, etc. Its purpose is to select optimum gain ready for conversion.

Gain ratios are a function of the resistor ratios. Sources of error will be due to the ON-resistance of the switches contributing to the resistor ratio. The low ON-resistance of the DG408 (typically 40 Ω at 25°C) and close matching should minimize ranging errors introduced by the switches. The switching speed of the DG408 will allow the preferred value of gain to be attained quickly.

Conclusion

For multiplexers to maintain their usefulness in high-performance systems, their design must incorporate the latest technological advances. As digital controllers are becoming faster and analog sources more accurate, the modern multiplexer must reflect these advances to become a stronger link in the transition from the analog to the digital world. The DG408 and DG409 are designed to meet these new requirements in the marketplace and reflect Siliconix' commitment to serve our customers' needs for state-of-the-art technology.

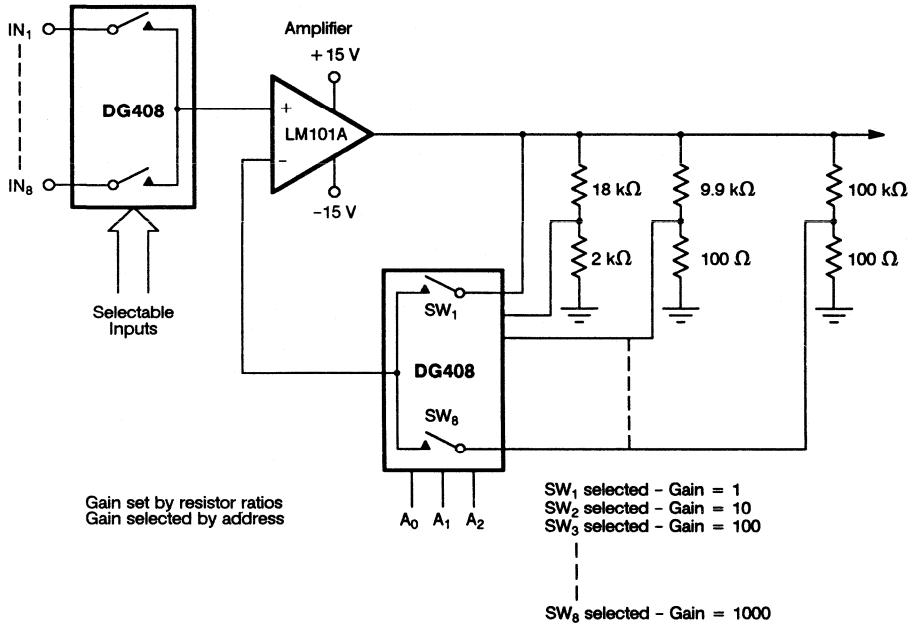

Figure 14. Programmable Amplifier with Selectable Inputs

References

"Multiplexer Adds Efficiency to 32-Channel Telephone Systems," *IC Data Book*, Siliconix, 1988.

Analog Switches and Their Applications, Siliconix, June 1980.

Bylanski, P., *Digital Transmission Systems*, Peter Peregrinus, Ltd., 1976.

"IC Multiplexer Increases Analog Switching Speeds," *IC Data Book*, Siliconix, 1988.

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- PP = 1989/1990 Power Products Data Book
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FAX: 914-897-5611 (Manual Receive)

E. Rochester (14445)
Tri-Tech Electronics, Inc.
300 Main Street
(716) 385-6500
Easylink: 62934993
FAX: 716-385-7655

NEW YORK (Metro/L.I.)

Babylon (11702)
Astrorep Incorporated
103 Cooper Street
(516) 422-2500
TLX: 286852
FAX: 516-422-2504

NORTH CAROLINA

Charlotte (28212)
Rep, Inc.Independence Office Park
6407 Idlewild Road, Ste. 425
(704) 563-5554
FAX: 704-535-7507

Morrisville (27560)
Rep. Inc.
2500 Gateway Centre Blvd.,Ste. 400
(919) 469-9997
FAX: 919-481-3879

NORTH DAKOTA

See Minnesota

OHIO

Beachwood (44122)
Thompson & Assoc. , Inc.
23200 Chagrin Blvd., Bldg. 2
Ste. 325
(216) 831-6277
FAX: 216-831-2553

Dayton (45459)
Thompson & Assoc., Inc.
1065 Centerville Station Rd.
Ste. A
(513) 435-7733
FAX: 513-435-1898

Orient (43146)
Thompson & Assoc., Inc.
5555 Pheasant Dr.
(614) 877-4304
FAX: 614)877-0872

OKLAHOMA

See Texas (Grand Prairie)

OREGON

Portland (97224)
QR /Crown , Inc.
17020 S. W. Upper Boones Ferry Rd.
(503) 620-8320
FAX: 503-639-4023

PENNSYLVANIA (Eastern)

See New Jersey (Southern)

PENNSYLVANIA (Western)

See Ohio

PUERTO RICO

Hato Rey (00918)
Semtronic Associates, Inc.
Mercantil Plaza Bldg.
Suite 816
(809) 766-0700/0701
FAX: 809-763-8071

SOUTH DAKOTA

See Minnesota

U.S. Sales Representatives (Cont'd)

TENNESSEE

Jefferson City (37760)
Rep. Inc.
P. O. Box 728
113 So. Branner Avenue
(615) 475-9012/3
FAX: 615-475-6340

TEXAS

Austin (78750)
Ion Associates, Inc.
9811 Anderson Mill Rd.
Suite 3
(512) 331-7251
FAX: 512-331-7254

Grand Prairie (75050)
Ion Associates, Inc.
1504 109th Street
(214) 647-8225
Easylink: 62956328
FAX: 214-641-9839

Houston (77014-1696)
Ion Associates, Inc.
14300 Cornerstone Village Drive
Suite 228
(713) 537-7717
FAX: 713-537-5612

TEXAS (El Paso Area)

See New Mexico

UTAH

See Washington

VERMONT

See Massachusetts

VIRGINIA

Charlottesville (22901)
Third Wave Solutions
2100 Wisteria Drive
(804) 974-7575
FAX: 804-974-7480

WASHINGTON

Bellevue (98005)
QR/Crown, Inc.
375 118th Ave., S.E.
(206) 453-5100
FAX: 206-646-8775

WEST VIRGINIA

See Ohio

WEST WISCONSIN

See Minnesota

WISCONSIN

Wauwatosa (53226)
Larsen Associates, Inc.
10855 West Potter Road
(414) 258-0529
FAX: 414-258-9655

WYOMING

See Colorado

DISTRICT OF COLUMBIA

See Maryland

Canadian Sales Representatives

Islington, Ontario (M9B6E3)
Pipe Thompson, Ltd.
5468 Dundas Street W.
Suite 206
(416) 236-2355
FAX: 416-236-3387

Kanata, Ontario (K2M2B8)
Pipe Thompson, Ltd.
(613) 591-1821
FAX: 613-591-0461

Chip Distributor

FLORIDA

Orlando (32810)
Chip Supply, Inc.
7725 N. Orange Blossom Trail
(407) 298-7100
TWX: 810-850-0103
FAX: 407-290-0164

U.S. Distributors

ALABAMA

Huntsville (35805)
Hamilton/Avnet, #23
4940 Research Drive
(205) 837-7210
FAX: 205-721-0356

Huntsville (35801)
Marshall Industries
3313 Memorial Parkway
(205) 881-9235
FAX: 205-881-1490

Huntsville (35805)
Pioneer Tech.
4825 University Square
(205) 837-9300
FAX: 205-837-9358

ARIZONA

Chandler (85226)
Hamilton/Avnet, #04
30 S. Mc Kemy Ave.
(602) 961-6400
TWX: 910-950-0077
FAX: 602-961-4555

Phoenix (85044)
Marshall Industries
9830 S. 51st St., Ste. B121
(602) 496-0290
TWX: 910-950-1946
FAX: 602-893-9029

Phoenix (85040)
Wyle Laboratories-EMG
4141 E. Raymond St., Suite 1
(602) 437-2088
TWX: 910-951-4282

CALIFORNIA

Agoura Hills (91301)
Zeus Components
5236 Colodny Drive
(818) 889-3838
FAX: 818-889-2464

Calabasas (91302)
Wyle Laboratories
26677 W. Agoura
(818) 880-9000
FAX: 818-880-5510

Chatsworth (91311)
Marshall Industries
9710 DeSoto Avenue
(818) 407-0101
FAX: 818-709-5334

Costa Mesa (92626)
Hamilton/Avnet, #29
3170 Pullman Street
(714) 641-4100
FAX: 714-641-4122

Culver City (90230)
Hamilton Corporate
10950 Washington Blvd.
(213) 558-2000
FAX: 213-558-2076

El Monte (91731)
Marshall Corporate
9320 Telstar Avenue
(818) 307-6000
FAX: 818-307-6297

Gardena (90248)
Hamilton Electro Sales, #01
1361 "B" W. 190th Street
(213) 217-6850
FAX: 213-217-6822

Irvine (92718)
Marshall Industries
1 Morgan
(714) 859-5050
FAX: 714-581-5255

Irvine (92714)
Wyle Laboratories-EMG
17872 Cowan Avenue
(714) 863-9953
TWX: 910-348-7140
FAX: 714-863-0473

Irvine (92715)
Wyle Military
18910 Teller Ave.
(714) 851-9953
FAX: 714-851-8366

Milpitas (95035)
Marshall Industries
336 Los Coches
(408) 942-4600
FAX: 408-262-1224

Rancho Cordova (95670)
Marshall Industries
3039 Kilgore Ave. #140
(916) 635-9700
FAX: 916-635-6044

Rancho Cordova (95742)
Wyle Distribution Group
Sacramento Division
2951 Sunrise Blvd., Ste. 175
(916) 638-5282
FAX: 916-638-1491

Reseda (91335)
JAN Devices
6925 Canby, Bldg. 109
(818) 708-1100
TWX: 910-997-1130
FAX: 818-708-7436

Rocklin (95677)
Bell Industries
4311 Anthony Ct., #100
(916) 652-0414
FAX: 916-652-0403

U.S. Distributors (Cont'd)

CALIFORNIA (Cont'd)

Sacramento (95348)
Hamilton/Avnet, #35
4103 Northgate Blvd.
(916) 920-3150
FAX: 916-925-3478

San Diego (92123)
Hamilton/Avnet, #02
4545 Viewridge Avenue
(619) 571-7500
FAX: 619-277-6136

San Diego (92123)
Marshall Industries
10105 Carroll Canyon Road
(619) 578-9600
FAX: 619-586-0469

San Diego (92123)
Wyle Laboratories-EMG
9525 Chesapeake Drive
(619) 565-9171
TWX: 910-335-1590
FAX: 619-565-9171, X274

San Diego (92123)
Zeus Components
5625 Ruffin Rd. #200
(619) 277-9681
FAX: 619-541-2758

San Jose (95119)
Zeus Components
6276 San Ignacio Ave., Ste. E
(408) 629-4789
FAX: 408-629-4792

Santa Clara (95052)
Wyle Distribution Group
3000 Bowers Avenue
(408) 727-2500
TWX: 910-379-6480
FAX: 408-988-3240

Sunnyvale (94086)
Bell Industries
1161 No. Fairoaks Avenue
(408) 734-8570
TWX: 910-339-9378
Fax: 408-734-8875

Sunnyvale (94086)
Hamilton/Avnet, #03
1175 Bordeaux Avenue
(408) 743-3300
FAX: 408-745-6679

Woodland Hills (91367)
Hamilton /Avnet. #48
21150 Califa St.
(818) 594-0404
FAX: 818-594-8234

Yorba Linda (92686)
Zeus Components
22700 Savi Ranch Pkwy.
(714) 921-9000
TWX: 910-591-1696
FAX: 714 -921-2715

COLORADO

Englewood (80112)
Hamilton/Avnet, #06
9605 Marcon Cir. #200
(303) 799-7800
FAX: 303-799-7801

Thornton (80221)
Marshall Industries
12351 N. Grant St.
(303) 451-8444
TWX: 910-989-1657
FAX: 303-457-2899

Thornton (80241)
Wyle Distribution Group
451 E. 124th Avenue
(303) 457-9953
TWX: 910-936-0770
FAX: 303-457-4831

Wheatridge (80033)
Bell Industries
12421 W. 49th Avenue
(303) 424-1985
TWX: 910-938-0393
FAX: 303-424-0932

CONNECTICUT

Danbury (06810)
Hamilton/Avnet, #21
Commerce Drive
Commerce Park
(203) 797-2800
FAX: 203-791-9050

Milford (06460)
Falcon Electronics
5 Higgins Drive
(203) 878-5272
TWX: 710-462-8407
FAX: 203-877-2010

Norwalk (06851)
Pioneer Std.
112 Main Street
(203) 853-1515
TWX: 710-468-3373
FAX: 203-838-9901

Wallingford (06492)
Marshall Industries
20 Sterling Drive
Barnes Industrial Park
(203) 265-3822
TWX: 910-997-5197
FAX: 203-284-9285

FLORIDA

Altamonte Springs (32701)
Future Electronics
380 S. Northlake Blvd.,
Suite 1048
(407) 767-8414
FAX: 407-834-9318

Altamonte Springs (32701)
Marshall Industries
380 S. Northlake Blvd.,Ste.1024
(407) 767- 8585
FAX: 407-767-8676

Altamonte Springs (32701)
Pioneer Tech.
337 South North-Lake Blvd. #1000
(407) 834-9090
TWX: 810-850-0177
FAX: 407-834-0665

Clearwater (34620)
Future Electronics
4900 N. Creekside Drive
(813) 578-2770
FAX: 813-576-7600

Deerfield Beach (33441)
Pioneer Tech.
674 S. Military Trail
(305) 428-8877
FAX: 305-481-2950

Fort Lauderdale (33309)
Hamilton/Avnet, #17
6801 N.W. 15th Way
(305) 979-2802
TWX: 510-956-3097
FAX: 305-971-5420

Fort Lauderdale (33309)
Marshall Industries
2700 W. Cypress Creek Blvd.
Suite C106
(305) 977-4880
FAX: 305-977-4887

Oveida (32765)
Zeus Components
1750 W. Broadway, Ste. 114
(407) 365-3000
FAX: 407-365-2356

St. Petersburg (33702)
Hamilton/Avnet, #25
3247 Tech Drive No.
(813) 573-3930
FAX: 813-572-4329

Winter Park (32792)
Hamilton/Avnet, #76
6947 University Blvd.
(407) 628-3888
TWX: 810-853-0322
FAX: 407-678-1878

GEORGIA

Norcross (30092)
Hamilton/Avnet, #15
5825 Peachtree Corners E-D
(404) 447-7500
FAX: 404-447-7526

Norcross (30071)
Future Electronics
3000 Northwoods Parkway
Suite 295
(404) 441-7676
FAX: 404-441-7580

Norcross (30093)
Marshall Industries
5300 Oakbrook Pkwy.,Ste.140
(404) 923-5750
TWX: 810-766-3969
FAX: 404-923-2743

Norcross (30071)
Pioneer Tech.
3100 F Northwoods Place
(404) 448-1711
FAX: 404-446-8270

ILLINOIS

Bensenville (60106)
Hamilton/Avnet, #10
1130 Thorndale Avenue
(708) 860-7780
TWX: 910-227-0060
FAX: 708-860-8530

Addison (60101)
Pioneer Std.
2171 Executive Drive
Suite 200
(708) 495-9680
FAX: 708-495-9831

Schaumburg (60173)
Marshall Industries
50 E. Commerce Dr., Ste. 1
(708) 490-0755
TWX: 910-256-0036
FAX: 708-490-0569

INDIANA

Carmel (46032)
Hamilton/Avnet, #28
485 Gradle Drive
(317) 844-9333
FAX: 317-844-5921

Indianapolis (46278)
Marshall Industries
6990 Corporate Drive
(317) 297-0483
FAX: 317-297-2787

Indianapolis (46240)
Pioneer Std.
9350 N. Priority Way West Dr.
(317) 573-0880
(800) 332-5503 (IN)
(800) 428-9128 (IL, KY)
FAX: 317-573-0979

IOWA

Cedar Rapids (52404)
Hamilton/Avnet, #44
915 33rd Avenue
(319) 362-4757

KANSAS

Lenexa (66214)
Marshall Industries
10413 W. 84th Terrace
(913) 492-3121
FAX: 913-492-6205

Lenexa (66219)
Hamilton/Avnet, #58
15313 W. 95th
(913) 888-8900
FAX: 913-541-7951

KENTUCKY

Lexington (40511)
Hamilton/Avnet
805A Newtown Circle
(606) 259-1475
FAX: 606-252-3238

MARYLAND

Columbia (21045)
Hamilton/Avnet, #12
6822 Oak Hall Lane
(301) 995-3500 (MD)
(301) 621-5410 (DC)
FAX: 301-995-3593

Columbia (21045)
Zeus Components
8930-A Route 108
(301) 997-1118
FAX: 301-964-9784

Gaithersburg (20760)
Pioneer Tech.
9100 Gaither Road
(301) 921-0660
TWX: 710-828-0545
FAX: 301-622-0451

Silver Springs (20877)
Marshall Industries
2221 Broad Birch Dr., Ste. G
(301) 622-1118
FAX: 301-622-0451

MASSACHUSETTS

Lexington (02173)
Pioneer Std.
44 Hartwell Ave.
(617) 861-9200
FAX: 617-863-1547

Lexington (02173)
Zeus
429 Marrett Road
(617) 863-8800
FAX: 617-863-8807

Peabody (01960)
Hamilton/Avnet, #18
10 D Centennial Drive
(508) 531-7430
FAX: 508-532-9802

Westborough (01581)
Future Electronics
133 Flanders Road
(508) 366-2400
FAX: 508-366-1195

Wilmington (01887)
Marshall Industries
33 Upton Dr.
(508) 658-0810
TWX: 710-332-6359
FAX: 508-658-7608

U.S. Distributors (Cont'd)

MICHIGAN

Grand Rapids (49508)
Hamilton/Avnet, #67
2215 29th Street S.E. A-5
(616) 243-8805
FAX: 616-243-0028

Grand Rapids (49508)
Pioneer Std.
4505 Broadmoor Ave. SE
(616) 698-1800
FAX: 616-698-1831

Livonia (48150)
Marshall Industries
31067 Schoolcraft
(313) 525-5850
FAX: 313-525-5855

Livonia (48150)
Pioneer Std.
13485 Stamford
(313) 525-1800
FAX: 313-427-3720

Novi (48050)
Hamilton/Avnet, #66
41650 Gardenbrook, #100
(313) 347-4270
FAX: 313-347-4021

MINNESOTA

Eden Prairie (55344)
Pioneer Std.
7625 Golden Triangle Dr.
(612) 944-3355
FAX: 612-944-3794

Minnetonka (55343)
Hamilton/Avnet, #63
12400 Whitewater Dr.
(612) 932-0600
FAX: 612-932-0613

Plymouth (55441)
Marshall Industries
3955 Annapolis Lane
(612) 559-2211
FAX: 612-559-8321

MISSOURI

Bridgeton (63043)
Marshall Industries
12774 Boenker
(314) 291-4650
FAX: 314-291-5391

Chesterfield (63005)
Hamilton/Avnet, #05
741 Goddard
(314) 537-4265
FAX: 314-537-4248

NEW HAMPSHIRE

Manchester (63017)
Hamilton/Avnet, #75
444 E. Industrial Park Drive
(603) 624-9400
TWX: 710-474-3255
FAX: 603-624-2402

NEW JERSEY

Cherry Hill (08003)
Hamilton/Avnet, #14
One Keystone Avenue
(609) 424-0100
TWX: 710-940-0262
FAX: 609-751-8624

Fairfield (07006)
Hamilton/Avnet, #19
10 Industrial Road
(201) 575-3390
TWX: 710-734-4388
FAX: 201-575-5839

Fairfield (07006)
Marshall Industries
101 Fairfield Road
(201) 882-0320
TWX: 710-989-7052
FAX: 201-882-0095

Fairfield (07006)
Pioneer Std.
14 "A" Madison
(201) 575-3510
TWX: 710-734-4382
FAX: 201-575-3454

Mt. Laurel (08054)
Marshall Industries
158 Gaither Dr., Unit 100
(609) 234-9100 (NJ)
(215) 627-1920 (PA)
FAX: 609-778-1819

NEW MEXICO

Albuquerque (87123)
Bell Industries
11728 Linn N.E.
(505) 292-2700
FAX: 505-275-2819

Albuquerque (87106)
Hamilton/Avnet, #22
5659 Jefferson St. N.E.
Ste. A & B
(505) 345-0001
TWX: 910-989-0614
FAX: 505-345-2024

NEW YORK

Binghamton (13904)
Pioneer Std.
69 Corporate Dr.
(607) 722-9300
FAX: 607-722-9562

Buffalo (14202)
Summit, Inc.
916 Main Street
(716) 887-2800
TWX: 710-522-1692
FAX: 716-887-2866

East Syracuse (13206)
Hamilton/Avnet, #08
103 Twin Oaks Drive
(315) 437-2642
TWX: 710-541-1560
FAX: 315-432-0740

Fairport (14450)
Pioneer Std.
840 Fairport Rd.
(716) 381-7070
TWX: 510-253-7001
FAX: 716-381-5955

Hauppauge (11788)
Hamilton/Avnet, #20
933 Motor Parkway
(516) 231-9800
FAX: 516-434-7426

Hauppauge (11787)
Marshall Industries
275 Oser Avenue
(516) 273-2424 and
(516) 273-2053
FAX: 516-434-4775

Johnson City (13790)
Marshall Industries
129 Brown Street
(607) 798-1611
FAX: 607-797-7031

Port Chester (10523)
Zeus Components
100 Midland Avenue
(914) 937-7400
TWX: 710-567-1248
FAX: 914-937-2553

Rochester (14623)
Hamilton/Avnet, #61
2050 Town Line Road
(716) 475-9130
FAX: 716-475-9119

Rochester (14623)
Marshall Industries
1250 Scottsville Road
(716) 235-7620
TWX: 510-253-5526
FAX: 716-235-0052

Ronkonkoma (11779)
Zeus Components
2110 Smithtown Ave.
(516) 737-4500
FAX: 516-737-4520

Westbury (11590)
Hamilton/Avnet, #39
1065 Old Country Road
(516) 997-6868
FAX: 516-997-6375

Woodbury (11797)
Pioneer Std.
60 Crossways Park W.
(516) 921-8700
TWX: 510-221-2184
FAX: 516-921-2143

NORTH CAROLINA

Charlotte (28209)
Future Electronics
1515 Mockingbird Lane, Ste. 801
(704) 529-5500
FAX: 704-527-2222

Charlotte (28210)
Pioneer Tech.
9801-A Southern Pine Blvd.
(704) 527-8188
TWX: 810-620-0366
FAX: 704-522-8564

Raleigh (27604)
Hamilton/Avnet, #24
3510 Spring Forrest Road
(919) 878-0819, X210
TWX: 510-928-1836
FAX: 919-872-4435

Raleigh (27604)
Marshall Industries
5221 N. Blvd.
(919) 878-9882
TWX: 910-997-5209
FAX: 919-872-2431

OHIO

Cleveland (44105)
Pioneer Std.
4800 E. 131st Street
(216) 587-3600
FAX: 216-587-3906

Dayton (45459)
Hamilton/Avnet, #64
954 Senate Drive
(513) 439-6700
FAX: 513-439-6711

Dayton (45414)
Marshall Industries
3520 Park Center Dr.
(513) 898-4480
FAX: 513-898-9636

Dayton (45424)
Pioneer Std.
4433 Interpoint Blvd.
(513) 236-9900
TWX: 810-459-1622
FAX: 513-236-8133

Dayton (45439)
Zeus Components
2912 Springboro West
(513) 293-6162
FAX: 513-293-1781

Solon (44139)
Hamilton/Avnet, #62
30325 Bainbridge Rd., Bldg. A
(215) 349-5100
FAX: 216-349-1894

Solon (44139)
Marshall Industries
30700 Bainbridge Rd. Unit A
(216) 248-1788
FAX: 216-248-2312

Westerville (43081)
Hamilton/Avnet, #79
777 Brooks Edge Boulevard
(614) 882-7004
FAX: 614-882-8650

OKLAHOMA

Tulsa (74146)
Hamilton
12121 E. 51st St., Suite 102
(918) 252-7297
FAX: 918-250-8763

Tulsa (74146)
Quality Components
3158 S. 108th E. Ave., Ste # 274
(918) 664-8812
FAX: 918-664-8515

OREGON

Beaverton (97005)
Hamilton/Avnet, #27
9409 SW Nimbus Ave.
(503) 627-0201
FAX: 503-636-1327

Beaverton (97005)
Marshall Industries
9705 S.W. Gemini
(503) 644-5050
FAX: 503-646-8256

Beaverton (97005)
Wyle Laboratories-EMG
9640 Sunshine Ct.
Bldg. G-200
(503) 643-7900
FAX: 503-646-5466

PENNSYLVANIA

Horsham (19044)
Pioneer Tech.
261 Gibralter Road
(215) 674-4000
TWX: 510-665-6778
FAX: 215-674-3107

Pittsburgh(15222)
Hamilton/Avnet, #43
2800 Liberty Avenue, Bldg. E.
(412) 281-4150
FAX: 412-281-8662

Pittsburgh (15205)
Marshall Electronics
401 Parkwayview Drive
(412) 788-0441
FAX: 412-788-0447

Pittsburgh(15238)
Pioneer Std.
259 Kappa Drive
(412) 782-2300
FAX: 412-963-8255

TEXAS

Addison (75001)
Quality Components
4257 Kellway Circle
(214) 733-4300
FAX: 214-250-0216

Austin (78758)
Hamilton/Avnet, #26
1807A W. Braker
(512) 837-8911
FAX: 512-832-4315

Austin (78754)
Marshall Industries
8504 Cross Park Dr.
(512) 837-1991
FAX: 512-832-9810

U.S. Distributors (Cont'd)

TEXAS (Cont'd)

Austin (78758)
Pioneer Std.
1826D Kramer Lane
(512) 835-4000
FAX: 512-835-9829

Austin (78758)
Quality Components
2120-M W. Braker Lane
(512) 835-0220
FAX: 512-339-9252

Austin (78759)
Wyle Distribution
4030 W. Braker Lane
Ste. 330
(512) 345-8853
FAX: 512-345-9330

Carrollton (75006)
Marshall Industries
2045 Chenault St.
(214) 233-5200
FAX: 214-770-0675

Dallas (75244)
Hamilton/Avnet, #16
4004 Beltline Rd.
(214) 404-9906
FAX: 214-308-8109

Dallas (75244)
Pioneer Std.
13765 Beta Road
(214) 386-7300
FAX: 214-490-6419

El Paso (79935)
Marshall Industries
2150 Trawood, Ste. B-160
(915) 593-0706
FAX: 915-594-1894

Houston (77099)
Pioneer Std.
10530 Rockley St. 100
(713) 495-4700
FAX: 713-495-5642

Houston (77478)
Wyle Distribution
11001 S. Willcrest, #100
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FAX: 713-879-6540

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1810 N. Greenville Avenue
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FAX: 214-644-5064

Richardson (75081)
Zeus Components
1800 N. Glenville Drive
Suite 120
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FAX: 214-234-4385

Stafford (77477)
Hamilton/Avnet, #11
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(713) 240-7733
FAX: 713-240-0582

Sugarland (77478)
Quality Components
1005 Industrial Rd.
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UTAH

Salt Lake City (84121)
Hamilton/Avnet, #09
1100 E. 6600 S., Ste. 120
(801) 266-2022
FAX: 801-977-9266

Salt Lake City (84115)
Marshall Industries
466 Lawndale Dr., Ste. #C
(801) 485-1551
FAX: 801-487-0936

West Valley City (84119)
Wyle Laboratories-EMG
1325 W. 2200 S.
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FAX: 801-972-2524

WASHINGTON

Bothell (98011)
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11715 N. Creek Pkwy, South
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Redmond (98052)
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17761 N.E. 78th Pl.
(206) 881-6697
FAX: 206-867-0159

Redmond (98052)
Wyle Distribution Group
15385 N.E. 90th Street
(206) 881-1150
FAX: 206-881-1567

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Milwaukee (53214)
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1563 South 101st Street
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FAX: 414-771-2847

Waukesha (53186)
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W227N913 W. Mound Dr.
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Waukesha (53186)
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FAX: 414-784-9509

Waukesha (53186)
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CALGARY (TZE 6Z3)
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Vancouver (V5K 4X7)
Future Electronics
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(604) 294-1166
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ONTARIO

Brampton (L6O 5G3)
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Downsview (M3J 1Z3)
Future Electronics
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FAX: 514-695-3707

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Singapore 1647
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TLX: RS 35382 DOS
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Electrolink (PTY) Ltd.
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Capetown 8000
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TLX: 527-7320

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Don Business Corp.
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Lane 251
Nanking East Road
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TEL: (02) 7636670/6
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CABLE: DONBC TAIPEI
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New Dynamar International LTD
14th Fl. No. 186 Nanking East Road
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